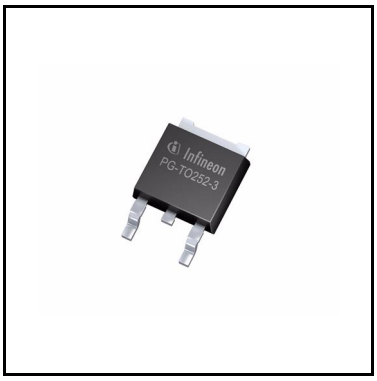
OPTIREG™ linear TLF80511TF

Low dropout linear fixed voltage regulator



Features

- Output voltages 5 V and 3.3 V
- Output voltage precision ±2%
- Output current up to 400 mA
- Ultra low current consumption of 38 µA
- Very low dropout voltage: 100 mV at 100 mA output current
- Extended operating range starting at 3.3 V
- Small output capacitor 1 µF
- Output current limitation
- Overtemperature shutdown
- Wide temperature range from -40°C up to 150°C
- Green Product (RoHS-compliant)

Potential applications

- Suitable for use in automotive electronics

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLF80511TF is a linear low dropout voltage regulator for load currents of up to 400 mA. An input voltage of up to 40 V is regulated to $V_{Q,nom}$ = 5 V (TLF80511TFV50) or $V_{Q,nom}$ = 3.3 V (TLF80511TFV33) with ±2% precision.

The TLF80511TF, with a typical quiescent current of 38 µA, is the ideal solution for systems requiring very low operating currents, such as those permanently connected to a battery.

It features a very low dropout voltage of 100 mV when the output current is less than 100 mA. In addition, the dropout region begins at input voltages of 3.3 V (extended operating range). This makes the TLF80511TF suitable to supply automotive systems.

In addition, the TLF80511's new fast regulation concept requires only a single 1 µF output capacitor to maintain stable regulation.

The device is designed for the harsh environment of automotive applications. Therefore, standard features like output current limitation and overtemperature shutdown are implemented and protect the device against failures like output short circuit to GND, overcurrent, and overtemperature. The TLF80511TF can also be used in all other applications requiring a stabilized 5 V or 3.3 V supply voltage.

Type	Package	Marking
TLF80511TFV50	PG-TO252-3	80511V5
TLF80511TFV33	PG-TO252-3	80511V3

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1 Block diagram

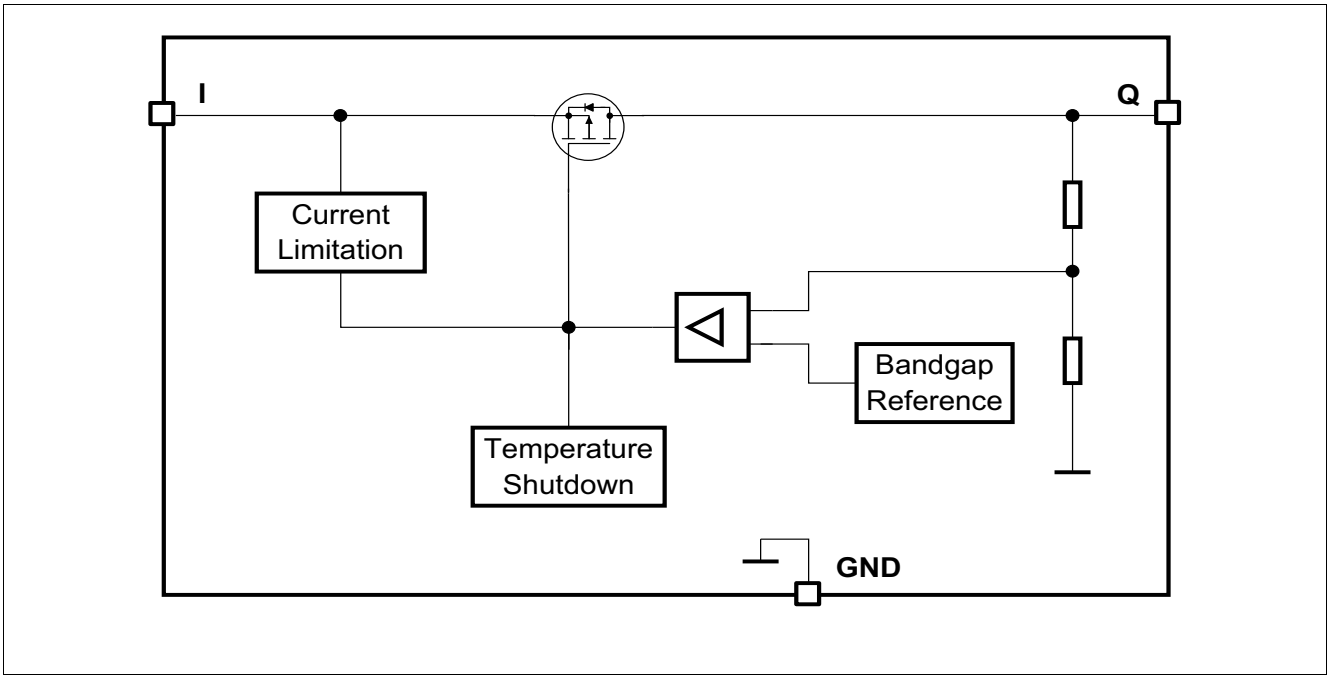


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

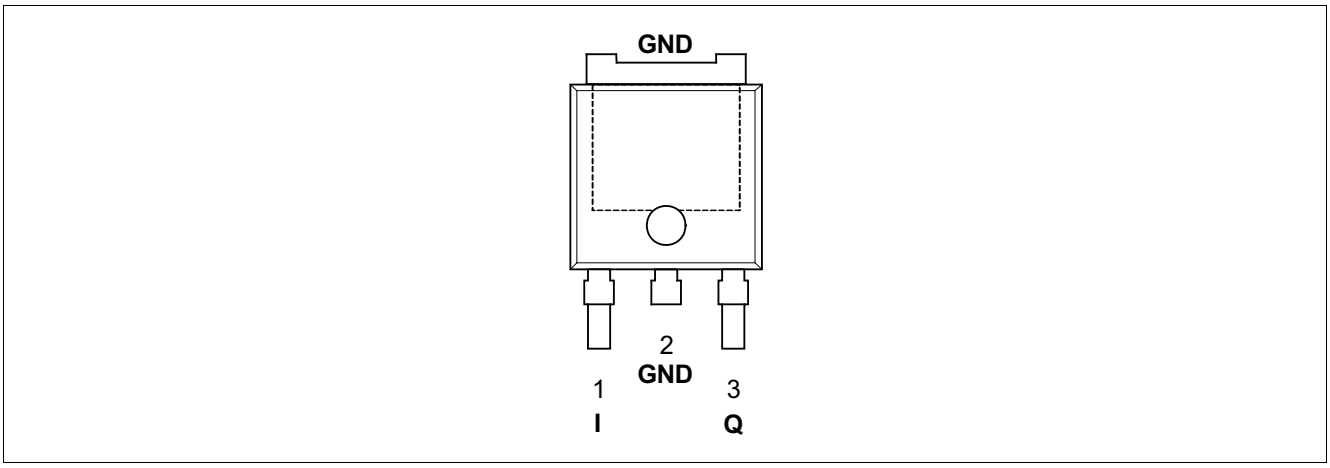


Figure 2 Pin configuration

2.2 Pin definitions and functions

Table 1 Pin definition and functions

Pin	Symbol	Function
1	I	**Input** For compensating line influences, a capacitor to GND close to the IC terminals is recommended
2	GND	**Ground**
3	Q	**Output** Block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in **Table 3**
Tab	GND	Heat slug Connect to heatsink area; connect with GND on PCB

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings [1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Voltage	V_I	-0.3	–	45	V	–	P_4.1.1
Output Q							
Voltage	V_Q	-0.3	–	7	V	–	P_4.1.2
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.3
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.4
ESD susceptibility							
ESD susceptibility	$V_{ESD,HBM}$	-4	–	4	kV	[2)] Human body model (HBM)	P_4.1.5
ESD susceptibility	$V_{ESD,CDM}$	-1.5	–	1.5	kV	[3)] Charge device model (CDM)	P_4.1.6

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).

3) ESD susceptibility, charged device model (CDM) according to JEDEC JESD22-C101.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range for normal operation	V_I	$V_{Q,nom} + V_{dr}$	–	40	V	–	P_4.2.1
Extended input voltage range	$V_{I,ext}$	3.3	–	40	V	1) $T_j > 25°C$	P_4.2.2
Output capacitor's requirements for stability	C_Q	1	–	–	µF	2)	P_4.2.3
Output capacitor's requirements for stability	$ESR(C_Q)$	–	–	5	Ω	3)	P_4.2.4
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.5

1) Between minimum value and $V_{Q,nom} + V_{dr}$: $V_Q = V_I - V_{dr}$. Below minimum value: $V_Q = 0$ V.
2) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.
3) Relevant ESR value at $f = 10$ kHz.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal resistance 1)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	4	–	K/W	–	P_4.3.1
Junction to ambient	R_{thJA}	–	27	–	K/W	2)	P_4.3.2
Junction to ambient	R_{thJA}	–	95	–	K/W	3) Footprint only	P_4.3.3
Junction to ambient	R_{thJA}	–	52	–	K/W	3) 300 mm² heatsink area on PCB	P_4.3.4
Junction to ambient	R_{thJA}	–	39	–	K/W	3) 600 mm² heatsink area on PCB	P_4.3.5

1) Not subject to production test, specified by design.
2) The specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on an FR4 2s2p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.
3) The specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on an FR4 1s0p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with one copper layer (1 × 70 µm Cu).

4 Block description and electrical characteristics

4.1 Voltage regulation

The output voltage V_Q is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature, and the internal circuit design. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in **Table 3** must be maintained. For details see the typical performance graph **Stability region: equivalent serial resistor ESR(C_Q) versus output current I_Q**. Since the output capacitor is used to buffer load steps, it should be sized according to the application's needs.

An input capacitor C_I is not required for stability, but is recommended to compensate line fluctuations. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the regulator terminals.

Whenever the load current exceeds the specified limit, for example, in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (for example, output continuously short-circuited) by switching off the power stage. After the chip has cooled, the regulator restarts. This oscillatory thermal behavior causes the junction temperature to exceed the 150°C maximum and significantly reduces the IC's life.

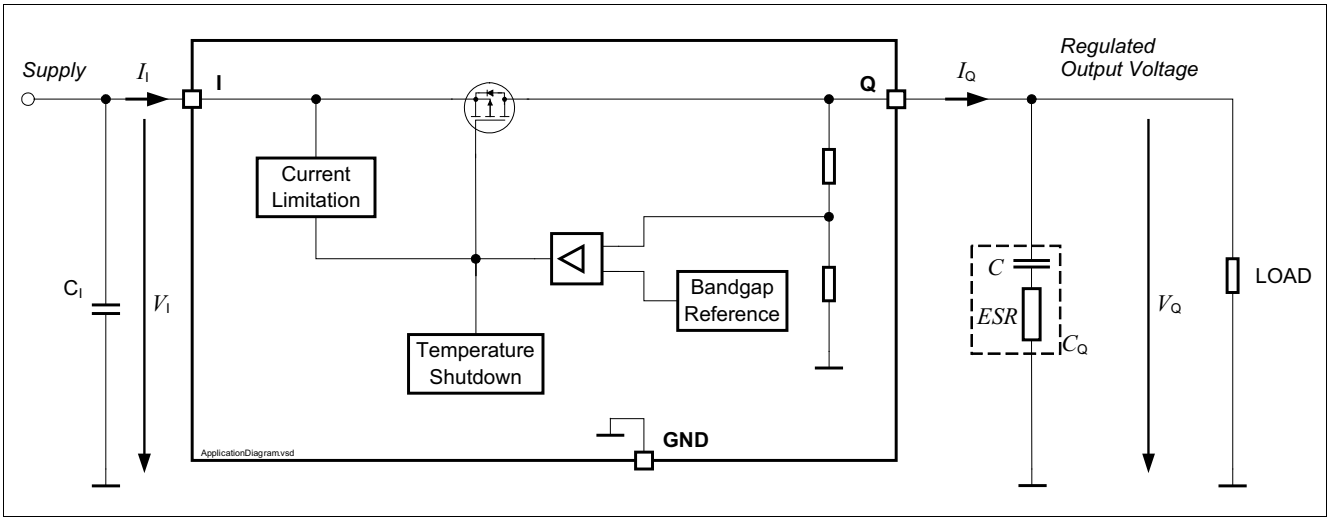


Figure 3 Block diagram: voltage regulation

Table 5 Electrical characteristics: voltage regulator, 5 V, and 3.3 V versions

V_I = 13.5 V; T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

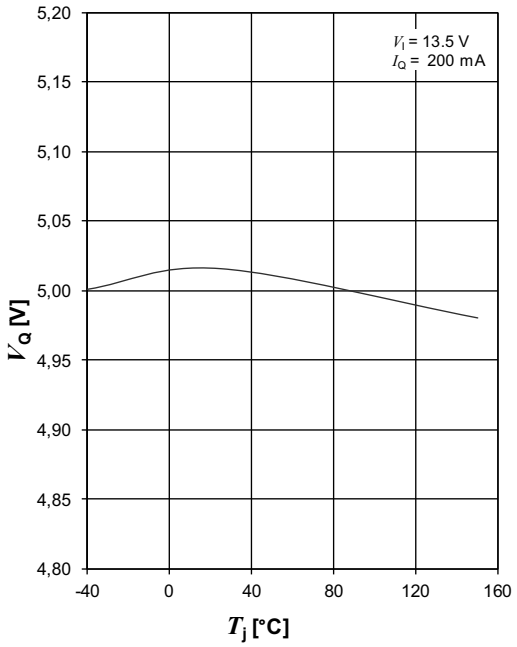
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage precision TLF80511TFV50	V_Q	4.9	5.0	5.1	V	0.05 mA < I_Q < 400 mA 6 V < V_I < 28 V	P_5.1.1
Output voltage precision TLF80511TFV50	V_Q	4.9	5.0	5.1	V	0.05 mA < I_Q < 200 mA 5.5 V < V_I < 40 V	P_5.1.2
Output voltage precision TLF80511TFV33	V_Q	3.23	3.3	3.37	V	0.05 mA < I_Q < 400 mA 4.4 V < V_I < 28 V	P_5.1.3
Output voltage precision TLF80511TFV33	V_Q	3.23	3.3	3.37	V	0.05 mA < I_Q < 200 mA 3.9 V < V_I < 40 V	P_5.1.4
Output current limitation	$I_{Q,max}$	401	600	900	mA	0 V < V_Q < 4.8 V	P_5.1.5
Load regulation steady-state	$\lvert\Delta V_{Q,load}\rvert$	–	20	50	mV	I_Q = 0.05 mA to 400 mA V_I = 6 V	P_5.1.6
Line regulation steady-state	$\lvert\Delta V_{Q,line}\rvert$	–	10	30	mV	V_I = 8 V to 32 V I_Q = 5 mA	P_5.1.7
Dropout voltage $V_{dr} = V_I - V_Q$ TLF80511TFV50	V_{dr}	–	250	500	mV	1) I_Q = 250 mA	P_5.1.8
Dropout voltage $V_{dr} = V_I - V_Q$ TLF80511TFV50	V_{dr}	–	100	–	mV	1) I_Q = 100 mA	P_5.1.9
Dropout voltage $V_{dr} = V_I - V_Q$ TLF80511TFV33	V_{dr}	–	320	650	mV	1) I_Q = 250 mA	P_5.1.10
Dropout voltage $V_{dr} = V_I - V_Q$ TLF80511TFV33	V_{dr}	–	130	–	mV	1) I_Q = 100 mA	P_5.1.11
Power supply ripple rejection TLF80511TFV50	*PSRR*	–	55	–	dB	2) f_{ripple} = 100 Hz V_{ripple} = 0.5 Vpp	P_5.1.12
Overtemperature shutdown threshold	$T_{j,sd}$	151	175	200	°C	2) T_j increasing	P_5.1.13
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	K	2) T_j decreasing	P_5.1.14

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

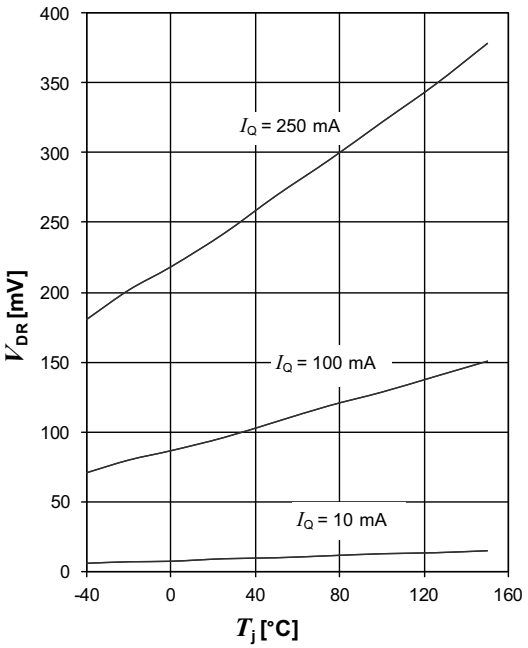
2) Not subject to production test, specified by design.

4.2 Typical performance characteristics: voltage regulator

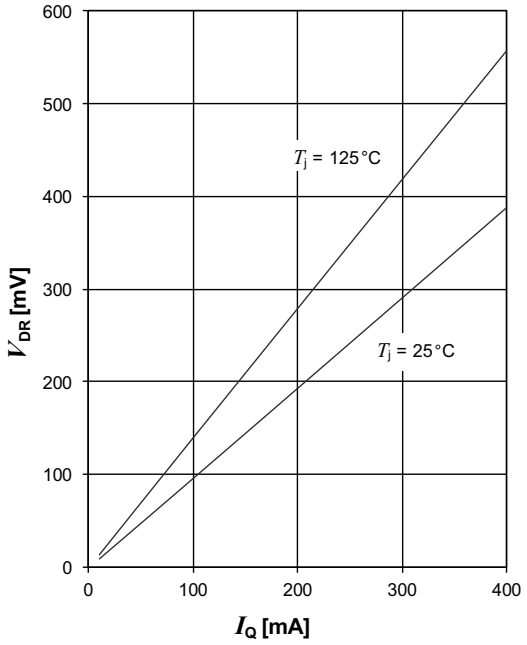
Output voltage V_Q versus junction temperature T_j (TLF80511TFV50)



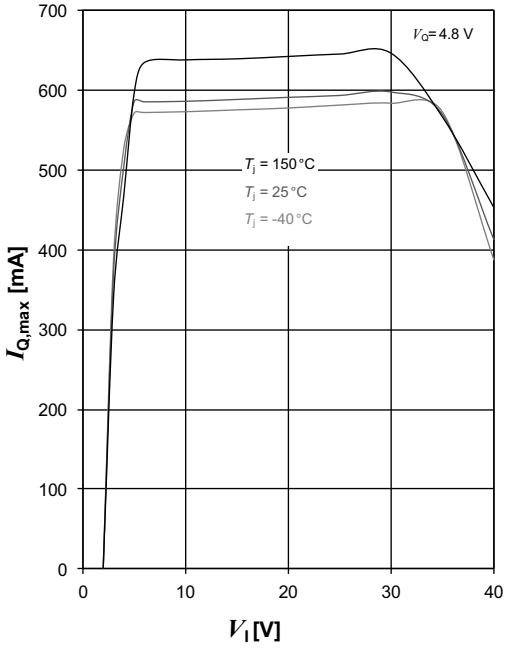
Dropout voltage V_{dr} versus junction temperature T_j (TLF80511TFV50)



Dropout voltage V_{dr} versus output current I_Q (TLF80511TFV50)

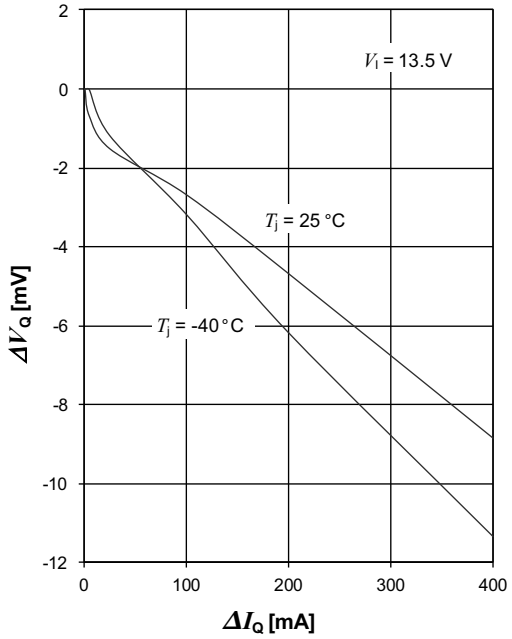


Maximum output current I_Q versus input voltage V_I (TLF80511TFV50)

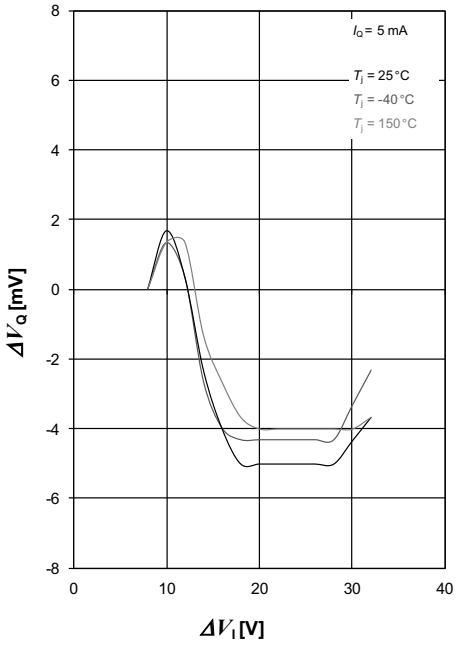


Block description and electrical characteristics

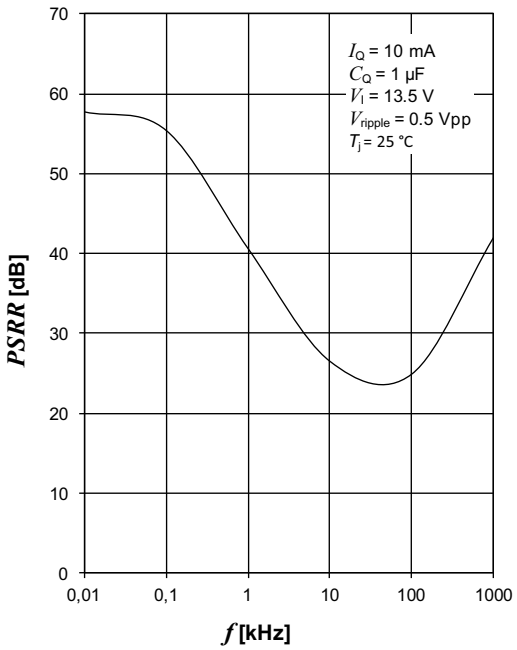
Load regulation $\Delta V_{Q,load}$ versus output current change ΔI_Q



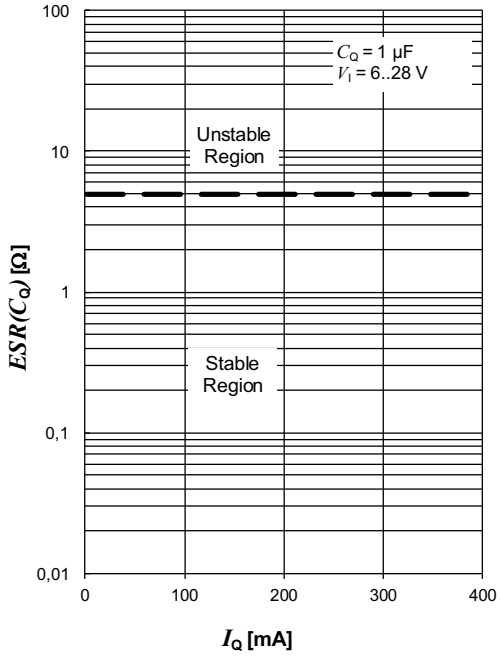
Line regulation $\Delta V_{Q,line}$ versus input voltage ΔV_I



Power supply ripple rejection versus frequency (TLF80511TFV50)

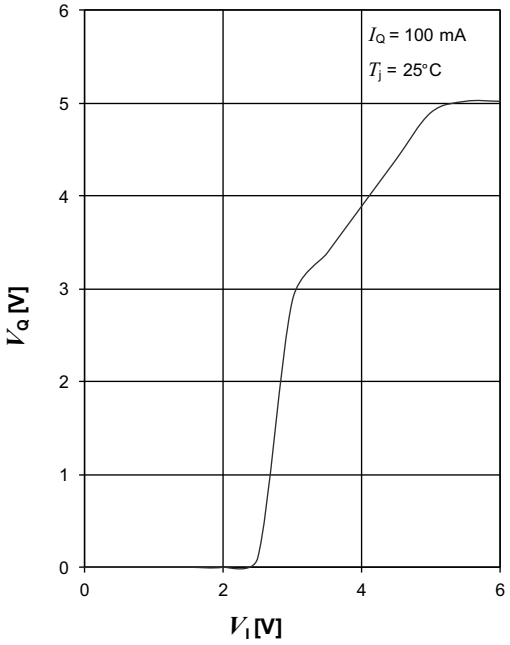


Stability region: equivalent serial resistor $ESR(C_Q)$ versus output current I_Q



Block description and electrical characteristics

Output voltage V_Q versus input voltage V_I (TLF80511TFV50)



4.3 Current consumption

Table 6 Electrical characteristics: current consumption

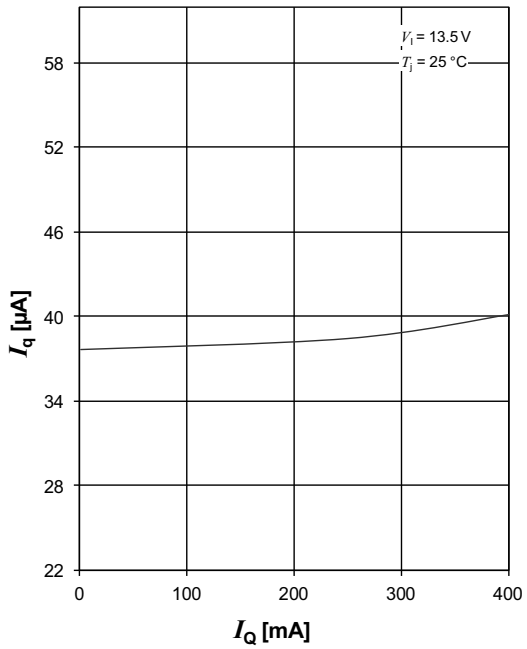
V_I = 13.5 V; T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I - I_Q$	I_q	–	38	46	µA	I_Q = 0.05 mA T_j < 25°C	P_5.3.1
Current consumption $I_q = I_I - I_Q$	I_q	–	–	75	µA	I_Q = 0.05 mA T_j < 125°C	P_5.3.2
Current consumption $I_q = I_I - I_Q$	I_q	–	67	80	µA	1) I_Q = 400 mA T_j < 125°C	P_5.3.3

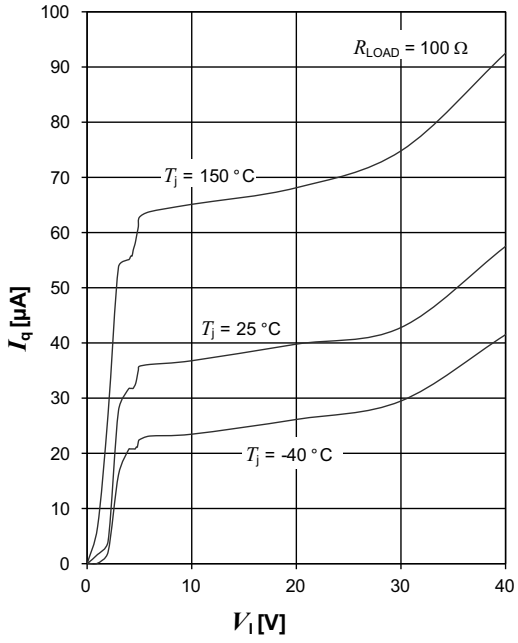
1) Not subject to production test, specified by design.

4.4 Typical performance characteristics: current consumption

Current consumption I_q versus output current I_Q



Current consumption I_q versus input voltage V_I



5 Application information

Note: The following information is given as a hint for the implementation of the device only and should not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

5.1 Application diagram

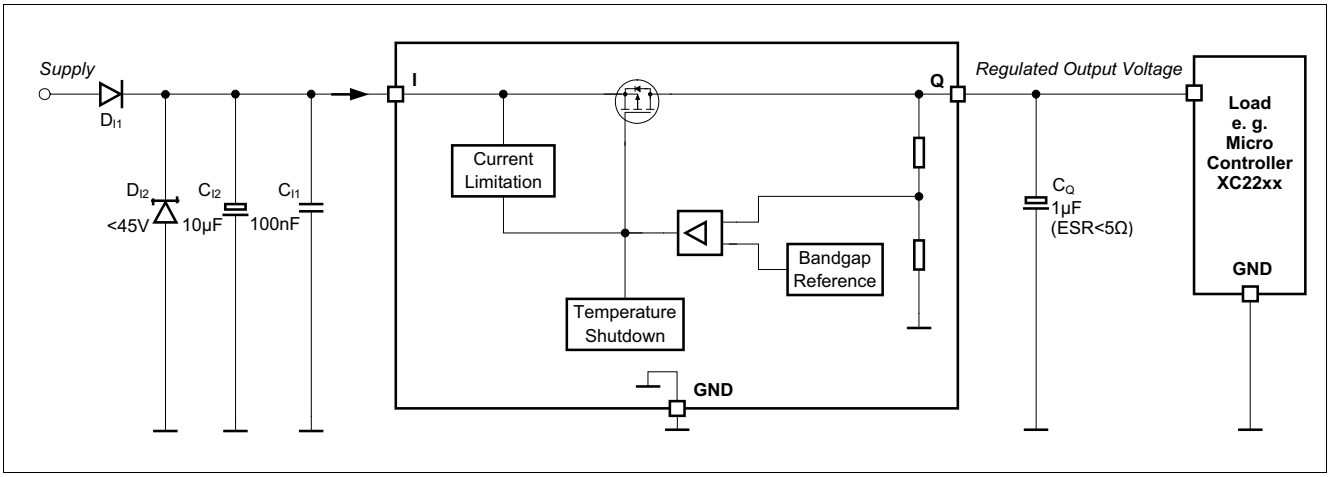


Figure 4 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

5.2 Selection of external components

5.2.1 Input pin

The typical input circuitry for a linear voltage regulator is shown in **Figure 4**.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line, for example, ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high-energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to overvoltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in order to protect the voltage regulator against external disturbances and damages.

5.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **Table 3**. The graph **Stability region: equivalent serial resistor ESR(C_Q) versus output current I_Q** shows the stable operation range of the device.

Application information

TLF80511TF is designed to be stable with extremely low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

5.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (5.1)$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a)/P_D \quad (5.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation, the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **Table 4**.

Example

Application conditions:

V_I = 13.5 V

V_Q = 5 V

I_Q = 150 mA

T_a = 85°C

Calculation of $R_{thJA,max}$:

$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$ ($V_I \times I_q$ can be neglected because of very low I_q)

$= (13.5\ V - 5\ V) \times 150\ mA$

$= 1.275\ W$

$R_{thJA,max} = (T_{j,max} - T_a) / P_D$

$= (150°C - 85°C) / 1.275\ W = 50.98\ K/W$

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 50.98 K/W. According to **Table 4**, at least 600 mm^2 of heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

5.4 Reverse polarity protection

TLF80511TF is not self protected against reverse polarity faults and must be protected by external components against negative supply voltages. An external reverse polarity diode is needed. The absolute maximum ratings of the device as specified in **Table 2** must be kept.

5.5 Further application information

For further information you may contact **http://www.infineon.com**.

6 Package information

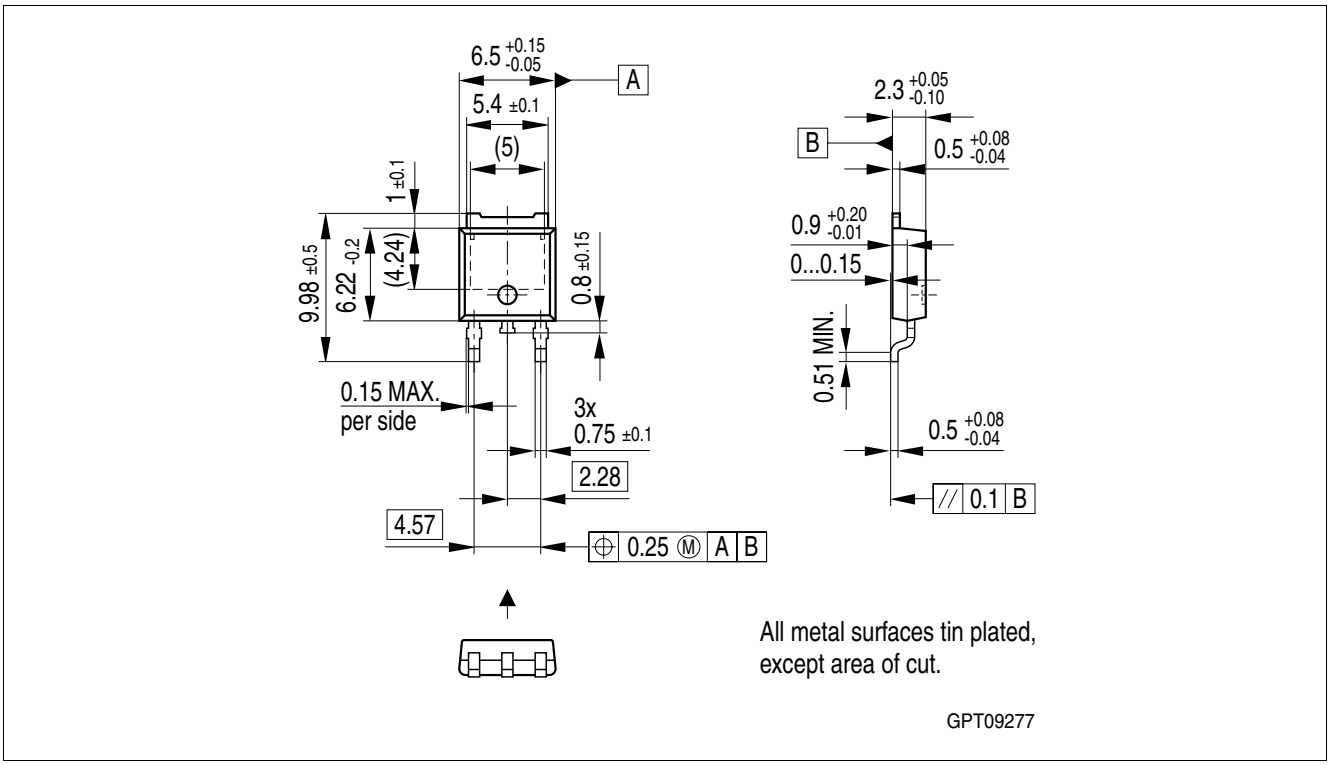


Figure 5 PG-TO252-3[1)]

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

7 Revision history

Revision	Date	Changes
1.01	2024-04-20	Updated template and layout Editorial changes
1.0	2014-01-28	Datasheet - Initial version