

Ultracompact, 1.5 A Thermoelectric Cooler (TEC) Controller

Data Sheet

ADN8834

FEATURES

- Patented high efficiency single inductor architecture
- Integrated low $R_{DS(ON)}$ MOSFETs for the TEC controller
- TEC voltage and current operation monitoring
- No external sense resistor required
- Independent TEC heating and cooling current limit settings
- Programmable maximum TEC voltage
- 2.0 MHz PWM driver switching frequency
- External synchronization
- Two integrated, zero drift, rail-to-rail chopper amplifiers
- Capable of NTC or RTD thermal sensors
- 2.50 V reference output with 1% accuracy
- Temperature lock indicator
- Available in a 25-ball, 2.5 mm × 2.5 mm WLCSP or in a 24-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- TEC temperature control
- Optical modules
- Optical fiber amplifiers
- Optical networking systems
- Instruments requiring TEC temperature control

GENERAL DESCRIPTION

The ADN8834 is a monolithic TEC controller with an integrated TEC controller. It has a linear power stage, a pulse-width modulation (PWM) power stage, and two zero-drift, rail-to-rail operational amplifiers. The linear controller works with the PWM driver to control the internal power MOSFETs in an H-bridge configuration. By measuring the thermal sensor feedback voltage and using the integrated operational amplifiers as a proportional integral differential (PID) compensator to condition the signal, the ADN8834 drives current through a TEC to settle the temperature of a laser diode or a passive component attached to the TEC module to the programmed target temperature.

The ADN8834 supports negative temperature coefficient (NTC) thermistors as well as positive temperature coefficient (PTC) resistive temperature detectors (RTD). The target temperature is set as an analog voltage input either from a digital-to-analog converter (DAC) or from an external resistor divider.

FUNCTIONAL BLOCK DIAGRAM

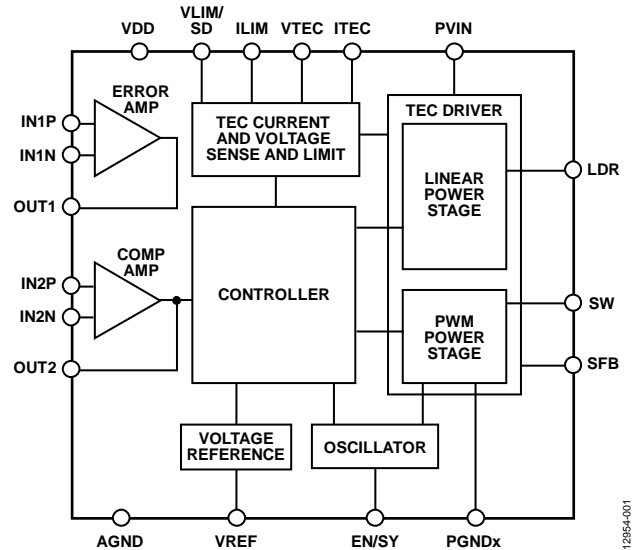


Figure 1.

The temperature control loop of the ADN8834 is stabilized by PID compensation utilizing the built in, zero drift chopper amplifiers. The internal 2.50 V reference voltage provides a 1% accurate output that is used to bias a thermistor temperature sensing bridge as well as a voltage divider network to program the maximum TEC current and voltage limits for both the heating and cooling modes. With the zero drift chopper amplifiers, extremely good long-term temperature stability is maintained via an autonomous analog temperature control loop.

Table 1. TEC Family Models

Device No.	MOSFET	Thermal Loop	Package
ADN8831	Discrete	Digital/analog	LFCSP (CP-32-7)
ADN8833	Integrated	Digital	WLCSP (CB-25-7), LFCSP (CP-24-15)
ADN8834	Integrated	Digital/analog	WLCSP (CB-25-7), LFCSP (CP-24-15)

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

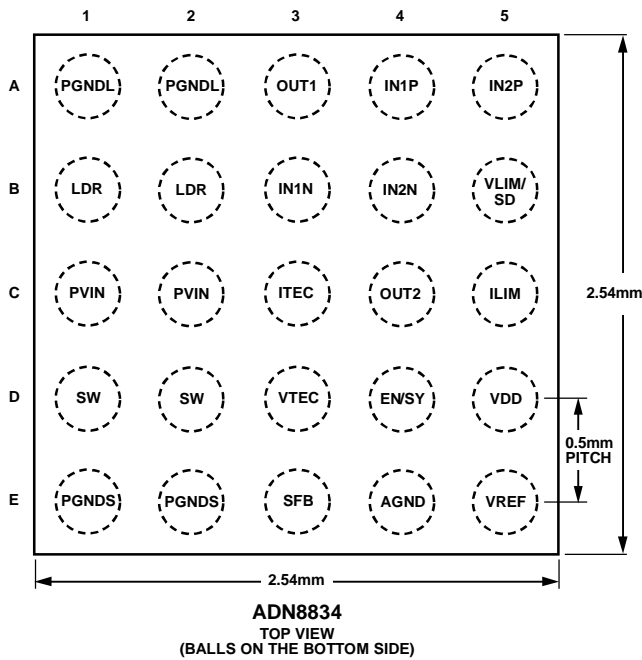
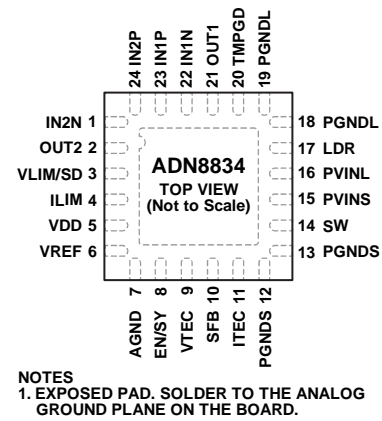


Figure 2. WLCSP Pin Configuration (Top View)



NOTES
1. EXPOSED PAD. SOLDER TO THE ANALOG GROUND PLANE ON THE BOARD.

12954-200

Figure 3. LFCSP Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.		Mnemonic	Description
WLCSP	LFCSP		
A1, A2	18, 19	PGNDL	Power Ground of the Linear TEC Controller.
N/A ¹	20	TMPGD	Temperature Good Output.
A3	21	OUT1	Output of the Error Amplifier.
A4	23	IN1P	Noninverting Input of the Error Amplifier.
A5	24	IN2P	Noninverting Input of the Compensation Amplifier.
B1, B2	17	LDR	Output of the Linear TEC Controller.
B3	22	IN1N	Inverting Input of the Error Amplifier.
B4	1	IN2N	Inverting Input of the Compensation Amplifier.
B5	3	VLIM/SD	Voltage Limit/Shutdown. This pin sets the cooling and heating TEC voltage limits. When this pin is pulled low, the device shuts down.
C1, C2	N/A ¹	PVIN	Power Input for the TEC Controller.
N/A ¹	16	PVINL	Power Input for the Linear TEC Driver.
N/A ¹	15	PVINS	Power Input for the PWM TEC Driver.
C3	11	ITEC	TEC Current Output.
C4	2	OUT2	Output of the Compensation Amplifier.
C5	4	ILIM	Current Limit. This pin sets the TEC cooling and heating current limits.
D1, D2	14	SW	Switch Node Output of the PWM TEC Controller.
D3	9	VTEC	TEC Voltage Output.
D4	8	EN/SY	Enable/Synchronization. Set this pin high to enable the device. An external synchronization clock input can be applied to this pin.
D5	5	VDD	Power for the Controller Circuits.
E1, E2	12, 13	PGNDS	Power Ground of the PWM TEC Controller.
E3	10	SFB	Feedback of the PWM TEC Controller Output.
E4	7	AGND	Signal Ground.
E5	6	VREF	2.5 V Reference Output.
N/A ¹	0	EPAD	Exposed Pad. Solder to the analog ground plane on the board.