bq24133 1.6-MHz Synchronous Switched-Mode Li-Ion and Li-Polymer Stand-Alone Battery Charger With Integrated MOSFETs and Power Path Selector

1 Features

- 1.6-MHz Synchronous Switched-Mode Charger With 2.5-A Integrated N-MOSFETs
- Up to 92% Efficiency
- 30-V Input Rating With Adjustable Overvoltage Protection
  - 4.5-V to 17-V Input Operating Voltage
- Battery Charge Voltage
  - 1-Cell, 2-Cell, or 3-Cell With 4.2 V/Cell
- High Integration
  - Automatic Power Path Selector Between Adapter and Battery
  - Dynamic Power Management
  - Integrated 20-V Switching MOSFETs
  - Integrated Bootstrap Diode
  - Internal Digital Soft Start
- Safety
  - Thermal Regulation Loop Throttles Back Current to Limit T_J = 120°C
  - Thermal Shutdown
  - Battery Thermistor Sense Hot/Cold Charge Suspend and Battery Detect
  - Adjustable Input Overvoltage Protection
  - Cycle-by-Cycle Current Limit
- Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% Charge Current Regulation
  - ±6% Input Current Regulation
- <15-µA Battery Current With Adapter Removed
- <1.5-mA Input Current With Adapter Present and Charge Disabled Package

2 Applications

- Tablet PCs
- Netbooks and Ultra-Mobile Computers
- Portable Data Capture Terminals
- Portable Printers
- Medical Diagnostics Equipment
- Battery Bay Chargers
- Battery Backup Systems

3 Description

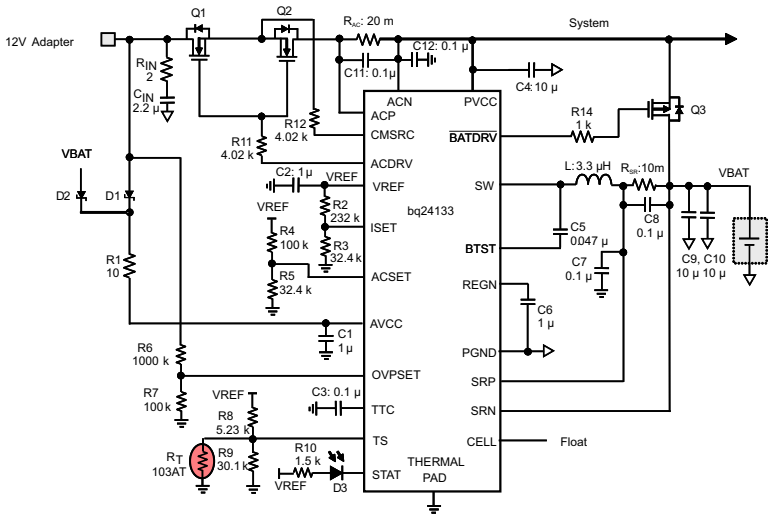
The bq24133 device is a highly integrated stand-alone Li-Ion and Li-Polymer switched-mode battery charger with two integrated N-channel power MOSFETs. The device offers a constant-frequency synchronous PWM controller with high accuracy regulation of input current, charge current, and voltage. The bq24133 closely monitors the battery pack temperature to allow charge only in a preset temperature window. The bq24133 charges one, two, or three cells (selected by CELL pin) at a fixed 4.2 V/cell.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24133	VQFN (24)	5.50 mm × 3.50 mm

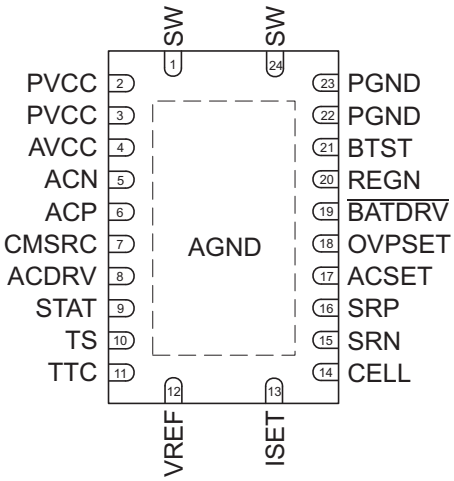
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



7 Pin Configuration and Functions

RGY Package
24-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ACDRV	8	O	AC adapter to system switch driver output. Connect to 4-kΩ resistor then to the gate of the ACFET N-channel power MOSFET and the reverse conduction blocking N-channel power MOSFET. Connect both FETs as common-source. The internal gate drive is asymmetrical, allowing a quick turnoff and slower turnon in addition to the internal break-before-make logic with respect to the $\overline{\text{BATDRV}}$.
ACN	5	I	Adapter current sense resistor negative input. A 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from ACN pin to AGND for common-mode filtering.
ACP	6	P/I	Adapter current sense resistor positive input. A 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from ACP pin to AGND for common-mode filtering.
ACSET	17	I	Input current set point. Use a voltage divider from VREF to ACSET to AGND to set this value: $I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}}$
AGND	Thermal Pad	P	Exposed pad beneath the IC. Always solder Thermal Pad to the board, and have vias on the Thermal Pad plane star-connecting to AGND and ground plane for high-current power converter. It dissipates the heat from the IC.
AVCC	4	P	IC power positive supply. Place a 1-µF ceramic capacitor from AVCC to AGND and place it as close as possible to IC. Place a 10-Ω resistor from input side to AVCC pin to filter the noise. For 5-V input, a 5-Ω resistor is recommended.
$\overline{\text{BATDRV}}$	19	O	Battery discharge MOSFET gate driver output. Connect to 1-kΩ resistor to the gate of the BATFET P-channel power MOSFET. Connect the source of the BATFET to the system load voltage node. Connect the drain of the BATFET to the battery pack positive node. The internal gate drive is asymmetrical to allow a quick turnoff and slower turnon, in addition to the internal break-before-make logic with respect to ACDRV.
BTST	21	P	PWM high-side driver positive supply. Connect the 0.047-µF bootstrap capacitor from SW to BTST.
CELL	14	I	Cell selection pin. Set CELL pin LOW for 1-cell, Float for 2-cell (0.8 V - 1.8 V), and HIGH for 3-cell with a fixed 4.2 V per cell.
CMSRC	7	O	Connect to common source of N-channel ACFET and reverse blocking MOSFET (RBFET). Place 4-kΩ resistor from CMSRC pin to the common source of ACFET and RBFET to control the turnon speed. The resistance between ACDRV and CMSRC should be 500 kΩ or bigger.