SGM37604A
Highly Efficient 4-String White LED Driver

GENERAL DESCRIPTION

The SGM37604A is an ultra-compact, highly efficient, 4-string white-LED driver designed for LCD display backlighting. The device operates over the 3V to 24V input voltage, it can power up to 8 series LEDs at up to 40mA per string. An adaptive current regulation method allows for different LED voltages in each string while maintaining current regulation.

The LED current is adjusted via an I^2C interface or through a logic level PWM input. The SGM37604A is available in Green WLCSP-1.78×1.36-12B and TDFN-3×3-12L packages. It operates over the -40℃ to +85℃ temperature range.

APPLICATIONS

Power Source for Smart Phone and Tablet Backlighting

FEATURES

- **11% Matched Current Sinks across Process, Voltage and Temperature at I_{LED} = 12.21μA**
- **1% Matched Current Sinks across Process, Voltage and Temperature at I_{LED} = 25mA**
- **11% Current Sink Accuracy across Process, Voltage and Temperature at I_{LED} = 12.21μA**
- **3% Current Sink Accuracy across Process, Voltage and Temperature at I_{LED} = 25mA**
- **12-Bit Dimming Resolution**
- **Up to 90% Solution Efficiency**
- **Drive from 1 to 4 Parallel LED Strings at Up to 29.5V**
- **PWM Dimming Input**
- **I^2C Programmable**
- **Phase Shift Function**
- **Hybrid PWM + Current Dimming for Higher LED Driver Optical Efficiency**
- **1.2MHz Switching Frequency**
- **Low EMI by Conducting Ringing Cancelling**
- **Over-Voltage Protection**
- **Over-Current Protection**
- **Thermal Shutdown Protection**

TYPICAL APPLICATION

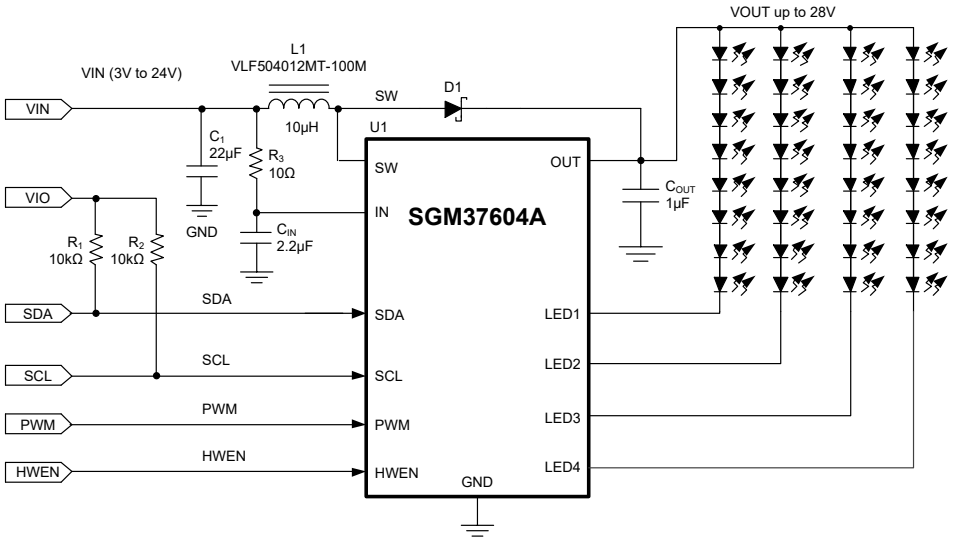


Figure 1. Typical Application

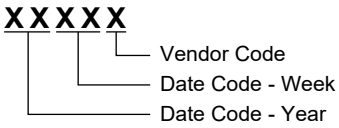
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM37604A	WLCSP-1.78×1.36-12B	-40℃ to +85℃	SGM37604AYG/TR	XXXXX GX4	Tape and Reel, 3000
	TDFN-3×3-12L	-40℃ to +85℃	SGM37604AYTDF12G/TR	SGM B4DF XXXXX	Tape and Reel, 4000

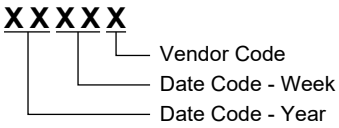
MARKING INFORMATION

NOTE: XXXXX = Date Code and Vendor Code.

WLCSP-1.78×1.36-12B



TDFN-3×3-12L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN ..... -0.3V to 28.6V
OUT ..... -0.3V to 40V
SW ..... -0.3V to 40V
LED1, LED2, LED3, LED4 ..... -0.3V to 17V
HWEN, PWM, SDA, SCL ..... -0.3V to 6V
Package Thermal Resistance
WLCSP-1.78×1.36-12B, θ_{JA} ..... 82℃/W
TDFN-3×3-12L, θ_{JA} ..... 50℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
MM 200V
CDM 500V

RECOMMENDED OPERATING CONDITIONS

IN ..... 3V to 24V
OUT ..... 0V to 30.5V
SW ..... 0V to 30.5V
LED1, LED2, LED3, LED4 ..... 0V to 12V
HWEN, PWM, SDA, SCL ..... 0V to 5.5V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

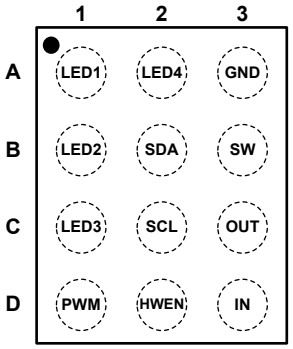
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

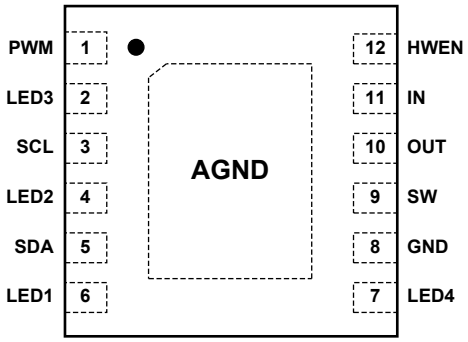
PIN CONFIGURATION

SGM37604A (TOP VIEW)



WLCSP-1.78×1.36-12B

SGM37604A (TOP VIEW)



TDFN-3×3-12L

PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
WLCSP-1.78×1.36-12B	TDFN-3×3-12L			
A1	6	LED1	I	Input Pin to Current Sink 1. The boost converter regulates the minimum voltage between LED1, LED2, LED3, LED4 to V_{HR}.
A2	7	LED4	—	Input Pin to Current Sink 4. The boost converter regulates the minimum voltage between LED1, LED2, LED3, LED4 to V_{HR}
A3	8	GND	O	Ground.
B1	4	LED2	I	Input Pin to Current Sink 2. The boost converter regulates the minimum voltage between LED1, LED2, LED3, LED4 to V_{HR}.
B2	5	SDA	I/O	Data I/O for I^2C-Compatible Interface.
B3	9	SW	I	Drain Connection for Internal Low-side NFET, and Anode Connection for External Schottky Diode.
C1	2	LED3	I	Input Pin to Current Sink 3. The boost converter regulates the minimum voltage between LED1, LED2, LED3, LED4 to V_{HR}.
C2	3	SCL	I	Clock Input for I^2C-Compatible Interface.
C3	10	OUT	I	OUT Serves as The Sense Point for Over-Voltage Protection. Connect OUT to the positive pin of the output capacitor.
D1	1	PWM	I	Logic Level Input for PWM Current Control.
D2	12	HWEN	I	Hardware Enable Input. Drive HWEN high to bring the device out of shutdown and allow I^2C writes or PWM control.
D3	11	IN	I	Input Voltage Connection. Bypass IN to GND with a minimum 2.2μF ceramic capacitor.
—	Exposed Pad	AGND	—	Power Ground Exposed Pad. Must be connected to ground plane.

NOTE: I: input; O: output; I/O: input or output.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
BOOST							
LED Current Matching I_{LED1} to I_{LED2} to I_{LED3} to I_{LED4}	I_{MATCH} (1)	I_{LED} = 12.21μA, V_{LED} = 300mV	+25℃		11		%
		I_{LED} = 25mA, V_{LED} = 180mV	+25℃		1		
Absolute Accuracy (I_{LED1}, I_{LED2}, I_{LED3}, I_{LED4})		I_{LED} = 12.21μA, V_{LED} = 300mV	+25℃		11		%
		I_{LED} = 25mA, V_{LED} = 180mV	+25℃		3		
Minimum LED Current (per string)	I_{LED_MIN}		+25℃		12.21		μA
Maximum LED Current (per string)	I_{LED_MAX}		+25℃		25		mA
Regulated Current Sink Headroom Voltage	V_{HR}	I_{LED} = 25mA	+25℃		180		mV
NMOS Switch On-Resistance	R_{NMOS}	I_{SW} = 250mA	+25℃		0.25	0.35	Ω
NMOS Switch Current Limit	I_{CL}		+25℃	1.7	2.2	2.7	A
Output Over-Voltage Protection	V_{OVP}		Full	28.5	29.5	30.5	V
OVP Hysteresis			+25℃		3		V
Switching Frequency	f_{SW}		Full	950	1200	1400	kHz
Maximum Boost Duty Cycle	D_{MAX}		Full	90	94		%
Shutdown Current	I_{SHDN}	Chip enable bit = 0, SDA = SCL = IN or GND	+25℃		0.5	1.5	μA
Thermal Shutdown	T_{SD}				160		℃
Thermal Shutdown Hysteresis					20		
PWM INPUT							
PWM Dimming Frequency Range	DFR		+25℃	20		100	kHz
Turn-On Delay from Shutdown to Backlight On	$t_{START-UP}$	PWM input active, PWM = logic high, HWEN input from low to high, f_{PWM} = 20kHz (50% duty cycle)	+25℃		10		ms
Input Logic High	V_{IH}	HWEN, SCL, SDA, PWM inputs	Full	1.4			V
Input Logic Low	V_{IL}	HWEN, SCL, SDA, PWM inputs	Full			0.4	

NOTE:

1. LED Current Matching between strings is given as the worst case matching between any two strings. Matching is calculated as $(I_{LEDX} - I_{LEDY})/(I_{LEDX} + I_{LEDY}) \times 100$.

I²C TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCL Clock Period	t_1	2.5			μs
Data in Setup Time to SCL High	t_2	100			ns
Data Out Stable After SCL Low	t_3	0			ns
SDA Low Setup Time to SCL Low (Start)	t_4	100			ns
SDA High Hold Time After SCL High (Stop)	t_5	100			ns

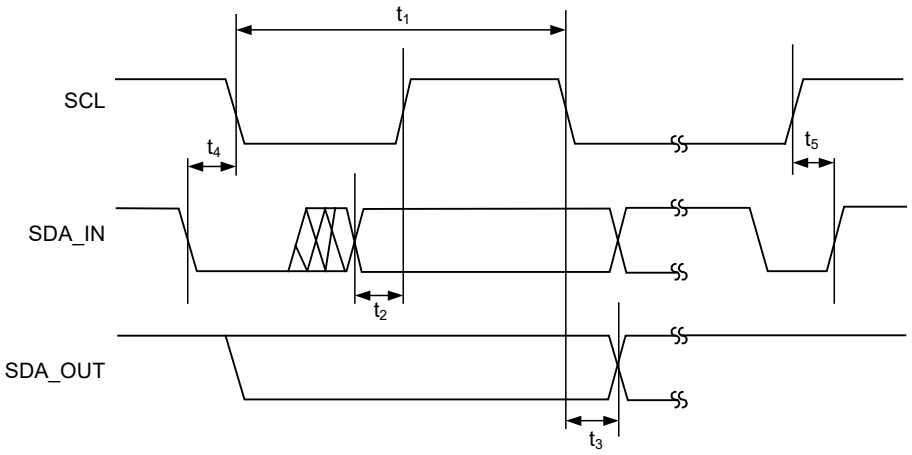
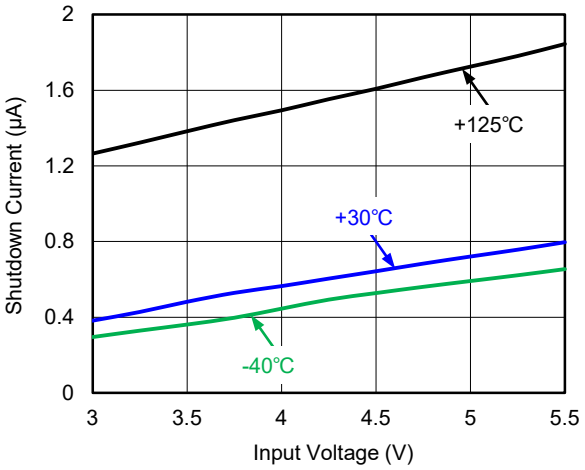


Figure 2. I²C Timing

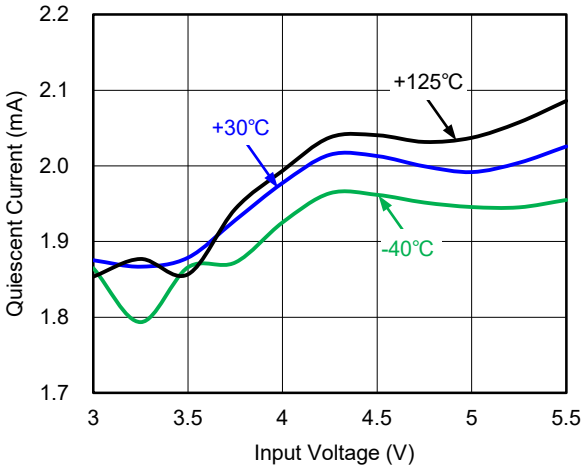
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_{IN} = 3.7V, L1 = 10μH (VLF504012MT-100M), D1 = NSR0530P2T5G, unless otherwise noted.

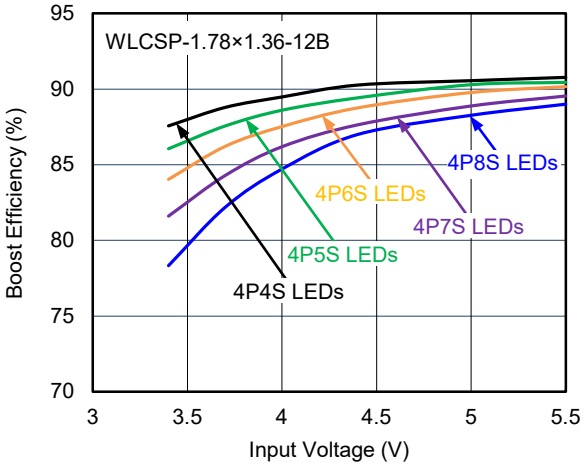
Shutdown Current vs. Input Voltage



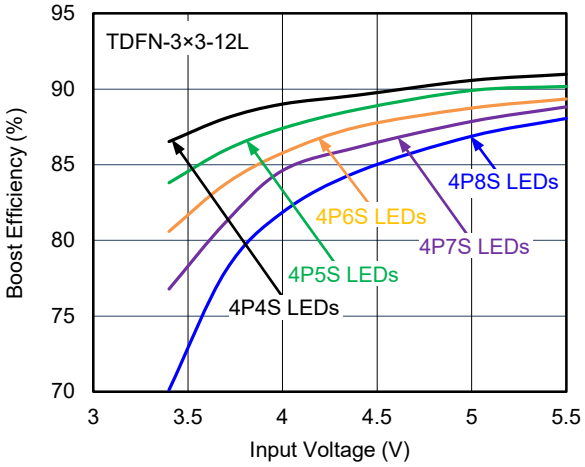
Quiescent Current (Switching) vs. Input Voltage



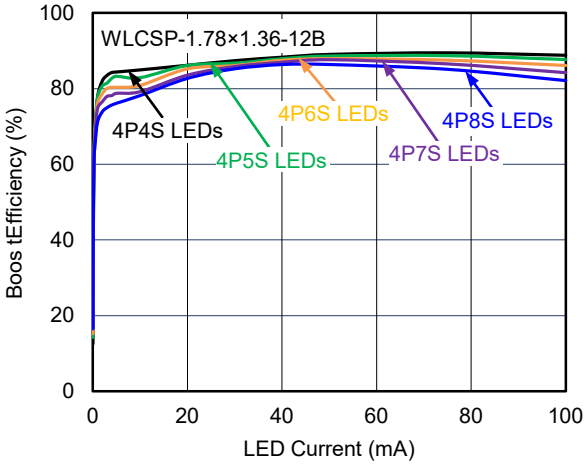
Boost Efficiency vs. Input Voltage



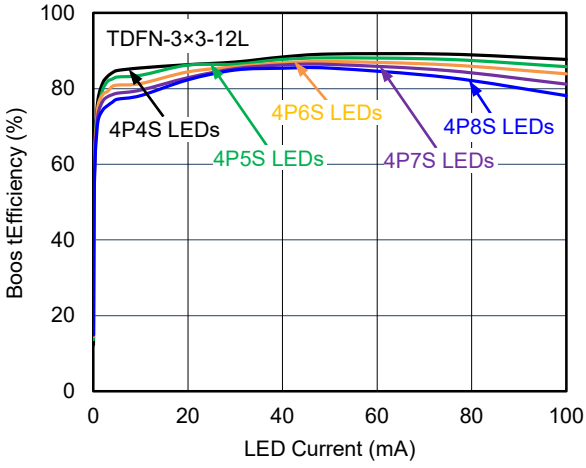
Boost Efficiency vs. Input Voltage



Boost Efficiency vs. LED Current



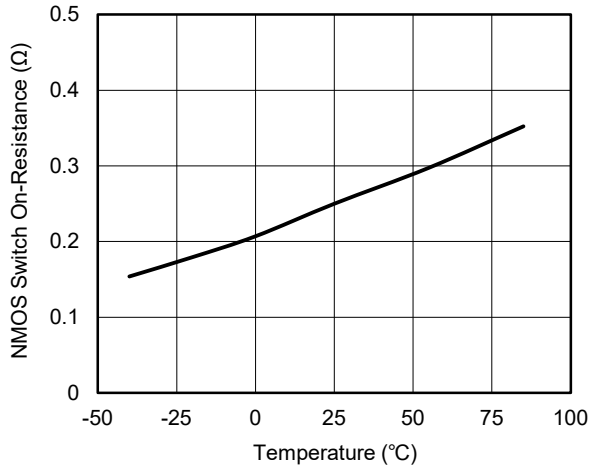
Boost Efficiency vs. LED Current



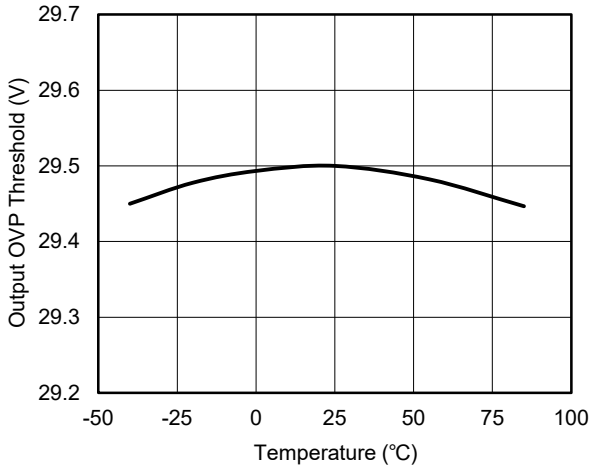
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_{IN} = 3.7V, L1 = 10μH (VLF504012MT-100M), D1 = NSR0530P2T5G, unless otherwise noted.

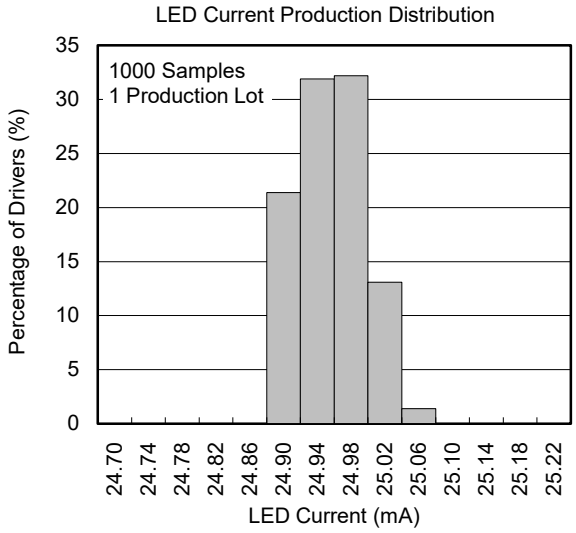
NMOS Switch On-Resistance vs. Temperature



Output Over-Voltage Protection Threshold vs. Temperature



LED Current Production Distribution



FUNCTIONAL BLOCK DIAGRAM

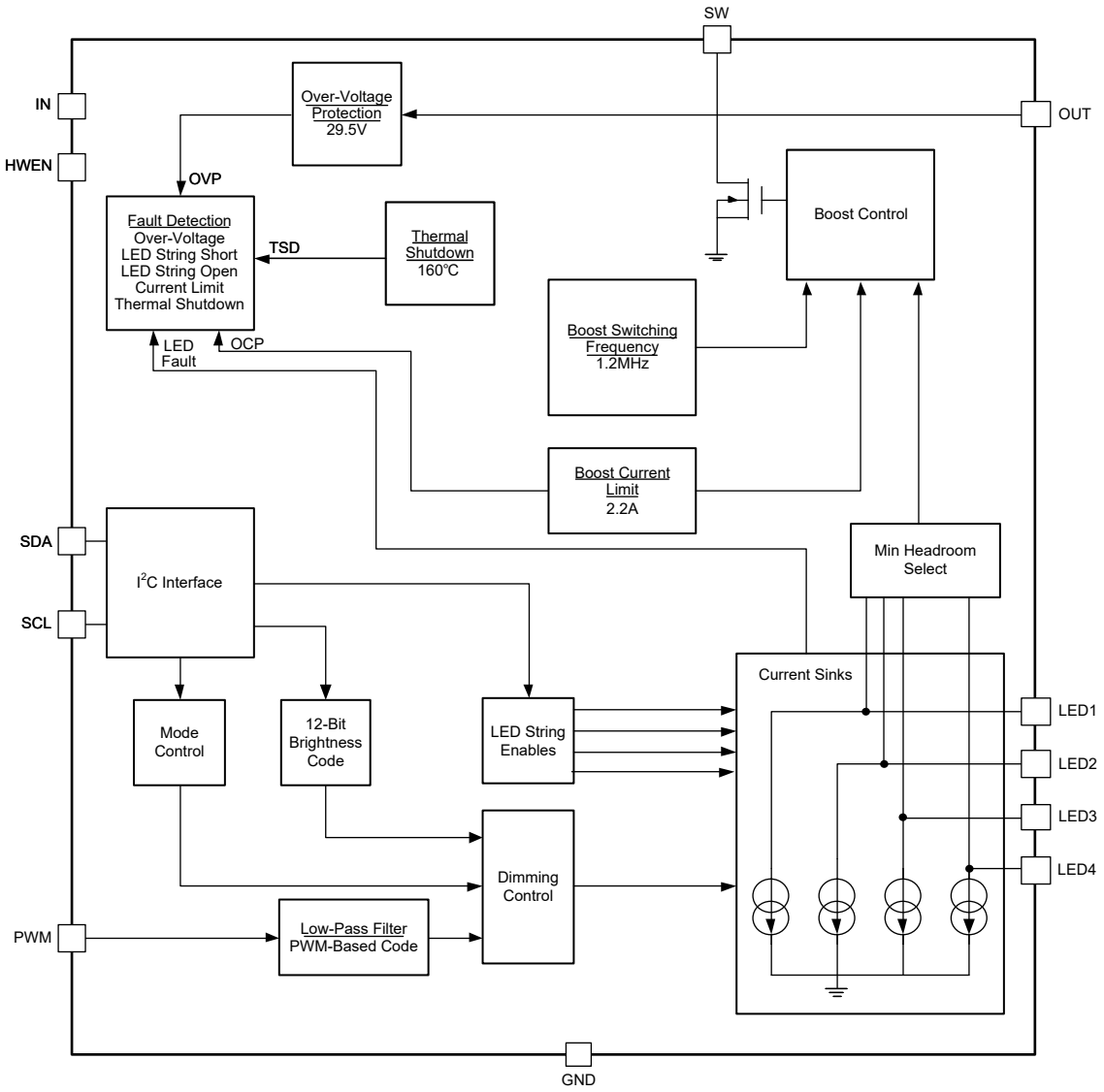


Figure 3. Functional Block Diagram

REGISTER MAPS

Note: Read of Reserved (R) register returns 0/1 as below.

Table 1. Software Reset (0x01)

Bits[7:1]	Software Reset Bit[0]
R (0000000)	0 = Normal Operation 1 = Device Reset (automatically resets back to 0)

Table 2. Enable (0x10)

Bits[7:5]	LED4 Enable Bit[4]	LED3 Enable Bit[3]	LED2 Enable Bit[2]	LED1 Enable Bit[1]	Device Enable Bit[0]
R (000)	0 = Disabled 1 = Enabled (Default)	0 = Disabled 1 = Enabled (Default)	0 = Disabled 1 = Enabled (Default)	0 = Disabled 1 = Enabled (Default)	0 = Disabled 1 = Enabled (Default)

Table 3. Brightness Control (0x11)

Bit[7]	Brightness Mode Bits[6:5]	Ramp Enable Bit[4]	Bits[3:0]
R (0)	00 = Brightness Register Only 01 = PWM Duty Cycle Only 10/11 = (Brightness Register × PWM Duty Cycle) (Default = 11)	0 = Ramp Disabled (Default) 1 = Ramp Enabled	R (0101)

Table 4. Brightness Register LSBs (0x1A)

Bits[7:4]	I^2C Brightness Code (LSB) Bits[3:0]
R (1111)	This is the lower 4 bits of the 12-bit brightness code (Default = 1111).

Table 5. Brightness Register MSBs (0x19)

I^2C Brightness Code (MSB) Bits [7:0]
This is the upper 8 bits of the 12-bit brightness code (Default = 11111111).

Table 6. Fault Flags (0x1F)

Reserved Bits[7:5]	LED Open Fault Bit[4]	LED Short Fault Bit[3]	TSD Fault Bit[2]	OCP Fault Bit[1]	OVP Fault Bit[0]
R (000)	1 = LED String Open Fault	1 = LED Short Fault	1 = Thermal Shutdown Fault	1 = Current Limit Fault	1 = Output Over-Voltage Fault

Table 7. Maximum LED Current (0x1B)

Reserved Bits[7:2]	Maximum LED Current Bit[1:0]
R (000000)	00 = Maximum LED Current of 25mA (Default) 01 = Maximum LED Current of 30mA 10 = Maximum LED Current of 35mA 11 = Maximum LED Current of 40mA

DETAILED DESCRIPTION

The SGM37604A is an inductive boost plus 4 current sink white-LED driver designed for powering from 1 to 4 strings of white LEDs used in display backlighting. The device operates over the 3V to 24V input voltage range. The 12-bit LED current is set via an I^2C interface, via a logic level PWM input, or a combination of both.

Enabling the SGM37604A

The SGM37604A has a logic level input HWEN which serves as the master enable/disable for the device. When HWEN is low the device is disabled, the registers are reset to their default state, the I^2C bus is inactive, and the device is in a low-power shutdown mode. When HWEN is forced high the device is enabled, and I^2C writes are allowed to the device.

Current Sink Enable

Each current sink in the device has a separate enable input. This allows for a 1-string, 2-string, 3-string or 4-string application. The default is with 4 strings enabled. Once the correct LED string configuration is programmed, the device can be enabled by writing the chip enable bit high (register 0x10 bit[0]), and then either enabling PWM and driving PWM high, or writing a non-zero code to the brightness registers.

The default setting for the device is with the chip enable bit set to 1, PWM input enabled. Therefore, once HWEN is driven high, the device enters the standby state and actively monitors the PWM input. After a non-zero PWM duty cycle is detected the SGM37604A converts the duty cycle information to a PWM-based code by an internal low-pass filter for brightness dimming. This allows for operation of the device in a stand-alone configuration without the need for any I^2C writes.

Figure 4 and Figure 5 describe the start-up timing for operation with both PWM controlled current and with I^2C controlled current.

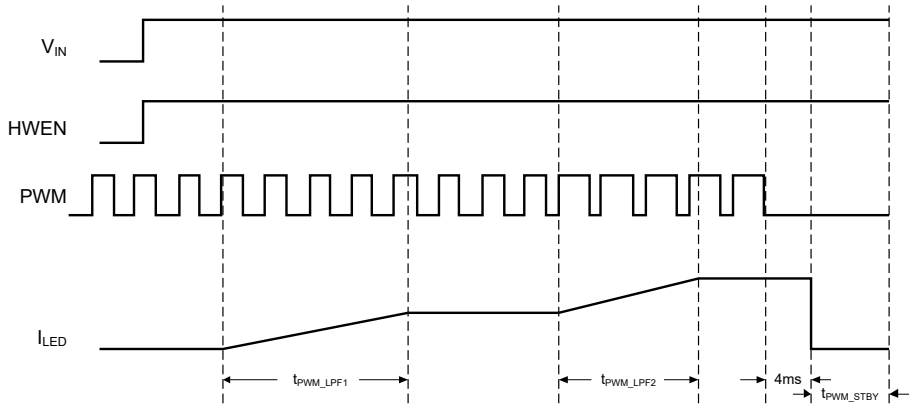


Figure 4. Enabling the SGM37604A via PWM

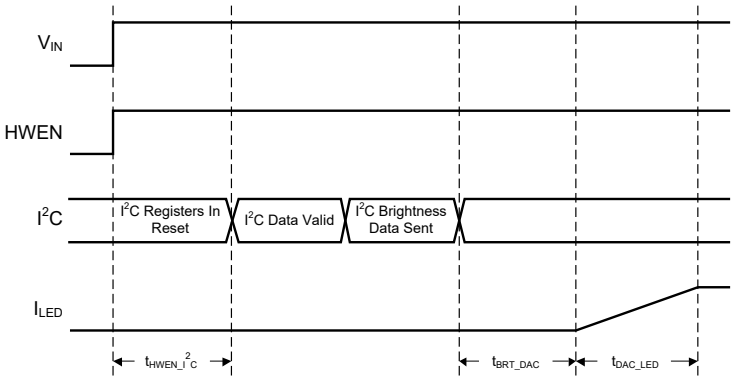


Figure 5. Enabling the SGM37604A via I^2C

DETAILED DESCRIPTION (continued)

SGM37604A Start-Up

The SGM37604A can be enabled or disabled in various ways. When disabled, the device is considered shutdown, and the quiescent current drops to I_{SHDN}. When the device is in standby, it returns to the I_{SHDN} current level retaining all programmed register values.

Table 8 describes the different operating states for the SGM37604A.

Regulated Headroom Voltage

If the LEDs connected to LED1 require 12V, the LEDs connected to LED2 require 12.5V, the LEDs connected to LED3 require 12.7V and the LEDs connected to LED4 require 13V at the programmed current, then the voltage at LED1 is V_{HR} + 1V, the voltage at LED2 is V_{HR} + 0.5V, the voltage at LED3 is V_{HR} + 0.3V, and the voltage at LED4 is regulated at V_{HR}. In other words, the boost makes the cathode of the highest voltage LED string the regulation point.

Table 8. SGM37604A Operating Modes

LED STRING ENABLES 0x10 bits[4:1]	PWM INPUT	I²C BRIGHTNESS REGISTERS 0x1A bits[3:0] 0x19 bits[7:0]	BRIGHTNESS MODE 0x11 bits[6:5]	DEVICE ENABLE 0x10 bit[0]	LED CURRENT
XXXX	X	XXX	XX	0	Off, device disabled
0000	X	XXX	XX	1	Boost enabled, LED current disabled
At least one enabled	X	000	00	1	Off, device in standby
At least one enabled	X	Code > 000	00	1	See (1)
At least one enabled	0	XXX	01	1	Off, device in standby
At least one enabled	PWM Signal	XXX (2)	01	1	See (1)
At least one enabled	0	XXX	10 or 11	1	Off, device in standby
At least one enabled	X	000	10 or 11	1	Off, device in standby
At least one enabled	PWM Signal	Code > 000	10 or 11	1	See (1)

Note:

1. I_{LED} is calculated by the equations from Equation 1 to Equation 8 below in Brightness Control Modes.
2. Code is forbidden to set to 0.

Brightness Control Modes

The SGM37604A has 3 brightness control modes:

1. I²C Only (brightness mode 00)
2. PWM Only (brightness mode 01)
3. I²C × PWM (brightness mode 10 or 11)

I²C Only (Brightness Mode 00)

In brightness control mode 00 the I²C Brightness registers are in control of the LED current, and the PWM input is disabled. The brightness data (BRT) is the concatenation of the two brightness registers (4 LSBs) and (8 MSBs) (registers 0x1A and 0x19, respectively). The LED current only changes when the MSBs are written, meaning that to do a full 12-bit current change via I²C, first the 4 LSBs of 0x1A are written and then the 8 MSBs are written.

The 12-bit code (0 to 4095) is in control of the LED current as follows:

DETAILED DESCRIPTION (continued)

When the code is from 256 to 4095, the average LED current increases proportionally to the brightness code and follows the below relationship (see Figure 7).

When the code is an odd integer,

$$I_{LED\_AVG} = 12.21\mu A \times 0.5 \times (code - 1) \quad (1)$$

When the code is an even integer,

$$I_{LED\_AVG} = 12.21\mu A \times 0.5 \times code \quad (2)$$

Where:

I_{LED_AVG} = average LED current

When the code is from 16 to 255, the average LED current is calculated by Equation 1 and Equation 2 and the LED current is in current-to-PWM control (see Figure 7) with a constant maximum current, while the duty cycle changes following the code.

When the code is from 1 to 15, the average LED current increases exponentially to the brightness code and follows the relationship by Equation 3 (see Figure 7). The LED current is also in current-to-PWM control, and the duty cycle is 16/256 constantly, and the amplitude of current pulse is 16 times of its corresponding average current.

$$I_{LED\_AVG} = 12.21\mu A \times 1.149^{(code - 1)} \quad (3)$$

Code 1 programs the LED current to 12.21μA with 25mA maximum LED current. If the bits[1:0] are not set to all 0 in register 0x1B, the maximum LED current will increase and the minimum current (code = 1) will proportionally increase. Code 0 programs 0 current.

When bit[4] is set to 1 in register 0x11, ramp function is enabled. Then when bits[7:4] in registers 0x19 are not all 0 (codes from 256 to 4095), the ramp rate is 128μs/step. When bits[7:4] in registers 0x19 are all 0 (codes from 1 to 255), the ramp rate is 1024μs/step. For example, if the code is set from 2000 to 4001, I_{LED_AVG} will change from 12.21mA to 24.42mA, the corresponding ramp rate = 128μs/step, so the ramp time for I_{LED_AVG} = [(4001 - 1) × 0.5 - 2000 × 0.5] × 128μs = 128ms.

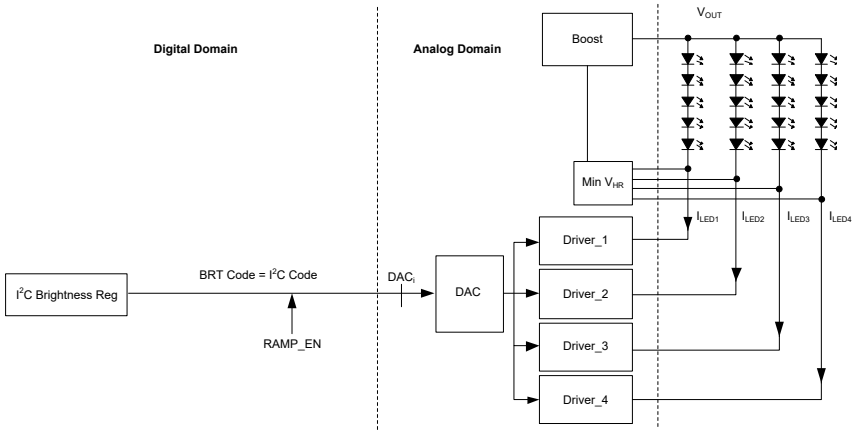


Figure 6. Brightness Control 00 (I²C Only)

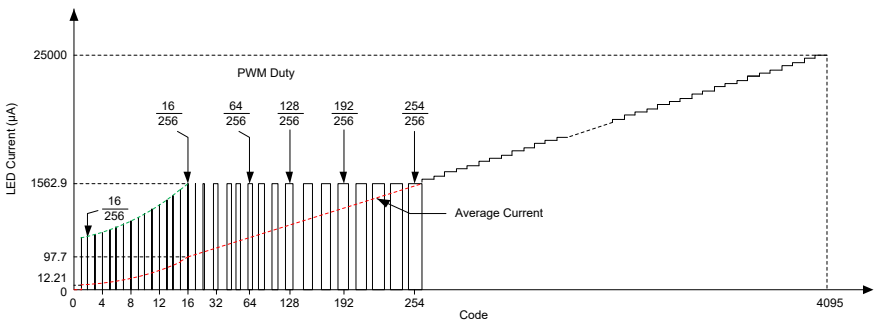


Figure 7. LED Current vs. Brightness Code (Mode 00)

DETAILED DESCRIPTION (continued)

PWM Only (Brightness Mode 01)

In brightness mode 01, only the PWM input sets the brightness. The I^2C code is ignored and forbidden to set to 0. The LED current is proportional with the PWM duty cycle and the maximum LED current is 25mA.

When the PWM pin is constantly high, the V_{REF} voltage is regulated to 2048mV typically. When the duty cycle of the input PWM signal is low, the regulation voltage is reduced, and the LED current is reduced; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and V_{REF} regulation voltage is given by Equation 4:

$$V_{REF} = Duty \times 2048mV \quad (4)$$

Where:
Duty = duty cycle of the PWM signal
2048mV = internal reference voltage

Then the value of V_{REF} is the PWM-based code for brightness dimming. The LED current increases proportionally to the brightness code and follows the relationship (see Figure 10):

$$I_{LED\_AVG} = 12.21\mu A \times code \quad (5)$$

This is valid from codes 1 to 2048. Code 0 programs 0 current. When the code < 16, the LED current is in current-to-PWM control. The duty cycle of the PWM is 1/8, and the amplitude of current pulse is 8 times of its corresponding average current. Figure 10 (a) shows the zoomed graph from codes 0 to 16 in Figure 10. There is no ramp function in this mode.

Thus, the user can easily control the WLED brightness by controlling the duty cycle of the PWM signal. The PWM frequency is in the range from 20kHz to 100kHz.

As shown in Figure 8, the IC chops up the internal 2048mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low-pass filter. SGM37604A regulation voltage is independent of the PWM logic voltage level which often has large variations.

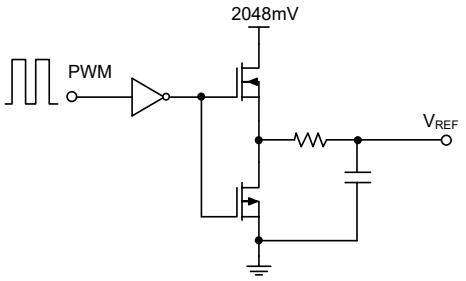


Figure 8. Programmable V_{REF} Using PWM Signal

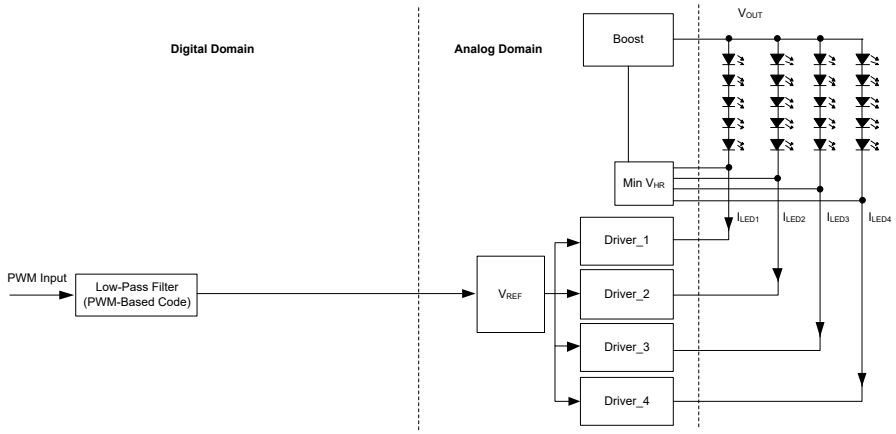


Figure 9. Brightness Control 01 (PWM Only)

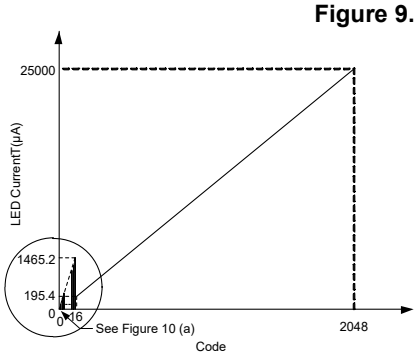


Figure 10. LED Current vs. Brightness Code (Mode 01)

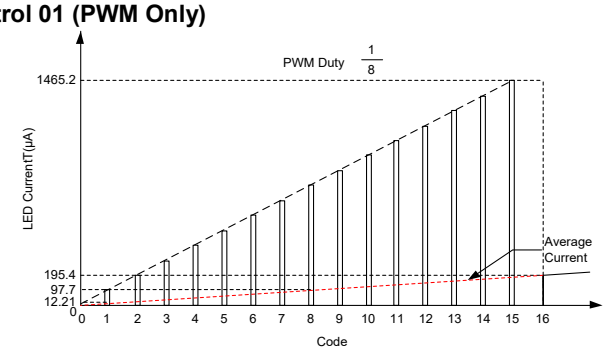


Figure 10 (a).

DETAILED DESCRIPTION (continued)

I²C + PWM (Brightness Mode 10 or 11)

In brightness control mode 10 or 11 both the I²C code and the PWM duty cycle control the LED current. The brightness code is calculated by PWM duty cycle and the I²C brightness code, and follows the relationship (see Figure 11):

When the I²C code is an odd integer,

BRT code = (I²C code - 1) × 0.5 × PWM duty cycle (6)

When the I²C code is an even integer,

BRT code = I²C code × 0.5 × PWM duty cycle (7)

Where:
BRT code = the brightness code
I²C codes are valid from 0 to 4095. The codes should be integers.

The average LED current increases proportionally to the brightness code and is calculated by Equation 8.

$$I_{LED\_AVG} = 12.21\mu A \times code \quad (8)$$

This is valid from codes 1 to 2047 and the codes could be integers or decimals. Code 1 programs the LED current to 12.21μA with 25mA maximum LED current. If the bits[1:0] are not set to all 0 in register 0x1B, the maximum LED current will increase and the minimum current (code = 1) will proportionally increase. Code 0 programs 0 current (see Figure 12). When the brightness code < 16, the LED current is in current-to-PWM control. The duty cycle of the PWM is 1/8, and the amplitude of current pulse is 8 times of its corresponding average current. Figure 12 (a) shows the zoomed graph from codes 0 to 16 in Figure 12.

When bit[4] is set to 1 in register 0x11, ramp function is enabled . When bits[7:4] in registers 0x19 are not all 0 (codes from 256 to 4095), regardless of PWM duty cycle, the ramp rate is 128μs/step. When bits[7:4] in registers 0x19 are all 0 (codes from 1 to 255), regardless of PWM duty cycle, the ramp rate is 1024μs/step. For example, if PWM duty cycle is set to 10% and the code is set from 2000 to 4001, when bit[1:0] in register 0x1B is 00, I_{LED_AVG} will change from 1.221mA to 2.442mA, the corresponding ramp rate = 128μs/step, so the ramp time for I_{LED_AVG} = [(4001 - 1) × 0.5 - 2000 × 0.5] × 128μs = 128ms.

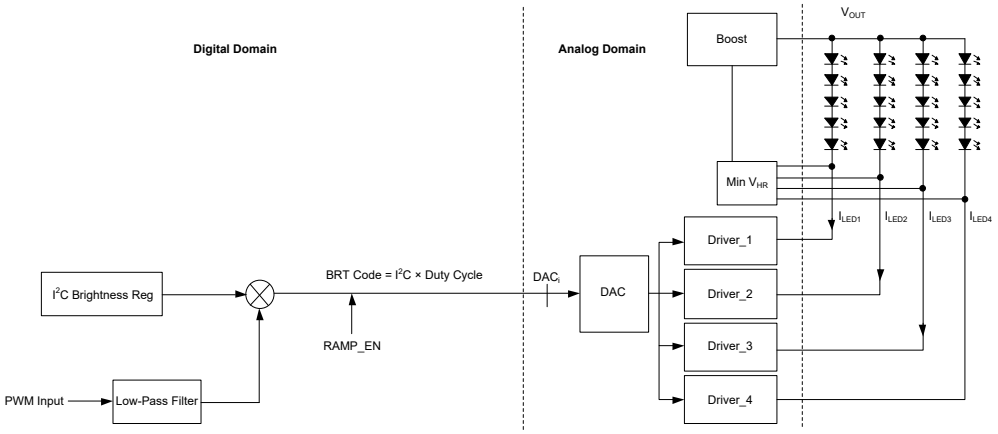


Figure 11. Brightness Control 10 or 11 (I²C + PWM)

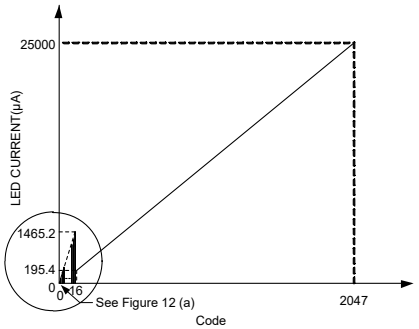


Figure 12. LED Current vs. Brightness Code (Mode 10 or Mode 11)

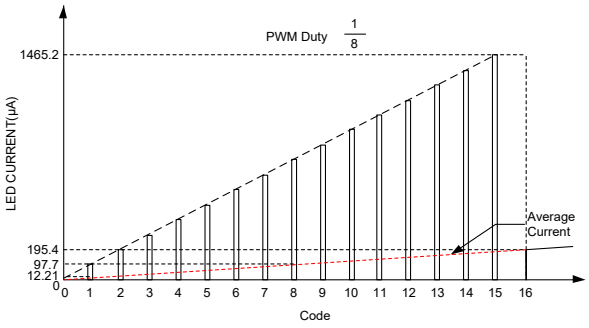


Figure 12 (a).

DETAILED DESCRIPTION (continued)

Hybrid PWM & I²C Dimming Control

Hybrid PWM & I²C dimming control combines PWM dimming and LED current-dimming control methods. With this dimming control, better optical efficiency is possible from the LEDs compared to pure PWM control while still achieving smooth and accurate control and low brightness levels. The switch point from current-to-PWM control is set to get the optimal compromise between good matching of the LEDs brightness/white point at low brightness and good optical efficiency. For I²C mode, the LED current enters current-to-PWM control when bits[7:4] in registers 0x19 are all 0; For other modes, the LED current enters current-to-PWM control when the brightness code < 16 (See Brightness Control Modes).

Phase Shift PWM Scheme

The phase shift PWM (PSPWM) scheme allows overlapping time when each LED current sink is active. When the LED current sinks are not activated simultaneously, the peak load current from the boost output is greatly decreased. This reduces the ripple seen on the boost output and allows smaller output capacitors to be used. Reduced ripple also reduces the output ceramic capacitor audible ringing. The PSPWM scheme also increases the load frequency seen on the boost output by up to three times, therefore transferring the possible audible noise to the frequencies outside the audible range.

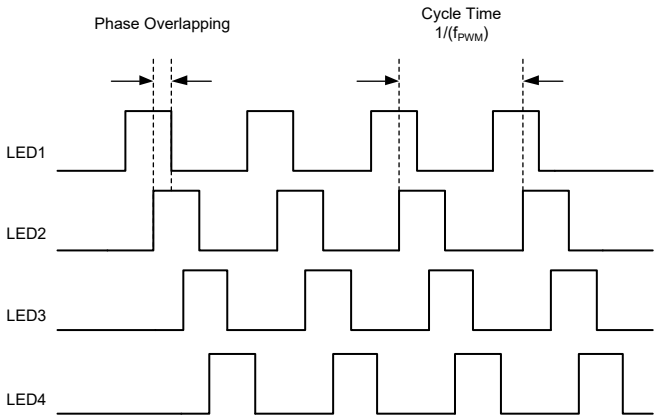


Figure 13. Phase Shift PWM Dimming Scheme Diagram

DETAILED DESCRIPTION (continued)

Fault Protection/Detection

Over-Voltage Protection (OVP)

The SGM37604A provides 29.5V OVP threshold. The OVP circuitry monitors the boost output voltage (V_{OUT}) and protects OUT and SW from exceeding safe operating voltages in case of open load conditions or in the event the LED string voltage requires more voltage than the programmed OVP setting. The operation of OVP differentiates between two over-voltage conditions and responds differently as outlined below:

Case 1 OVP Fault Only (OVP Threshold Hit and All Enabled Current Sink Inputs > 40mV)

In steady-state operation with V_{OUT} near the OVP threshold a rapid change in V_{IN} or brightness code can result in a momentary transient excursion of V_{OUT} above the OVP threshold. In this case the boost circuitry enters skip mode until V_{OUT} drops below OVP - hysteresis (3V). If V_{OUT} remains above the OVP threshold for > 1ms the OVP Fault flag is set (register 0x1F bit[0]).

Case 2 OVP Fault and Open LED String Fault (OVP Threshold Occurrence and Any Enabled Current Sink Input ≤ 40mV)

When any of the enabled LED strings is open the boost converter tries to drive V_{OUT} above OVP and at the same time the open string(s) current sink headroom voltage(s) (LED1, LED2, LED3, LED4) drop to 0. When the SGM37604A detects V_{OUT} > OVP and any enabled current sink input (V_{LED1} or V_{LED2}, V_{LED3}, V_{LED4}) ≤ 40mV, the OVP Fault flag is set (register 0x1F bit[0]), and the LED Open Fault flag is set (register 0x1F bit[4]).

Testing for LED String Open

The procedure for detecting an open in a LED string is:

• Apply power on the SGM37604A.
• Enable all LED strings (register 0x10 bits[4:0] = 11111).
• Set maximum brightness (register 0x1A bits[3:0] = 1111 and register 0x19 = 0xFF).
• Set the brightness control (register 0x11 bits[6:4] = 000).
• Open LED1 string.
• Wait 4msec.
• Read LED Open Fault (register 0x1F bit[4]).
• If bit[4] = 1, then a LED open fault condition has been detected.
• Connect LED1 string.
• Repeat the procedure for the other LED strings.

LED String Short Fault

The SGM37604A can detect an LED string short fault. This happens when the current sink voltage over 16V. This test can only be performed on one LED string at a time. Performing this test with more than one LED string enabled can result in a faulty reading. The procedure for detecting a short in a LED string is:

• Apply power on the SGM37604A.
• Enable only LED1 string (register 0x10 bits[4:0] = 00011).
• Set maximum brightness (register 0x1A bits[3:0] = 1111 and register 0x19 = 0xFF).
• Set the brightness control (register 0x11 bits[6:4] = 000).
• Short LEDs to make the current sink voltage over 16V
• Wait 10msec.
• Read LED Short Fault (register 0x1F bit[3]).
• If bit[3] = 1, then a LED short fault condition has been detected.
• Set LED string enable low (register 0x10 bits[4:0] = 00000).
• Repeat the procedure for the other LED strings.

Over-Current Protection (OCP)

The SGM37604A has OCP threshold (2.2A). The OCP threshold is a cycle-by-cycle current limit and is detected in the internal low-side NFET. Once the threshold is hit the NFET turns off for the remainder of the switching period.

OCP Fault

If enough over-current threshold events occur, the OCP Fault flag (register 0x1F bit[1]) is set. To avoid transient conditions from inadvertently setting the OCP Fault flag, a pulse density counter monitors OCP threshold events over a 128μs period. If 32 consecutive 128μs periods occur where the pulse density count has found 2 or more OCP events, then the OCP Fault flag is set, so there is a 4ms blank time more or less.

Device Over Temperature (TSD)

Thermal shutdown (TSD) is triggered when the device die temperature reaches +160℃. When this happens the boost stops switching, and the TSD Fault flag (register 0x1F bit[2]) is set. The boost automatically starts up again when the die temperature cools down to +140℃.

LEDx Pin Unused

As shown in Figure 14, a user can easily disable the unused channel by connecting its LEDx pin to GND pin or leaving it floating.

DETAILED DESCRIPTION (continued)

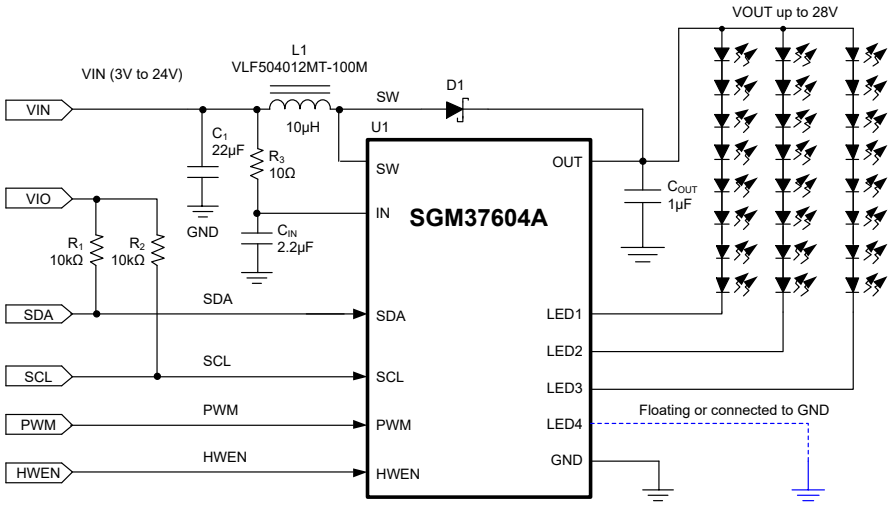


Figure 14. Typical Application for Less than Four Parallel LED Strings

I²C Interface

Start and Stop Conditions

The SGM37604A is configured via an I²C interface. START (S) and STOP (P) conditions classify the beginning and the end of the I²C session (see Figure 15). A START condition is defined as SDA transitioning from high to low while SCL is high. A STOP condition is defined as SDA transitioning from low to high while SCL is high. The I²C master always generates the START and STOP conditions. The I²C bus is considered busy after a START condition and free after a STOP condition. During the data transmission the I²C master can generate repeated START conditions. A START and a repeated START conditions are equivalent function-wise. The data on SDA must be stable during the high period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is low.

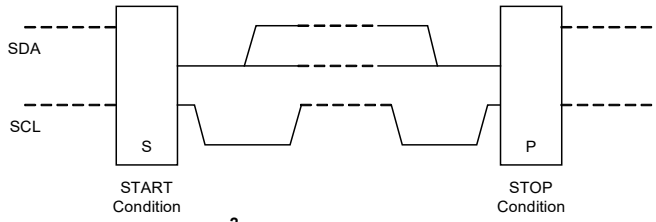


Figure 15. I²C Start and Stop Conditions

I²C Address

The 7-bit chip address for the SGM37604A is (0x36). After the START condition the I²C master sends the 7-bit chip address followed by an eighth bit read or write (R/W). R/W = 0 indicates a WRITE, and R/W = 1 indicates a READ (0x6C in write mode and 0x6D in read mode). The second byte following the chip address selects the register address to which the data is written. The third byte contains the data for the selected register.

Transferring Data

Every byte on the SDA line must be eight bits long with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse, (9th clock pulse), is generated by the master. The master then releases SDA (HIGH) during the 9th clock pulse. The SGM37604A pulls down SDA during the 9th clock pulse, signifying an acknowledge. An acknowledge is generated after each byte has been received.

Register Programming

For glitch free operation, the bits[6:5] in Register 0x11 (Brightness Mode) and bit[4] in Register 0x11 (Ramp Enable) should only be programmed while the LED Enable bits are 0 (register 0x10, Bits[4:1] = 0) and Device Enable bit is 1 (register 0x10, Bit[0] = 1).

APPLICATION INFORMATION

The SGM37604A provides a complete high-performance LED lighting solution for mobile handsets. The SGM37604A is highly configurable and can support multiple LED configurations.

The number of LED strings, number of series LEDs, and minimum input voltage are needed in order to calculate the peak input current. This information guides the designer to make the appropriate inductor selection for the application. The SGM37604A boost converter output voltage (V_{OUT}) is calculated as follows: number of series LEDs × V_F + 0.18V. The SGM37604A boost converter output current (I_{OUT}) is calculated as follows: number of parallel LED strings × 25mA. The SGM37604A peak input current is calculated using Equation 8.

Table 9. Typical Application Component List

CONFIGURATION	L1	D1	C_{OUT}
4P7S, 4P8S	VLF504012MT-100M VLF504012MT-150M	NSR0530P2T5G	C2012X7R1H105K085AC
4P6S	VLF504012MT-220M	NSR0530P2T5G	C2012X7R1H105K085AC
4P5S	VLF403210MT-100M	NSR0530P2T5G	C2012X7R1H105K085AC
4P4S	VLF302510MT-100M	NSR0530P2T5G	C2012X7R1H105K085AC

Component Selection

Inductor

The SGM37604A requires a typical 10μH inductance. When selecting the inductor, ensure that the saturation rating for the inductor is high enough to accommodate the peak inductor current of the application (I_{PEAK}) given in the inductor datasheet. The peak inductor current occurs at the maximum load current, the maximum output voltage, the minimum input voltage, and the minimum switching frequency setting. Also, the peak current requirement increases with decreasing efficiency. I_{PEAK} can be estimated using Equation 8:

$$I_{PEAK} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{V_{IN}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{IN} \times \eta}{V_{OUT}}) \quad (8)$$

Also, the peak current calculated above is different from the peak inductor current setting (I_{SAT}). The NMOS switch current limit setting (I_{CL_MIN}) must be greater than I_{PEAK} from Equation 8 above.

Output Capacitor

The SGM37604A requires a ceramic capacitor with a minimum of 0.4μF of capacitance at the output, specified over the entire range of operation. This ensures that the device remains stable and oscillation free. The 0.4μF of capacitance is the minimum amount of capacitance, which is different than the value of capacitor. Capacitance would take into account tolerance, temperature, and DC voltage shift.

Table 9 lists typical application component.

Table 10 lists possible output capacitors that can be used with the SGM37604A.

The useful voltage range is determined from the effective output voltage range for a given capacitor as determined by Equation 9:

$$\text{DC Voltage Dereating} \geq \frac{0.38\mu F}{(1 - TOL) \times (1 - TEMP\_CO)} \quad (9)$$

For example, with a 10% tolerance, and a 15% temperature coefficient, the DC voltage derating must be ≥ 0.38/(0.9 × 0.85) = 0.5μF. For the C1608X5R1H105K080AB (0603, 50V) device, the useful voltage range occurs up to the point where the DC bias derating falls below 0.523μF, or around 12V. For configurations where V_{OUT} is > 15V, two of these capacitors can be paralleled, or a larger capacitor such as the C2012X5R1H105K085AB must be used.

APPLICATION INFORMATION (continued)

Input Capacitor

The input capacitor in a boost is not as critical as the output capacitor. The primary function of input capacitor is to filter the switching supply currents at the device input and to filter the inductor current ripple at the input of the inductor. The recommended input capacitor is a 2.2μF ceramic (0402, 10V device) or equivalent.

Input Supply Bypassing

The SGM37604A is designed to operate from an input supply range of 3V to 24V. This input supply should be well regulated and be able to provide the peak current required by the LED configuration and inductor selected without voltage drop under load transients (start-up or rapid brightness change). The resistance of the input supply rail should be low enough such that the input current transient does not cause the SGM37604A supply voltage to droop more than 5%. Additional bulk decoupling located close to the input capacitor (C_{IN}) may be required to minimize the impact of the input supply rail resistance.

Table 10. Recommended Output Capacitors

PART NUMBER	MANUFACTURER	CASE SIZE	VOLTAGE RATING (V)	NOMINAL CAPACITANCE (μF)	TOLERANCE (%)	TEMPERATURE COEFFICIENT (%)	RECOMMENDED MAX OUTPUT VOLTAGE (FOR SINGLE CAPACITOR)
C2012X5R1H105K085AB	TDK	0805	50	1	±10	±15	22
C2012X5R1H225K085AB	TDK	0805	50	2.2	±10	±15	24
C1608X5R1V225K080AC	TDK	0603	35	2.2	±10	±15	12
C1608X5R1H105K080AB	TDK	0603	50	1	±10	±15	15

LAYOUT

Layout Guidelines

The SGM37604A's inductive boost converter sees a high switched voltage (up to V_{OVP}) at the SW pin, and a step current (up to I_{CL}) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OUT pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 16 highlights these two noise-generating components.

The following list details the main (layout sensitive) areas of the SGM37604A's inductive boost converter in order of decreasing importance:

- Output Capacitor
  - Schottky Cathode to C_{OUT+}
  - C_{OUT-} to GND
- Schottky Diode
  - SW pin to Schottky Anode
  - Schottky Cathode to C_{OUT+}
- Inductor
  - SW Node PCB capacitance to other traces
- Input Capacitor
  - C_{IN+} to IN pin

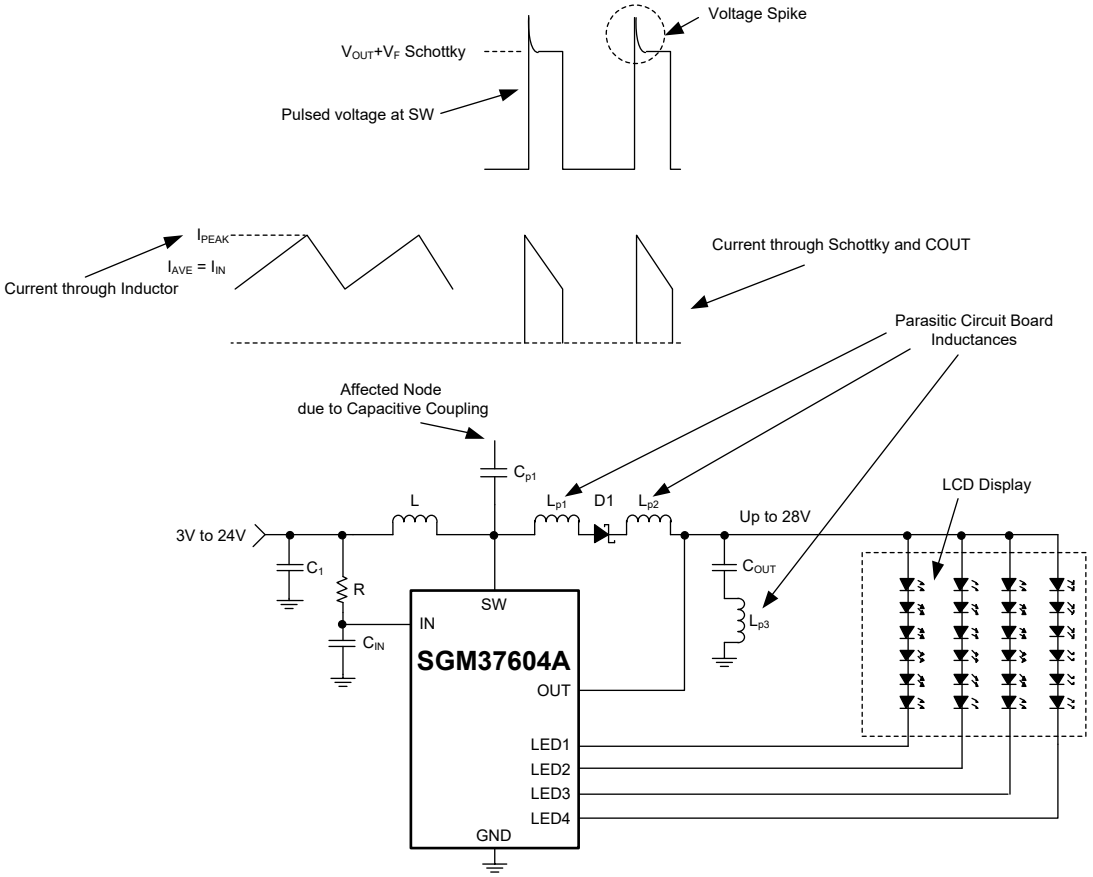


Figure 16. SW Pin Voltage (High Dv/Dt) and Current Through Schottky Diode and C_{OUT} (High Di/Dt)

LAYOUT (continued)

Boost Output Capacitor Placement

Because the output capacitor is in the inductor current discharge path it detects a high-current step from 0 to I_{PEAK} each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through C_{OUT} and back into the SGM37604A's GND pin contributes to voltage spikes (V_{SPIKE} = $L_{P\_}$ × di/dt) at SW and OUT. To avoid this, C_{OUT+} must be connected as close as possible to the cathode of the Schottky diode, and C_{OUT-} must be connected as close as possible to the SGM37604A's GND pin. The best placement for C_{OUT} is on the same layer as the SGM37604A in order to avoid any vias that can add excessive series inductance.

Schottky Diode Placement

In the SGM37604A's boost circuit the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode sees a high-current step from 0 to I_{PEAK} each time the switch turns off and the diode turns on. Any inductance in series with the diode causes a voltage spike (V_{SPIKE} = $L_{P\_}$ × di/dt) at SW and OUT. This can potentially over-voltage the SW pin, or feed through to V_{OUT} and through the output capacitor and into GND. Connecting the anode of the diode as close as possible to the SW pin and the cathode of the diode as close as possible to C_{OUT} can reduce the inductance ($L_{P\_}$) and minimize these voltage spikes.

Inductor Placement

The node where the inductor connects to the SGM37604A's SW pin has 2 issues. First, a large switched voltage (0 to V_{OUT} + $V_{F\_SCHOTTKY}$) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW bump. Any resistance in this path can cause voltage drops that can negatively affect efficiency and reduce the input operating voltage range. To reduce the capacitive coupling of the signal on SW into nearby traces, the SW bump-to-inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, high impedance nodes that are more susceptible to electric field coupling need to be routed away from SW and not directly adjacent or beneath. This is especially true for traces such as SCL, SDA, HWEN and PWM. A GND plane placed directly below SW dramatically reduces the capacitance from SW into nearby traces. Lastly, limit the trace resistance of the VIN to inductor connection and from the inductor to SW connection, by use of short, wide traces.

Boost Input Capacitor Placement

For the SGM37604A boost converter, the input capacitor filters the inductor current ripple and the internal MOSFET driver currents during turn-on of the internal power switch. The driver current requirement can range from 50mA at 3V to over 200mA at 5.5V with fast durations of approximately 10ns to 20ns. This appears as high di/dt current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN pin and to the GND pin is critical since any series inductance between IN and C_{IN+} or C_{IN-} and GND can create voltage spikes that could appear on the VIN supply line and in the GND plane. Close placement of the input bypass capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the SGM37604A, form a series RLC circuit. If the output resistance from the source (R_S) is low enough the circuit is underdamped and has a resonant frequency (typically the case). Depending on the size of L_S the resonant frequency could occur below, close to, or above the SGM37604A switching frequency. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the SGM37604A switching frequency;
2. Greater than the inductor current ripple when the resonant frequency occurs near the switching frequency; or
3. Less than the inductor current ripple when the resonant frequency occurs well below the switching frequency.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2019 – REV.A to REV.A.1

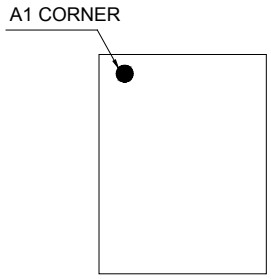
Changed Register Maps section 9
Changed Detailed Description section 16

Changes from Original (SEPTEMBER 2018) to REV.A

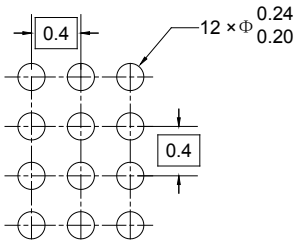
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

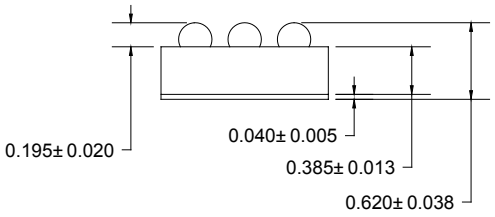
WLCSP-1.78×1.36-12B



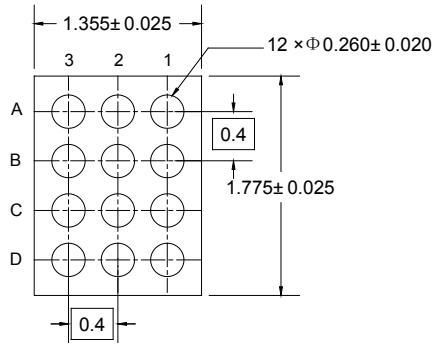
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

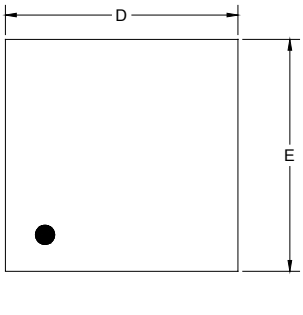


BOTTOM VIEW

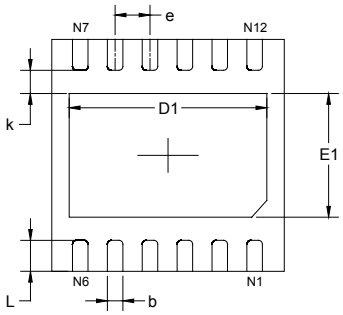
NOTE: All linear dimensions are in millimeters.

PACKAGE OUTLINE DIMENSIONS

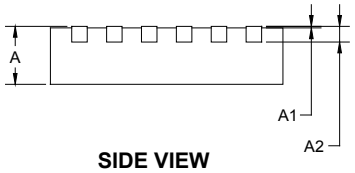
TDFN-3×3-12L



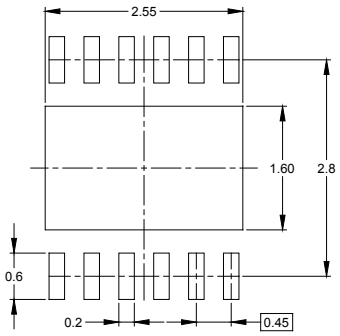
TOP VIEW



BOTTOM VIEW



SIDE VIEW

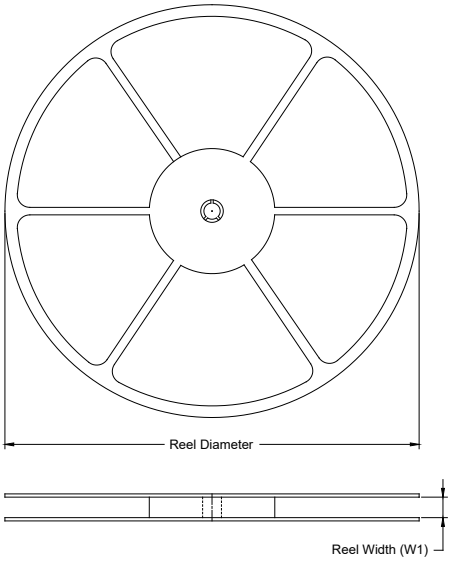


RECOMMENDED LAND PATTERN (Unit: mm)

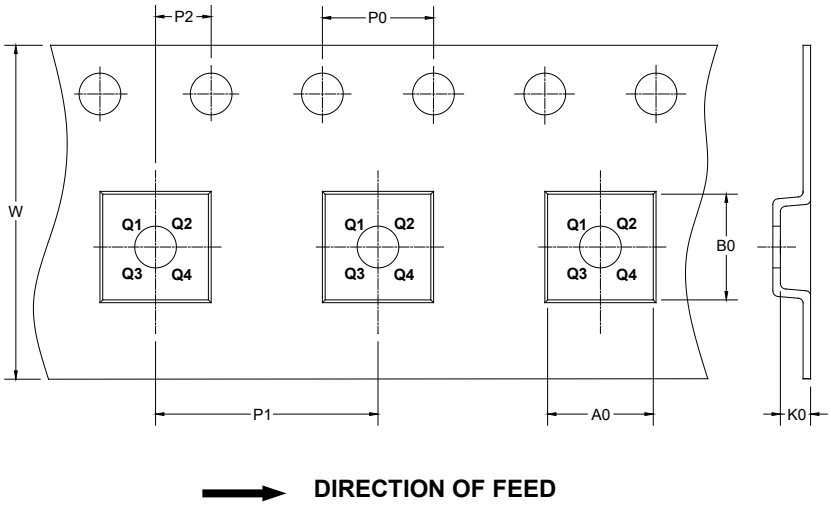
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.924	3.076	0.115	0.121
D1	2.450	2.650	0.096	0.104
E	2.924	3.076	0.115	0.121
E1	1.500	1.700	0.059	0.067
k	0.200 MIN		0.008 MIN	
b	0.150	0.250	0.006	0.010
e	0.450 TYP		0.018 TYP	
L	0.324	0.476	0.013	0.019

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



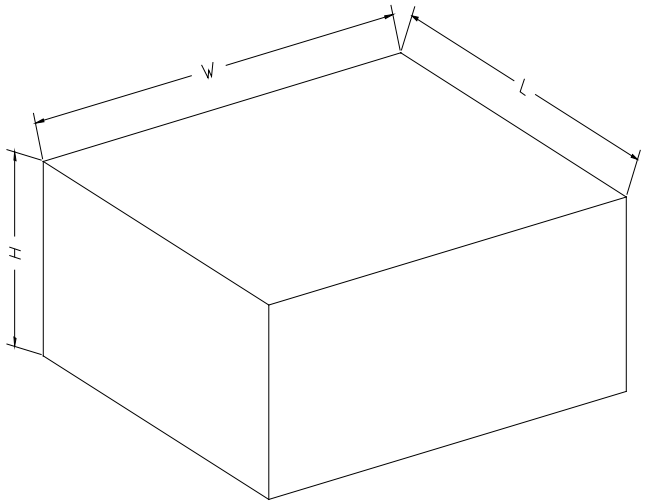
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.78×1.36-12B	7″	9.2	1.46	1.90	0.81	4.0	4.0	2.0	8.0	Q1
TDFN-3×3-12L	13″	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002