SGM41283

GENERAL DESCRIPTION

The SGM41283 is a monolithic step-up converter that integrates a power switch and a biased avalanche photodiode (APD) current monitor. The device can double the output voltage through the APD optical receivers. The SGM41283 can provide up to 70V output.

The SGM41283 uses a current-mode, fixed-frequency architecture to regulate the output voltage, which provides a fast transient response and cycle-by-cycle current limiting. The SGM41283 features two accurate APD current monitoring outputs with 10:1 and 2:1 ratios, respectively. Resistor-adjustable current limiting protects the APD from optical power transients.

The SGM41283 includes over-current and thermaloverload protection to prevent damage in the event of an output overload.

The SGM41283 is available in Green TQFN-3×3-16L package. It operates over an ambient temperature range of -40℃ to +85℃.

with APD Current Monitor

● **2.7V to 5.5V Input Voltage**

FEATURES

- **72V/0.6Ω NFET with 1.1A Limit**
- **Up to 70V Output Voltage**
- **50ns APD Current Monitoring Response Speed**

70V Step-Up Converter

- **850kHz Fixed Switching Frequency**
- **Internal Compensation and Soft-Start**
- **High-side APD Current Monitor with Less than ±5% Tolerance**
- **High-side Current Monitor Ratio:10:1 and 2:1**
- **Thermal-Shutdown Protection**
- **Programmable APD Over-Current Limit and Protection**
- **-40**℃ **to +85**℃ **Operating Temperature Range**
- **Available in Green TQFN-3×3-16L Package**

APPLICATIONS

APD Biasing PIN Diode Biasing Optical Receivers and Modules Fiber-Optic-Network Equipment

Figure 1. Typical Application Circuit

TYPICAL APPLICATION

PACKAGE/ORDERING INFORMATION

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

RECOMMENDED OPERATING CONDITIONS

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any otherconditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION

PIN DESCRIPTION

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, V_{EN} = 3.3V, typical values are at T_A = +25°C, unless otherwise noted.)

TYPICAL PERFORMANCE CHARACTERISTICS

FUNCTIONAL BLOCK DIAGRAM

APPLICATION INFORMATION

The SGM41283 step-up converter uses a constantfrequency, current-mode control scheme to provide excellent line and load regulation.

At the start of each oscillator cycle, the RS latch is set, which turns on the power switch. The output of current sense amplifier which is proportional to the switching current is added to a generated ramp. The resulting sum is fed into the positive terminal of the PWM comparator. The RS latch resets, turning off the power switch as soon as the positive terminal exceeds the level of negative input of PWM comparator which is proportional to the difference between the feedback voltage and the reference voltage. As the load varies, the error amplifier sets the switching peak current necessary to supply the load and regulate the output voltage.

SGM41283 has an integrated high-side APD current monitor. The MONx pin has an open-circuit protection feature and is internally clamped to 4V. MON1 and MON2 mirror the load current on the APD pin, and convert the currents to voltage signals through resistors R_{MOM1} and R_{MOM2} . The current mirror ratios are set to be 10:1 and 2:1. The APD output current has over-current protection with a threshold programmed by an external resistor at the RLIM pin.

APD Current-Limit Design

The current limit can be adjusted from 0mA to 2.5mA. Calculate the value of the external resistor, RLIM, for a given current limit, ILIM, using the following equation:

$$
R_{\text{RLIM}}(k\Omega) = \frac{70}{I_{\text{APD,MAX}}} (mA)
$$
 (1)

Soft-Start

There is no need for a soft-start because V_{OUT} rises very slowly on the order of ms. The portion of the inductor current that actually drives up the output voltage is small due to the high conversion ratio. The inductor current limit 1.1A (TYP), the output capacitor 0.1 μ F (TYP), and V_{IN} limit the V_{OUT} rise time.

VOUT Programming

A resistor feedback network programs the output voltage. Typically, the top resistor from V_{OUT} to V_{FB} is 1MΩ. The bottom resistor from V_{FB} to GND is:

$$
R_{\text{BOTTM}}(k\Omega) = R_{\text{TOP}}(k\Omega) \times \frac{V_{\text{FB}}}{V_{\text{OUT}} - V_{\text{FB}}}
$$
 (2)

In addition, place a series resistor and capacitor of 100kΩ and 100pF, respectively, in parallel with R_{TOP} . This gives a phase boost for good phase margin as well as decreases the gain for good gain margin in the extreme cases of V_{IN} and V_{OUT} .

Inductor Design

Three key inductor parameters must be specified for operation with the SGM41283: inductance value (L), inductor saturation current (ISAT), and DC resistance (DCR). In general, the inductor should have a saturation current rating greater than the maximum peak switch current-limit value (ILIM_SW = 1.1A). DCR should be be low for reasonable efficiency. The SGM41283 was designed for operation with inductors in the 1.5μH to 4μH range. Typically, 2.0μH inductor is recommended.

Diode Design

Due to the high-output voltage combined with the diode capacitive coupling, there is a significant reverse current through the inductor. Generally, a low reverse bias capacitance equates to a low reverse inductor current. However, this is not always true though; so test the diodes prior to final selection. Two recommended diodes with relatively small reverse currents are the DFLS1150-7 (Diodes Inc, Schottky, 1A (AVG), 150V) and the BAT46ZFILM (STMicroelectronics, Schottky, 150mA (AVG), 100V).

APPLICATION INFORMATION (continued)

RMON1, RMON2 Design

The maximum allowed voltage on either R_{MON1} or R_{MON2} is 2.5V (TYP). The maximum allowed current is 2.5mA (TYP). For faster response, chose the maximum output less than the maximum allowed voltage.

$$
I_{MON1,MAX}(mA) = \frac{I_{APD,MAX}}{10}
$$
 (3)

$$
I_{\text{MON2,MAX}}(mA) = \frac{I_{\text{APD,MAX}}}{20}
$$
 (4)

$$
R_{\text{MON1}}(k\Omega) = \frac{V_{\text{MON1,MAX}}}{I_{\text{MON1,MAX}}}
$$
(5)

$$
R_{\text{MON2}}\left(k\Omega\right) = \frac{V_{\text{MON2,MAX}}}{I_{\text{MON2,MAX}}}
$$
(6)

Where: $V_{MON1,MAX}$, $V_{MON2,MAX}$ < 2.5V.

CIN Design

If the C_{IN} is not big enough, the initial current pulses will pull VIN down below UVLO during power start-up. This may cause false starts. Select a C_{IN} of at least 10μF.

Table 1. Recommended Values (V_{IN}: 2.7V to 5.5V)

COUT Design

For most applications, use a small output capacitor of 0.1μF or greater. To achieve low output ripple, a capacitor with low ESR, low ESL, and high capacitance value should be selected. If tantalum or electrolytic capacitors are used to achieve high capacitance values, always add a smaller ceramic capacitor in parallel to bypass the high-frequency components of the diode current. The higher ESR and ESL of electrolytic capacitors increase the output ripple and peak-to-peak transient voltage. Assuming the contribution from the ESR and capacitor discharge equals 50% (proportions may vary), calculate the output capacitance and ESR required for a specified ripple using the following equations:

$$
C_{\text{OUT}}\ (\mu F) = \frac{I_{\text{OUT}}}{0.5 \times \Delta V_{\text{OUT}}}\left[t_{\text{s}} - \frac{I_{\text{PEAK}} \times L_{\text{OPTIMUM}}}{V_{\text{OUT}} - V_{\text{IN_MIN}}}\right] \tag{7}
$$

$$
ESR (m\Omega) = \frac{0.5 \times \Delta V_{\text{OUT}}}{I_{\text{OUT}}}
$$
 (8)

PACKAGE OUTLINE DIMENSIONS

TQFN-3×3-16L

RECOMMENDED LAND PATTERN (Unit: mm)

TAPE AND REEL INFORMATION

REEL DIMENSIONS

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

CARTON BOX DIMENSIONS

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

