NCP110

Linear Regulator, Low V_{IN}, Low Noise and High PSRR, 200 mA

The NCP110 is a linear regulator capable of supplying 200 mA output current from 1.1 V input voltage. The device provides wide output range from 0.6 V up to 4.0 V, very low noise and high PSRR. Due to low quiescent current the NCP110 is suitable for battery powered devices such as smartphones and tablets. The device is designed to work with a 1 μF input and a 1 μF output ceramic capacitor. It is available in ultra−small 0.35P, 0.64 mm x 0.64 mm Chip Scale Package (CSP) and XDFN4 0.65P, 1 mm x 1 mm.

Features

- Operating Input Voltage Range: 1.1 V to 5.5 V
- Available in Fixed Voltage Option: 0.6 V to 4.0 V
- ±2% Accuracy Over Load/Temperature
- Ultra Low Quiescent Current Typ. 20 μA
- Standby Current: Typ. 0.1 μA
- Very Low Dropout: 70 mV for 1.05 V @ 100 mA
- High PSRR: Typ. 95 dB at 20 mA, f = 1 kHz
- Ultra Low Noise: 8.8 μV_{RMS}
- Stable with a 1 μF Small Case Size Ceramic Capacitors
- Available in −WLCSP4 0.64mm x 0.64mm x 0.33mm − Case 567VS
  −XDFN4 1mm x 1mm x 0.4mm − Case 711AJ
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery−powered Equipment
- Smartphone, Tablets
- Digital Cameras
- Smoke Detectors
- Portable Medical Equipment
- RF, PLL, VCO and Clock Power Supplies
- Battery Powered Wireless IoT Modules

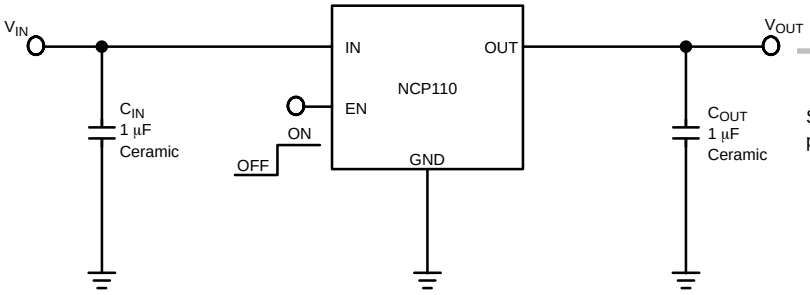
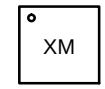


Figure 1. Typical Application Schematics

MARKING DIAGRAMS

WLCSP4
CASE 567VS



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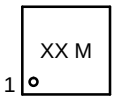
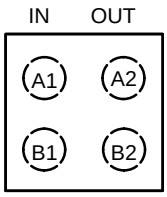
XDFN4
CASE 711AJ

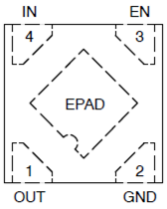


X or XX = Specific Device Code
M = Date Code

PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 14 of this data sheet.

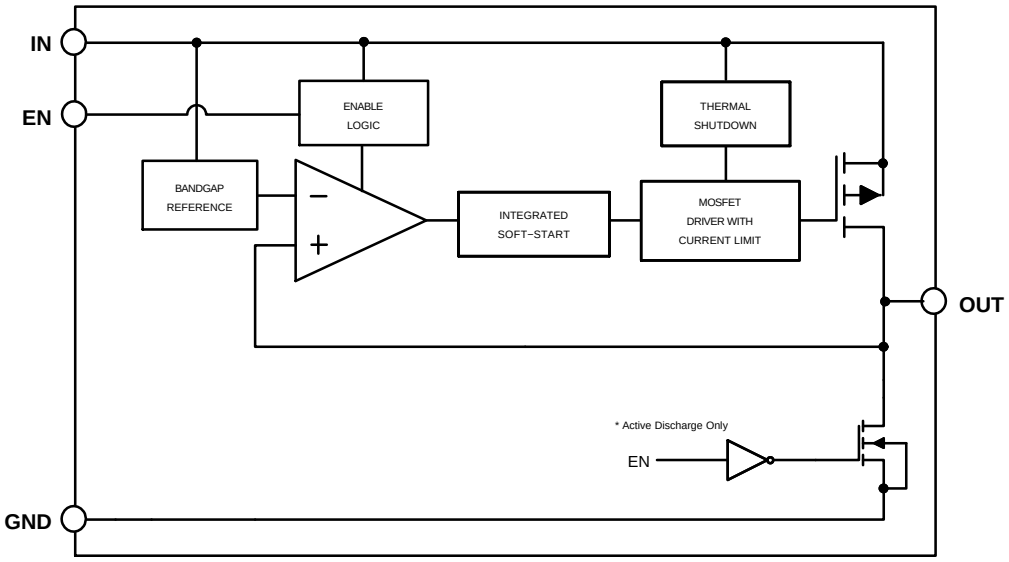


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. CSP4	Pin No. XDFN4	Pin Name	Description
A1	4	IN	Input voltage supply pin
A2	1	OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor.
B1	3	EN	Chip enable: Applying V_{EN} < 0.2 V disables the regulator, Pulling V_{EN} > 0.7 V enables the LDO.
B2	2	GND	Common ground connection
−	EPAD	EPAD	Expose pad can be tied to ground plane for better power dissipation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3, max. 6 V	V
Chip Enable Input	V_{CE}	−0.3 to 6 V	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, CSP4 (Note 3) Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	108	°C/W
Thermal Characteristics, XDFN4 (Note 3) Thermal Resistance, Junction−to−Air		208	