SGM2049
2A, High Accuracy, Low Noise, Low Dropout Linear Regulator

GENERAL DESCRIPTION

The SGM2049 is a low noise, very low dropout linear regulator which operates from input voltage as low as 1.1V. It is capable of supplying 2A output current with typical dropout voltage of only 70mV. The SGM2049 output voltage is pin-selectable from 0.8V to 3.95V and adjustable from 0.8V to 5.2V using an external resistor divider.

The low noise, high PSRR and high output current capabilities make the SGM2049 ideal to power noise-sensitive devices such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs) and RF components.

With very high accuracy, remote sensing, and soft-start capabilities to reduce inrush current, the SGM2049 ensures the optimal system performance for powering digital loads such as FPGAs, DSPs, and ASICs. These applications require low-input voltage, low-output voltage operation, the exceptional accuracy, remote sensing, excellent transient performance and soft-start capabilities.

The SGM2049 is available in Green TQFN-3.5×3.5-20L and TQFN-5×5-20L packages. It operates over an operating temperature range of -40℃ to +125℃.

APPLICATIONS

Digital Loads:

SerDes, FPGAs and DSPs

Instrumentation, Medical and Audio

High-Speed Analog Circuits:

VCO, ADC, DAC and LVDS

Imaging: CMOS Sensors and Video ASICs

Test and Measurement

FEATURES

- **Low Dropout Voltage:**
  70mV (TYP) at 2A with Bias
- **Low Noise: 6.3μV_{RMS} (TYP)**
- **Input Voltage Range:**
  - **Without Bias: 1.4V to 7V**
  - **With Bias: 1.1V to 7V**
- **Output Voltage Range:**
  - **Adjustable Operation: 0.8V to 5.2V**
  - **Pin-Selectable Operation: 0.8V to 3.95V**
- **Excellent Load Transient Response**
- **Adjustable Soft-Start Inrush Control**
- **Open-Drain Power-Good (PG) Output**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TQFN-3.5×3.5-20L and TQFN-5×5-20L Packages**

TYPICAL APPLICATION

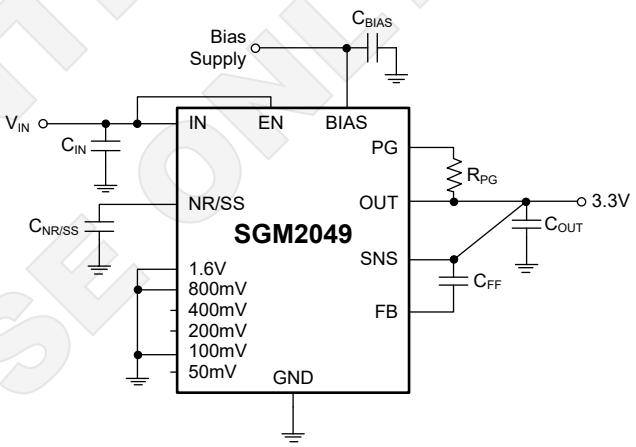

Figure 1. Typical Application Circuit

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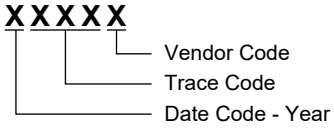
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2049	TQFN-3.5×3.5-20L	-40℃ to +125℃	SGM2049XTRL20G/TR	SGM2049 XTRL20 XXXXX	Tape and Reel, 4000
	TQFN-5×5-20L	-40℃ to +125℃	SGM2049XTRM20G/TR	SGM2049 XTRM20 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, BIAS, PG, EN to GND ..... -0.3V to 8V
SNS, OUT to GND ..... -0.3V to Min(V_{IN} + 0.3V, 8V)
NR/SS, FB to GND ..... -0.3V to 3.6V
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V to GND
..... -0.3V to V_{OUT} + 0.3V
PG Current (Sink Current into Device) 5mA
Package Thermal Resistance
TQFN-3.5×3.5-20L, θ_{JA} ..... 40℃/W
TQFN-5×5-20L, θ_{JA} ..... 37℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage Range ..... 1.1V to 7V
Bias Supply Voltage Range (1) ..... 3V to 7V
Output Voltage Range (2) ..... 0.8V to 5.2V
Enable Voltage Range ..... 0V to V_{IN}
Output Current ..... 0A to 2A
Input Capacitance, C_{IN} ..... 5μF (MIN)
Output Capacitance, C_{OUT} ..... 10μF to 1000μF
Bias Capacitance, C_{BIAS} ..... 5μF (MIN)
Power-Good Pull-Up Resistance ..... 10kΩ to 100kΩ
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTES:
1. Bias supply is required when the V_{IN} supply is below 1.4V. Conversely, no bias supply is required when the V_{IN} supply is higher than or equal to 1.4V.
2. This output voltage range does not include device accuracy or accuracy of the feedback resistors.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

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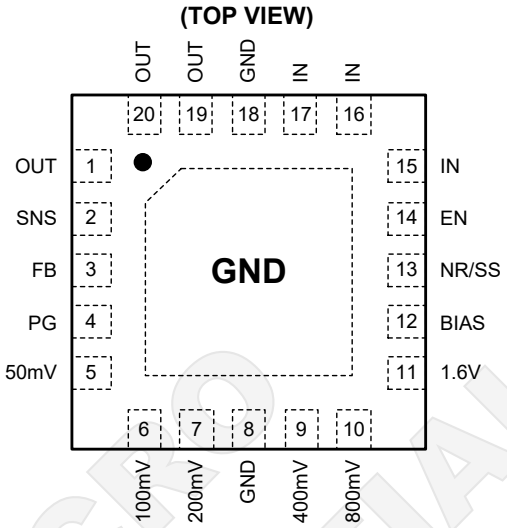
PIN CONFIGURATIONS



TQFN-3.5×3.5-20L/TQFN-5×5-20L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 19, 20	OUT	Regulator Output Pins. It is recommended to use output capacitor with effective capacitance in the range of 10μF to 1000μF. Place the output capacitor as close to the device as possible and minimize the impedance between OUT pins to the load.
2	SNS	Output Voltage Sense Input Pin. This pin connects the internal R1 resistor to the output. Connect this pin to the load side of the output trace only if the pin-selectable feature is used. Keep SNS pin floating if the V_{OUT} voltage is set by external resistor.
3	FB	Feedback Voltage Input Pin. This pin is used to set the desired output voltage via an external resistive divider. Although not required, it is recommended to use a 10nF feed-forward capacitor from FB to OUT pins (as close to the device as possible) to maximize AC performance. The use of a feed-forward capacitor may disrupt power-good functionality.
4	PG	Power-Good Indicator Output Pin. An open-drain output indicates when the output voltage reaches $V_{IT(PG)}$ of the target. The pin is pulled to ground when the output voltage is lower than its specified threshold, EN shutdown, OCP and OTP. The use of a feed-forward capacitor may disrupt power-good functionality.
5	50mV	Output Voltage Setting Pins. Connect these pins to ground or leave floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) if the V_{OUT} voltage is set by external resistor.
6	100mV	
7	200mV	
9	400mV	
10	800mV	
11	1.6V	
12	BIAS	Bias Supply Voltage Pin for Internal Control Circuits. This pin enables the use of low-input voltage, low-output voltage conditions (that is, V_{IN} = 1.2V, V_{OUT} = 1V) to reduce power dissipation across the chip die. A 10μF or larger capacitor must be connected between this pin and ground. This pin must be left floating or tied to ground if not used.
13	NR/SS	Noise-Reduction and Soft-Start Pin. Decouple this pin to GND with an external capacitor $C_{NR/SS}$ can not only reduce output noise to very low levels but also enable the soft-start function to slow down the rising of V_{OUT}. A 10nF or larger capacitor as close as possible to NR/SS pin is suggested for low noise application.
14	EN	Enable Pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. This pin must be connected to IN or BIAS pin if enable functionality is not used.
15-17	IN	Input Supply Voltage Pins. A 10μF or larger ceramic capacitor from IN pins to ground is required and should be placed as close to the input as possible for better noise rejection.
8, 18	GND	Ground Pins. These pins must be connected to ground, the thermal pad and each other with a low-impedance connection.
Exposed Pad	GND	Exposed Thermal Pad. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

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ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.4V) or 1.4V, whichever is greater, V_{BIAS} = Open, $V_{OUT(NOM)}$ = 0.8V (1), V_{EN} = 1.1V, C_{IN} = 10μF, C_{OUT} = 22μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage Range (2)	V_{IN}	T_J = +25℃	1.1		7	V
Bias Supply Voltage Range (2)	V_{BIAS}	V_{IN} = 1.1V, T_J = +25℃	3		7	V
Feedback Voltage	V_{FB}			0.8		V
NR/SS Pin Voltage	$V_{NR/SS}$			0.8		V
Input Supply UVLO with Bias	$V_{UVLO1(IN)}$	V_{IN} rising with V_{BIAS} = 3V		1		V
$V_{UVLO1(IN)}$ Hysteresis	$V_{HYS1(IN)}$	V_{BIAS} = 3V		135		mV
Input Supply UVLO without Bias	$V_{UVLO2(IN)}$	V_{IN} rising		1.3		V
$V_{UVLO2(IN)}$ Hysteresis	$V_{HYS2(IN)}$			60		mV
Bias Supply UVLO	$V_{UVLO(BIAS)}$	V_{BIAS} rising, V_{IN} = 1.1V		2.8		V
$V_{UVLO(BIAS)}$ Hysteresis	$V_{HYS(BIAS)}$	V_{IN} = 1.1V		250		mV
Output Voltage Range	V_{OUT}	Pin-selectable operation, T_J = +25℃	0.8		3.95	V
		Adjustable operation, using external resistors (3), T_J = +25℃	0.8		5.2	
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 1.4V to 7V, I_{OUT} = 5mA		0.25		mV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{BIAS} = 3V to 7V, V_{IN} = 1.1V, I_{OUT} = 5mA to 2A		0.25		mV/A
		I_{OUT} = 5mA to 2A		0.25		
		I_{OUT} = 5mA to 2A, V_{OUT} = 5.2V		0.7		
Dropout Voltage	V_{DROP}	V_{IN} = 1.4V, I_{OUT} = 2A, V_{FB} = 0.8V - 3%		72		mV
		V_{IN} = 5.2V, I_{OUT} = 2A, V_{FB} = 0.8V - 3%		70		
		V_{IN} = 1.1V, V_{BIAS} = 5V, V_{FB} = 0.8V - 3%, I_{OUT} = 2A		70		
Output Current Limit	I_{LIMIT}	V_{OUT} forced at 0.9 × $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.4V		3.4		A
Short-Circuit Current Limit	I_{SC}	R_{LOAD} = 20mΩ, under foldback operation		1.6		A
GND Pin Current	I_{GND}	V_{IN} = 7V, I_{OUT} = 5mA		3.5		mA
		V_{IN} = 1.4V, I_{OUT} = 2A		3.6		mA
		Shutdown, PG = Open, V_{IN} = 7V, V_{EN} = 0.5V		1.2		μA
EN Pin Current	I_{EN}	V_{IN} = 7V, V_{EN} = 0V and 7V		0.04		μA
BIAS Pin Current	I_{BIAS}	V_{IN} = 1.1V, V_{BIAS} = 7V, $V_{OUT(NOM)}$ = 0.8V, I_{OUT} = 2A		3.1		mA
EN Pin Low-Level Input Voltage (Disable Device)	$V_{IL(EN)}$	T_J = +25℃	0		0.5	V
EN Pin High-Level Input Voltage (Enable Device)	$V_{IH(EN)}$	T_J = +25℃	1.1		7	V
PG Pin Threshold	$V_{IT(PG)}$	For falling V_{OUT}		88% × V_{OUT}		V
PG Pin Hysteresis	$V_{HYS(PG)}$	For rising V_{OUT}		2% × V_{OUT}		V
PG Pin Low-Level Output Voltage	$V_{OL(PG)}$	V_{OUT} < $V_{IT(PG)}$, I_{PG} = -1mA (current into device)		0.23		V
PG Pin Leakage Current	$I_{lkg(PG)}$	V_{OUT} > $V_{IT(PG)}$, V_{PG} = 7V		0.01		μA
NR/SS Pin Charging Current	$I_{NR/SS}$	$V_{NR/SS}$ = GND, V_{IN} = 7V		6.4		μA
FB Pin Leakage Current	I_{FB}	V_{IN} = 7V		2		nA

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ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.4V) or 1.4V, whichever is greater, V_{BIAS} = Open, $V_{OUT(NOM)}$ = 0.8V (1), V_{EN} = 1.1V, C_{IN} = 10μF, C_{OUT} = 22μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	PSRR	V_{OUT} = 0.8V, V_{IN} - V_{OUT} = 0.4V, V_{BIAS} = 5V, I_{OUT} = 2A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 22μF	f = 10kHz		45		dB
			f = 500kHz		25		
		V_{OUT} = 5V, V_{IN} - V_{OUT} = 0.4V, I_{OUT} = 2A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 22μF	f = 10kHz		45		
			f = 500kHz		20		
Output Noise Voltage	e_n	BW = 10Hz to 100kHz, V_{OUT} = 0.8V, V_{BIAS} = 5V, I_{OUT} = 2A, V_{IN} = 1.1V, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 22μF			6.3		μV_{RMS}
		BW = 10Hz to 100kHz, V_{OUT} = 5V, I_{OUT} = 2A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 22μF			12		
Thermal Shutdown Temperature	T_{SHDN}				160		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}				20		℃
Operating Junction Temperature				-40		+125	℃

NOTES:

1. $V_{OUT(NOM)}$ is the calculated V_{OUT} target value from the pin-selectable in a fixed configuration. In an adjustable configuration, $V_{OUT(NOM)}$ is the expected V_{OUT} value set by the external feedback resistors.
2. The bias supply is required when the V_{IN} supply is below 1.4V. Conversely, no bias supply is required when the V_{IN} supply is higher than or equal to 1.4V.
3. When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.

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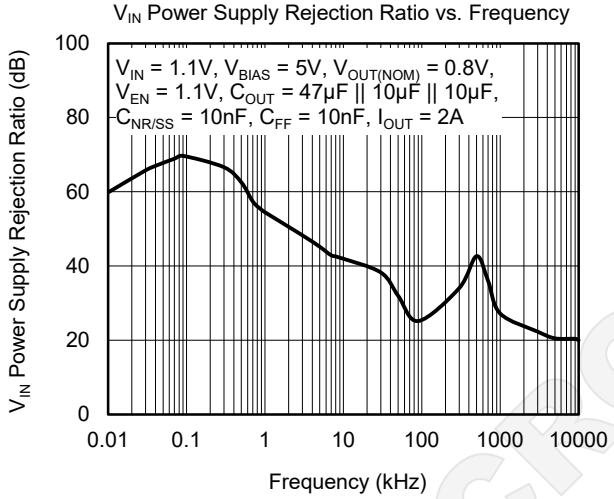
TYPICAL PERFORMANCE CHARACTERISTICS

At T_J = +25℃, unless otherwise noted.



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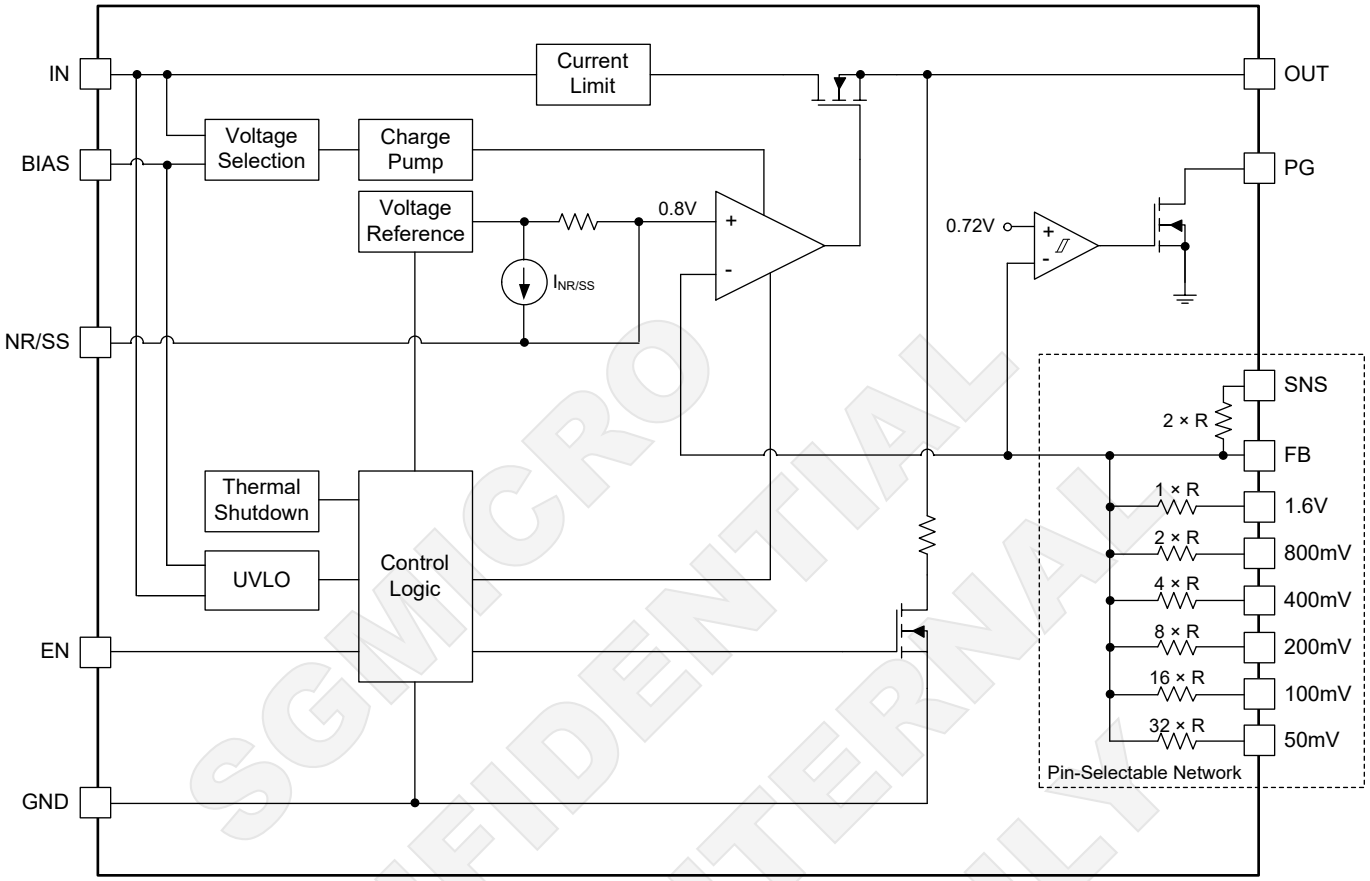
FUNCTIONAL BLOCK DIAGRAM



NOTE: For the pin-selectable network, the ratios between the values are highly accurate as a result of matching, but the actual resistance may vary significantly from the numbers listed.

Figure 2. Block Diagram

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DETAILED DESCRIPTION

The SGM2049 is capable of supplying 2A output current with typical dropout voltage of only 70mV. It is a high accuracy, low noise, low dropout linear voltage regulator. These features make the device a robust solution to solve many challenging problems in generating a clean, accurate power supply. The high performance also makes the SGM2049 useful in a variety of applications. See Table 1 for a categorization of the functionalities shown in Functional Block Diagram.

Table 1. Features

Voltage Regulation	System Start-Up	Internal Protection
High Accuracy	Programmable Soft-Start	Foldback Current Limit
Low Noise, High PSRR Output	No Sequencing Requirement between BIAS, IN and EN	Thermal Shutdown
Fast Transient Response	Power-Good Output	
	Start-Up with Negative Bias on OUT	

These features make the SGM2049 have versatility and ability to generate a supply for most applications.

System Start-Up

The SGM2049 start-up can be adjustable by user to benefit power supply during turn-on within a specific window of time to either ensure proper operation of the load or to minimize the loading on the input supply or other sequencing requirements. This function benefits many power supply design engineers to solve the demanding requirements.

Programmable Soft-Start

The noise-reduction and soft-start capacitor ($C_{NR/SS}$) accomplishes the dual purpose of both noise-reduction and programming the soft-start ramp time during turn-on.

Enable (EN)

The SGM2049 provides an EN pin, as an external chip digital control, to enable or disable the device. The enable signal (V_{EN}) is an active-high digital control that enables the device when the enable voltage is past the rising threshold ($V_{EN} \geq V_{IH(EN)}$) and disables the device when the enable voltage is below the falling threshold ($V_{EN} \leq V_{IL(EN)}$).

Under-Voltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before V_{IN} rises above the V_{UVLO} threshold. The UVLO circuit responds quickly to glitches on the IN pin or BIAS pin and attempts to disable the output of the device if either of these rails collapses. The local input capacitance prevents severe brownouts in most applications.

Active Discharge

When either EN or UVLO is low, the SGM2049 discharges the device output (via the OUT pins) through an internal current sink to ground. Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input when $V_{OUT} > V_{IN}$, which can cause damage to the device (when $V_{OUT} > V_{IN} + 0.3V$); see the Reverse Current Protection section for more details.

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DETAILED DESCRIPTION (continued)

Power-Good Output (PG)

The PG circuit monitors the feedback pin voltage to indicate the status of the output voltage. The PG pin requires an external pull-up resistor, which is typically connected to the OUT pins and active high. The PG circuit sets the PG pin into a high-impedance state to indicate that the power is good. If this feature is not used, connect this pin to ground. PG can be used to signal other devices in a system when the output voltage is approximately or above the set output voltage ($V_{OUT(NOM)}$). The PG signal provides an easy solution to meet demanding sequencing requirements. A simplified schematic is shown in Figure 3.

Using a large feed-forward capacitor (C_{FF}) delays the output voltage and because the PG circuit monitors the FB pin, the PG signal can indicate a false positive. A simple solution to this scenario is to use an external voltage detector device, see Feed-Forward Capacitor (C_{FF}) for more information.

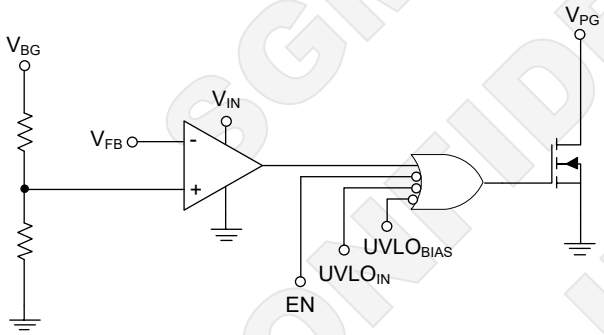

Figure 3. Simplified PG Circuit

Internal Protection

Fault events such as short circuits and excessive heat can occur that damage devices in many applications. The SGM2049 implements the circuit to protect the device and its load during these events. Continuously operating in these fault conditions or above a junction temperature of +125℃ is not recommended because the long term reliability of the device is reduced.

Foldback Current Limit (I_{LIMIT})

The SGM2049 continuously monitors the output current to protect the pass transistor against abnormal operations. The internal current limit circuit is used to protect the device against high load current faults or shorting events. A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If the load current demand exceeds the foldback current limit before EN goes high, the device does not start up. Thermal shutdown can activate during a current limit event because of the high-power dissipation typically found in these conditions. Minimize the inductances to the input and load to ensure proper operation of the current limit.

Thermal Protection

The SGM2049 implements thermal shutdown protection. When the thermal protection circuit activated, the regulator output turns off. When it cools down under the low temperature threshold, device output is activated again. The thermal shutdown protection is provided to prevent failures from accidental over-heating.

A high-power dissipation across the device, combined with a high ambient temperature (T_A), can cause T_J to be greater than or equal to T_{SHDN}, triggering the thermal shutdown and causing the output to fall to 0V. The device can cycle on and off when thermal shutdown is reached under these conditions.

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APPLICATION INFORMATION

Adjustable Operation

The SGM2049 can be set either with the internal pin-selectable network or by using external resistors to achieve different output voltages. Using the pin-selectable network allows the SGM2049 to be programmed from 0.8V to 3.95V. For output voltage range greater than 3.95V and up to 5.2V, external resistors must be used. The output voltage is set by two resistors, as shown in Figure 4.

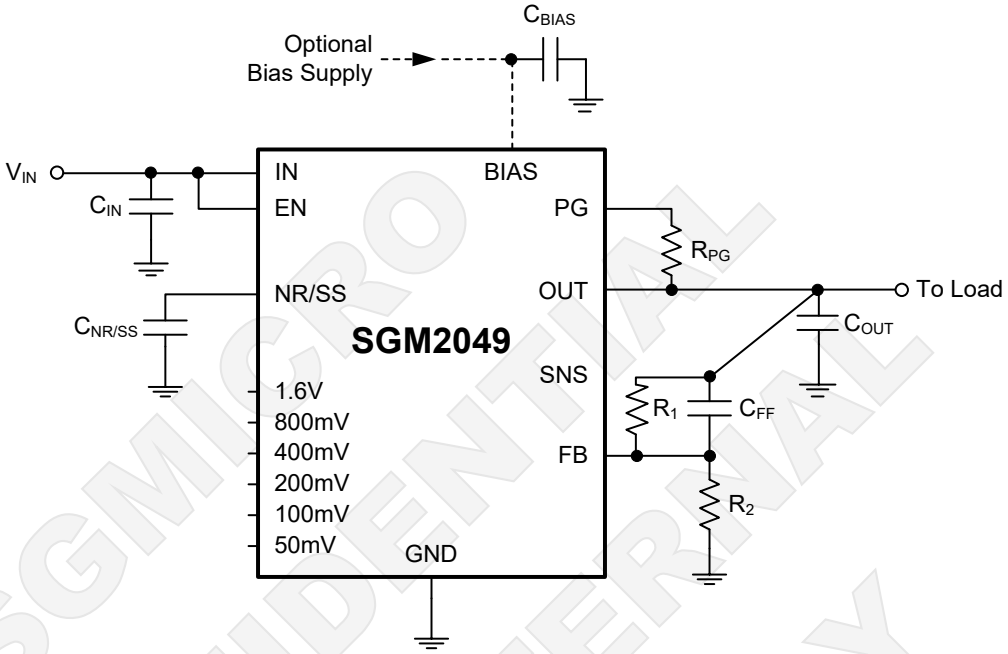

Figure 4. Adjustable Operation

R_1 and R_2 can be calculated for any output voltage range using Equation 1. This resistive network must provide a current equal to or greater than 5μA for DC accuracy. It is recommended to use an R_1 approximately 12kΩ to optimize the noise and PSRR.

$$V_{OUT} = V_{NR/SS} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Table 2 shows the resistor combinations required to achieve several common rails using standard 1% tolerance resistors.

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APPLICATION INFORMATION (continued)

Table 2. Recommended Feedback Resistor Values

Targeted Output Voltage (V)	Feedback Resistor Values		Calculated Output Voltage (V)
	R_1 (kΩ)	R_2 (kΩ)	
0.9	12.4	100	0.899
0.95	12.4	66.5	0.949
1	12.4	49.9	0.999
1.1	12.4	33.2	1.099
1.2	12.4	24.9	1.198
1.5	12.4	14.3	1.494
1.8	12.4	10	1.798
1.9	12.1	8.87	1.890
2.5	12.4	5.9	2.480
2.85	12.1	4.75	2.838
3	12.1	4.42	2.990
3.3	11.8	3.74	3.324
3.6	12.1	3.48	3.582
4.5	11.8	2.55	4.502
5	12.4	2.37	4.985

NOTE: R_1 is connected from OUT pin to FB pin; R_2 is connected from FB pin to GND.

Pin-Selectable Programmable Output Voltage

Pin-selectable programmable output voltage is achieved with the pin-selectable resistors via pin 2 and pins 5 to 11. Each pin can be connected to ground (active) or left open (floating) or connected to the SNS pin. Pin-selectable programming is set by Equation 2 as the sum of the internal reference voltage ($V_{NR/SS}$ = 0.8V) plus the accumulated sum of the respective voltages assigned to each active pin. Table 3 shows these voltage values associated with each active pin setting for reference. The output is thereby programmed to the minimum possible output voltage equal to V_{FB} by leaving all program pins open or floating.

$$V_{OUT} = V_{NR/SS} + (\Sigma \text{ Pin-Selectable Pins to Ground}) \quad (2)$$

Table 3. Pin-Selectable Programmable Output Voltage

Pin-Selectable Program Pins (Active Low)	Additive Output Voltage Level
Pin 5 (50mV)	50mV
Pin 6 (100mV)	100mV
Pin 7 (200mV)	200mV
Pin 9 (400mV)	400mV
Pin 10 (800mV)	800mV
Pin 11 (1.6V)	1.6V

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APPLICATION INFORMATION (continued)

Table 4 provides a full list of target output voltages and corresponding pin settings when the pin-selectable pins are only tied to ground or left floating. As with the adjustable operation, the output voltage is set according to Equation 3 except that R_1 and R_2 are internally integrated and matched for higher accuracy. Tying any of the pin-selectable pins to SNS can increase the resolution of the internal feedback network by lowering the value of R_1.

$$V_{OUT} = V_{NR/SS} \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

Table 4. User-Configurable Output Voltage Settings

$V_{OUT(NOM)}$ (V)	50mV	100mV	200mV	400mV	800mV	1.6V
0.80	Open	Open	Open	Open	Open	Open
0.85	GND	Open	Open	Open	Open	Open
0.90	Open	GND	Open	Open	Open	Open
0.95	GND	GND	Open	Open	Open	Open
1.00	Open	Open	GND	Open	Open	Open
1.05	GND	Open	GND	Open	Open	Open
1.10	Open	GND	GND	Open	Open	Open
1.15	GND	GND	GND	Open	Open	Open
1.20	Open	Open	Open	GND	Open	Open
1.25	GND	Open	Open	GND	Open	Open
1.30	Open	GND	Open	GND	Open	Open
1.35	GND	GND	Open	GND	Open	Open
1.40	Open	Open	GND	GND	Open	Open
1.45	GND	Open	GND	GND	Open	Open
1.50	Open	GND	GND	GND	Open	Open
1.55	GND	GND	GND	GND	Open	Open
1.60	Open	Open	Open	Open	GND	Open
1.65	GND	Open	Open	Open	GND	Open
1.70	Open	GND	Open	Open	GND	Open
1.75	GND	GND	Open	Open	GND	Open
1.80	Open	Open	GND	Open	GND	Open
1.85	GND	Open	GND	Open	GND	Open
1.90	Open	GND	GND	Open	GND	Open
1.95	GND	GND	GND	Open	GND	Open
2.00	Open	Open	Open	GND	GND	Open
2.05	GND	Open	Open	GND	GND	Open
2.10	Open	GND	Open	GND	GND	Open
2.15	GND	GND	Open	GND	GND	Open
2.20	Open	Open	GND	GND	GND	Open
2.25	GND	Open	GND	GND	GND	Open
2.30	Open	GND	GND	GND	GND	Open
2.35	GND	GND	GND	GND	GND	Open
2.40	Open	Open	Open	Open	Open	GND
2.45	GND	Open	Open	Open	Open	GND
2.50	Open	GND	Open	Open	Open	GND
2.55	GND	GND	Open	Open	Open	GND
2.60	Open	Open	GND	Open	Open	GND
2.65	GND	Open	GND	Open	Open	GND
2.70	Open	GND	GND	Open	Open	GND
2.75	GND	GND	GND	Open	Open	GND
2.80	Open	Open	Open	GND	Open	GND
2.85	GND	Open	Open	GND	Open	GND
2.90	Open	GND	Open	GND	Open	GND
2.95	GND	GND	Open	GND	Open	GND
3.00	Open	Open	GND	GND	Open	GND
3.05	GND	Open	GND	GND	Open	GND
3.10	Open	GND	GND	GND	Open	GND
3.15	GND	GND	GND	GND	Open	GND
3.20	Open	Open	Open	Open	GND	GND
3.25	GND	Open	Open	Open	GND	GND
3.30	Open	GND	Open	Open	GND	GND
3.35	GND	GND	Open	Open	GND	GND
3.40	Open	Open	GND	Open	GND	GND
3.45	GND	Open	GND	Open	GND	GND
3.50	Open	GND	GND	Open	GND	GND
3.55	GND	GND	GND	Open	GND	GND
3.60	Open	Open	Open	GND	GND	GND
3.65	GND	Open	Open	GND	GND	GND
3.70	Open	GND	Open	GND	GND	GND
3.75	GND	GND	Open	GND	GND	GND
3.80	Open	Open	GND	GND	GND	GND
3.85	GND	Open	GND	GND	GND	GND
3.90	Open	GND	GND	GND	GND	GND
3.95	GND	GND	GND	GND	GND	GND

NOTE: For output voltages greater than 3.95V, use a traditional adjustable configuration.

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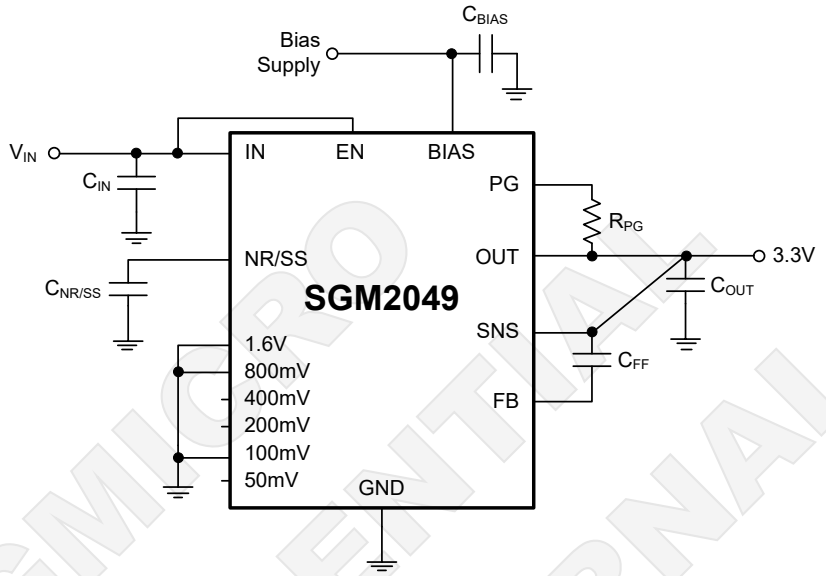
APPLICATION INFORMATION (continued)

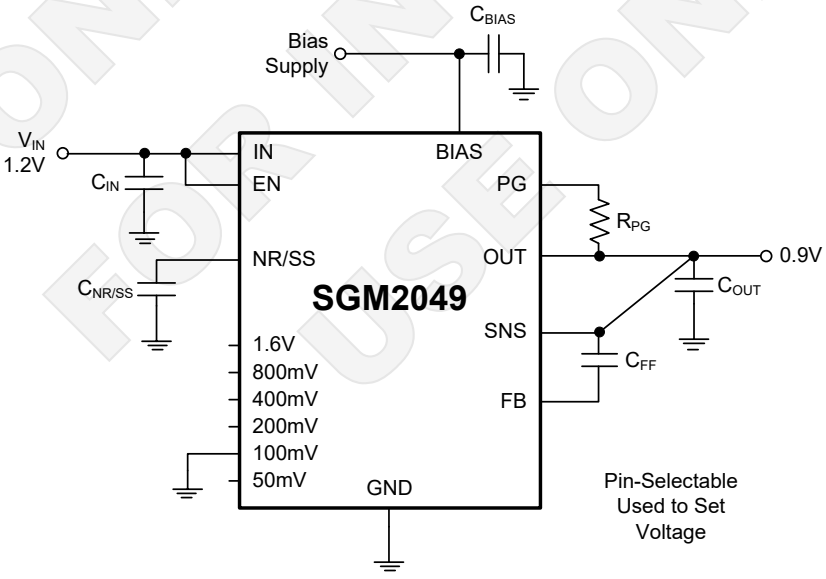
Pin-Selectable Operation

As shown in Figure 5, when grounded, all control pins add a specific voltage on top of the internal reference voltage ($V_{NR/SS}$ = 0.8V). The output voltage can be calculated by Equation 4 and Equation 5. Figure 5 and Figure 6 show a 0.9V output voltage, respectively, that provides an example of the circuit usage with and without bias voltage.



$$V_{OUT(NOM)} = V_{NR/SS} + 1.6V + 0.8V + 0.1V = 0.8V + 1.6V + 0.8V + 0.1V = 3.3V \quad (4)$$

Figure 5. Pin-Selectable Configuration Circuit (3.3V Output, No External Bias)



$$V_{OUT(NOM)} = V_{NR/SS} + 0.1V = 0.8V + 0.1V = 0.9V \quad (5)$$

Figure 6. Pin-Selectable Configuration Circuit (0.9V Output with Bias)

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APPLICATION INFORMATION (continued)

Input and Output Capacitors (C_{IN}, C_{OUT})

The SGM2049 is designed and characterized for operation with low ESR (Equivalent Series Resistance) ceramic capacitors. A 10μF or larger input ceramic capacitor is recommended. An output capacitor with effective capacitance in the range of 10μF to 1000μF is recommended to ensure the stability of the SGM2049. Place the input and output capacitors as close to the respective input and output pins as possible to minimize trace parasitic and ensure stability.

If the trace inductance from the input supply to the SGM2049 is high, a fast load transient can cause V_{IN} level ringing above the absolute maximum voltage rating which damages the device. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10nF C_{FF} optimizes the transient, noise and PSRR performance. A higher capacitance C_{FF} can be also used; however, the start-up time is longer and the PG signal can incorrectly indicate that the output voltage is settled.

Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The SGM2049 is designed for a programmable, monotonic soft-start time of output rising, and it can be achieved via an external capacitor ($C_{NR/SS}$) on the NR/SS pin. Using an external $C_{NR/SS}$ is recommended for general application. It not only minimizes the inrush current but also helps reduce the noise component from internal reference.

During the monotonic start-up procedure, the error amplifier of the SGM2049 tracks the voltage ramp of the external soft-start capacitor until the voltage approaches the internal reference. The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$) and the internal reference ($V_{NR/SS}$). Soft-start ramp time can be calculated with Equation 6:

$$t_{SS} = \frac{(V_{NR/SS} \times C_{NR/SS})}{I_{NR/SS}} \quad (6)$$

For noise-reduction consideration, the $C_{NR/SS}$ combines conjunction with an internal noise-reduction resistor to form a low-pass filter (LPF, a single-pole filter and the cutoff frequency can be calculated with Equation 7.) and filters out the noise from the internal bandgap reference before it is gained up with the error amplifier, thus reducing the total device noise floor. The typical value of $R_{NR/SS}$ is 250kΩ. For low-noise applications, a 10nF to 1μF $C_{NR/SS}$ is recommended.

$$f_{CUTOFF} = \frac{1}{(2 \times \pi \times R_{NR/SS} \times C_{NR/SS})} \quad (7)$$

Sequencing Requirements

There is no sequencing requirement between the BIAS, IN and EN pins.

Reverse Current Protection

As with most LDOs, the SGM2049 can be damaged by excessive reverse current. If the reverse current flow gets high enough, a latch-up condition can be entered. If the maximum V_{OUT} exceeds V_{IN} + 0.3V, that may induce reverse current from V_{OUT} to V_{IN} which flows through the body diode of pass element instead of the normal conducting channel. In this case, the pass element may be damaged. For example, the output is biased above input supply voltage level or input supply has instant collapse at light load operation that makes $V_{IN} < V_{OUT}$.

As shown in Figure 7, an external Schottky diode can be added to prevent the pass element from being damaged by the reverse current. If excessive reverse current flow is expected in the application, an external Schottky diode must be added as Figure 7.

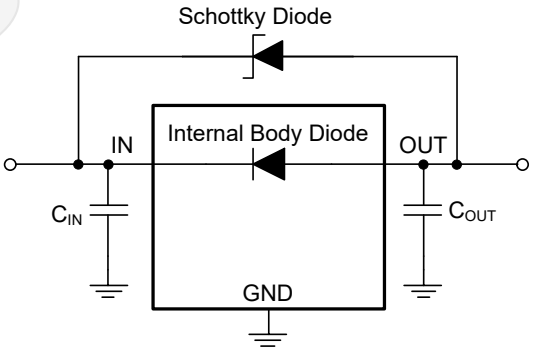

Figure 7. Example Circuit for Reverse Current Protection Using a Schottky Diode

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APPLICATION INFORMATION (continued)

Thermal Considerations and Power Dissipation (P_D)

Thermal protection limits power dissipation in the SGM2049. Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB) and correct sizing of the thermal plane. As a first-order approximation, P_D can be approximated using Equation 8:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (8)$$

An important note is that power dissipation can be minimized input-to-output voltage. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. The ground plane should be connected by a wide copper surface for good thermal dissipation.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction to ambient thermal resistance (θ_{JA}) of the combined PCB, device package and the temperature of the ambient air (T_A), according to Equation 9.

$$T_J = T_A + \theta_{JA} \times P_D \quad (9)$$

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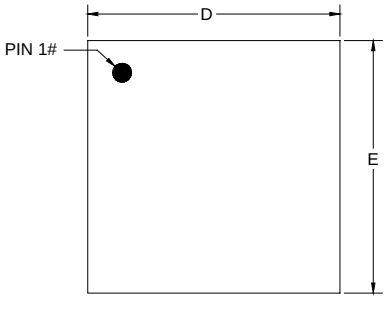
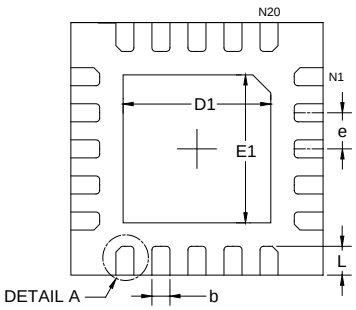
PACKAGE OUTLINE DIMENSIONS

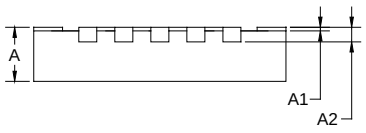
TQFN-3.5×3.5-20L



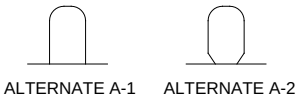
TOP VIEW



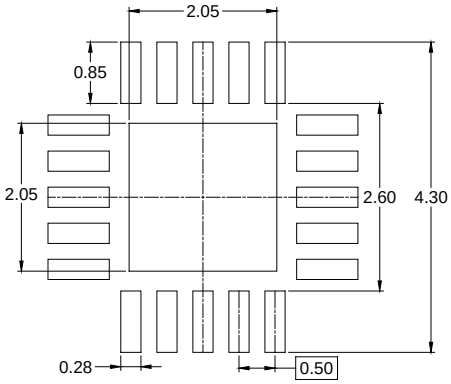
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



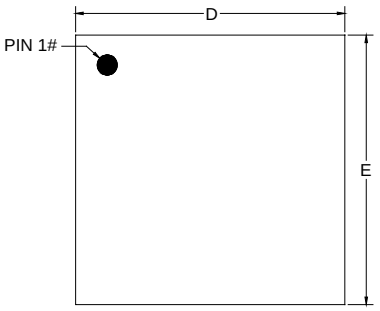
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	-	-	0.050
A2	0.203 REF		
D	3.450	3.500	3.550
D1	2.000	2.050	2.100
E	3.450	3.500	3.550
E1	2.000	2.050	2.100
b	0.200	0.250	0.300
e	0.500 BSC		
L	0.350	0.400	0.450

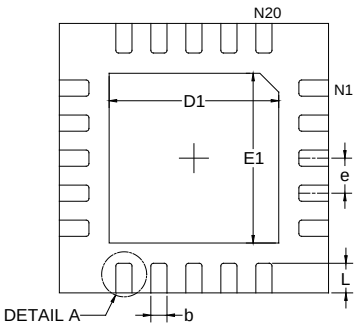
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

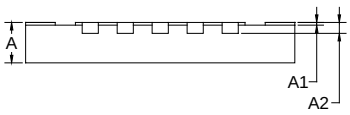
TQFN-5×5-20L



TOP VIEW

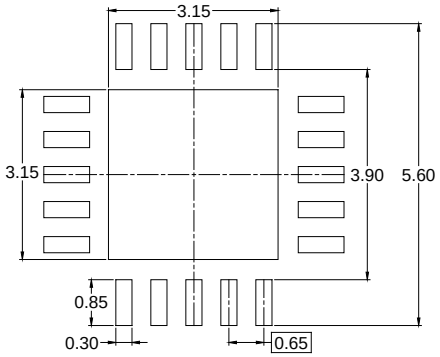


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



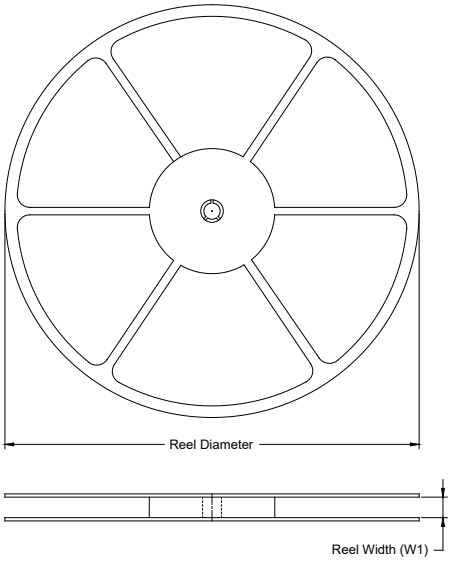
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
D	4.950	5.000	5.050
D1	3.100	3.150	3.200
E	4.950	5.000	5.050
E1	3.100	3.150	3.200
b	0.250	0.300	0.350
e	0.650 BSC		
L	0.500	0.550	0.600

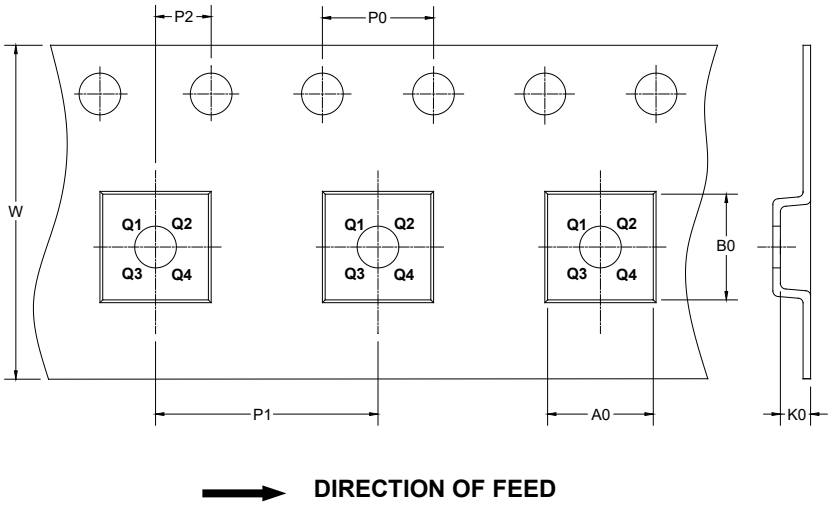
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



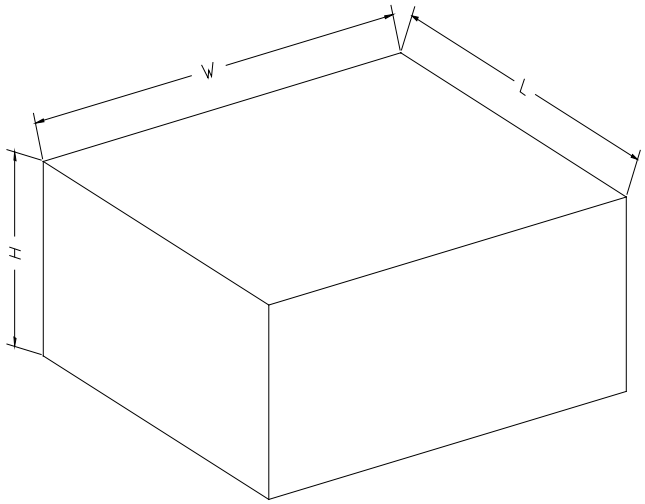
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5×3.5-20L	13″	12.4	3.80	3.80	0.95	4.0	8.0	2.0	12.0	Q2
TQFN-5×5-20L	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002