SGM2048
1A, Low Noise, Wide Bandwidth, High PSRR, Low Dropout Linear Regulator

GENERAL DESCRIPTION

The SGM2048 is a single output low dropout voltage regulator (LDO) designed for applications requiring very low dropout voltage and ultra-high power supply ripple rejection at up to 1A output current.

An advanced BiCMOS process and a PMOSFET pass device are utilized for this product to achieve the best in class analog performance and overall value with just a 4.7μF ceramic output capacitor. The SGM2048 operates over a wide input voltage range of 2.2V to 7V. The output voltage can be programmed from 0.8V to 6V.

The SGM2048 is available in a Green TDFN-3×3-8CL package. It operates over an operating temperature range of -40℃ to +125℃.

FEATURES

- **1A Low Dropout Regulator with Enable**
- **Very Low Dropout: 140mV (TYP) at 1A**
- **Adjustable Output Voltage Range: 0.8V to 6V**
- **Fixed Output Voltages: 0.8V to 6V**
- **Wide Bandwidth, High PSRR:**
  - **75dB at 1kHz**
  - **60dB at 100kHz**
  - **50dB at 1MHz**
- **Low Noise: 27μV_{RMS} (TYP) (100Hz to 100kHz)**
- **Stable with a 4.7μF Ceramic Capacitor**
- **Excellent Load and Line Transient Responses**
- **Over-Current and Over-Temperature Protection**
- **Available in a Green TDFN-3×3-8CL Package**

APPLICATIONS

Telecom Infrastructure

Audio

High-Speed I/F (PLL/VCO)

TYPICAL APPLICATION

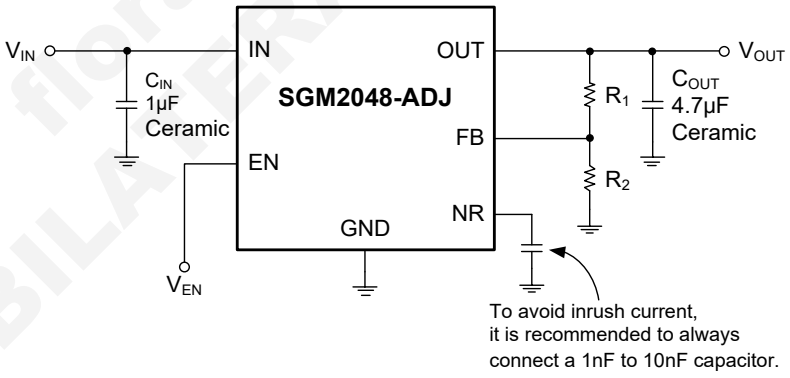


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2048-5.0	TDFN-3×3-8CL	-40℃ to +125℃	SGM2048-5.0XTEK8G/TR	SGMRB0 XTEK8 XXXXX	Tape and Reel, 4000
SGM2048-ADJ	TDFN-3×3-8CL	-40℃ to +125℃	SGM2048-ADJXTEK8G/TR	SGMRAF XTEK8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

X X X X X

- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range .... -0.3V to 8V
FB, NR Voltage Range .... -0.3V to 3.6V
EN Voltage Range .... -0.3V to Min (V_{IN} + 0.3V, 7V)
OUT Voltage Range... -0.3V to 8V
OUT Current .... Internally Limited
Package Thermal Resistance
TDFN-3×3-8CL, θ_{JA} .... 53℃/W
Junction Temperature...+150℃
Storage Temperature Range ....-65℃ to +150℃
Lead Temperature (Soldering, 10s) ....+260℃

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} (1) ....2.2V to 7V
Adjustable Output Voltage Range...........................0.8V to 6V
Fixed Output Voltage Range..................................0.8V to 6V
Output Current Range, I_{OUT} ....0A to 1A
Operating Temperature Range ....-40℃ to +125℃
Input Capacitance, C_{IN} .... 1μF (MIN)
Output Capacitance, C_{OUT} ....4.7μF to 100μF

NOTE:
1. Minimum V_{IN} = V_{OUT} + V_{DROP} or 2.2V, whichever is greater.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

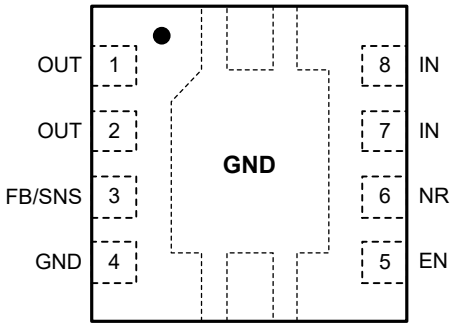
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-3×3-8CL

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1, 2	OUT	O	Regulator Output. A 4.7μF or larger capacitor of any type is required for stability.
3	FB	I	Feedback Pin (adjustable voltage version only). This pin is the Input to the control loop error amplifier and is used to set the output voltage of the device.
	SNS		Output Voltage Sense Input Pin (fixed voltage version only) (1).
4	GND	–	Ground.
5	EN	I	Enable Pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN if not used and must not be left floating.
6	NR	–	Noise-Reduction Pin. Connect an external capacitor between this pin and ground to reduce output noise to very low levels. Also, the capacitor slows down the VOUT ramp (RC soft-start).
7, 8	IN	I	Input Supply Voltage Pin.
Exposed Pad	GND	–	Exposed Pad. Connect to GND for best thermal performance.

NOTE:

1. In order to minimize the trace resistive drop, connect the SNS pin close to the load and make sure that the trace inductance to the load is also minimized.

ELECTRICAL CHARACTERISTICS

(At T_J = -40℃ to +125℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 2.2V, whichever is greater, I_{OUT} = 1mA, V_{EN} = 2.2V, C_{IN} = 1μF, C_{OUT} = 4.7μF and C_{NR} = 0.01μF. For SGM2048-ADJ, tested at V_{OUT} = 0.8V and V_{OUT} = 6V. Typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Internal Reference	V_{NR}	SGM2048-ADJ		+25℃		0.8		V
Output Voltage	V_{OUT}	SGM2048-ADJ		+25℃	0.8		6	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 7V, V_{IN} ≥ 2.2V, I_{OUT} = 100mA		+25℃		50		μV/V
Load Regulation	$\Delta V_{OUT}/\Delta_{IOUT}$	I_{OUT} = 1mA to 1A		+25℃		1.2		μV/mA
Dropout Voltage	V_{DROP}	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 6.5V, V_{IN} = 2.2V, V_{FB} = GND	I_{OUT} = 500mA	+25℃		80		mV
			I_{OUT} = 750mA	+25℃		115		
			I_{OUT} = 1A	+25℃		150		
		V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 6.5V, V_{IN} = 7V, V_{FB} = GND	I_{OUT} = 500mA	+25℃		70		mV
			I_{OUT} = 750mA	+25℃		100		
			I_{OUT} = 1A	+25℃		140		
Ground Pin Current	I_{GND}	I_{OUT} = 1mA		+25℃		80		μA
		I_{OUT} = 1A		+25℃		950		
Shutdown Current (I_{GND})	I_{SHDN}	V_{EN} ≤ 0.4V, V_{IN} = 7V, R_L = 1kΩ		+25℃		0.84		μA
Feedback Pin Current	I_{FB}	V_{IN} = 6.5V, V_{FB} = 0.8V		+25℃		0.02		μA
Power Supply Rejection Ratio	PSRR	V_{IN} = 4.3V, $V_{OUT(NOM)}$ = 3.3V, I_{OUT} = 750mA, C_{NR} = 10nF	f = 100Hz	+25℃		75		dB
			f = 1kHz	+25℃		75		
			f = 10kHz	+25℃		70		
			f = 100kHz	+25℃		60		
			f = 1MHz	+25℃		50		
Output Noise Voltage	e_n	BW = 100Hz to 100kHz, V_{IN} = 4.3V, $V_{OUT(NOM)}$ = 3.3V, I_{OUT} = 100mA	C_{NR} = 1nF	+25℃		56		$μV_{RMS}$
			C_{NR} = 10nF	+25℃		28		
			C_{NR} = 100nF	+25℃		27		
Enable High (Enabled)	$V_{EN(HI)}$	2.2V < V_{IN} ≤ 6.5V, R_L = 1kΩ		+25℃	1.2			V
Enable Low (Shutdown)	$V_{EN(LO)}$	R_L = 1kΩ		+25℃			0.4	V
Enable Pin Current, Enabled	$I_{EN(HI)}$	V_{IN} = V_{EN} = 7V		+25℃		0.45		μA
Start-Up Time	t_{STR}	$V_{OUT(NOM)}$ = 3.3V, V_{OUT} = 0%-90%$V_{OUT(NOM)}$, R_L = 3.3kΩ, C_{OUT} = 4.7μF	C_{NR} = 1nF	+25℃		0.2		ms
			C_{NR} = 10nF	+25℃		1.6		
Under-Voltage Lockout	UVLO	V_{IN} rising, R_L = 1kΩ		+25℃		2		V
UVLO Hysteresis		V_{IN} falling, R_L = 1kΩ		+25℃		85		mV
Thermal Shutdown Temperature	T_{SHDN}					170		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}					20		℃

TYPICAL APPLICATION CIRCUITS

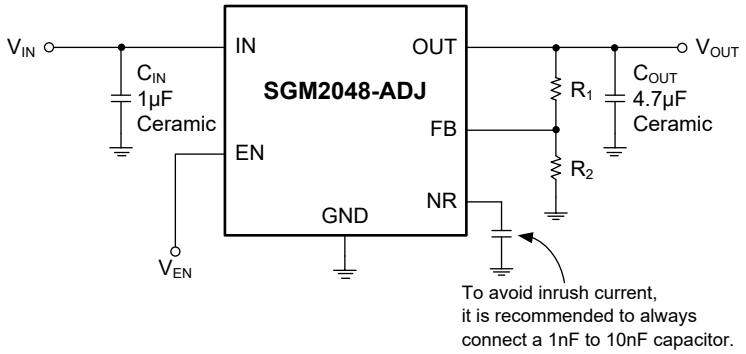


Figure 2. SGM2048 with Adjustable Output Voltage

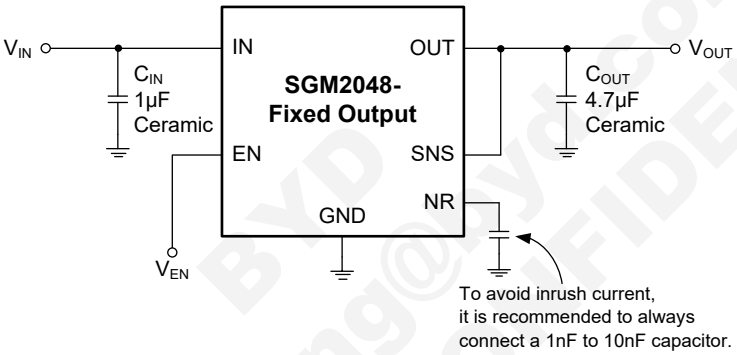


Figure 3. SGM2048 with Fixed Output Voltage

FUNCTIONAL BLOCK DIAGRAM

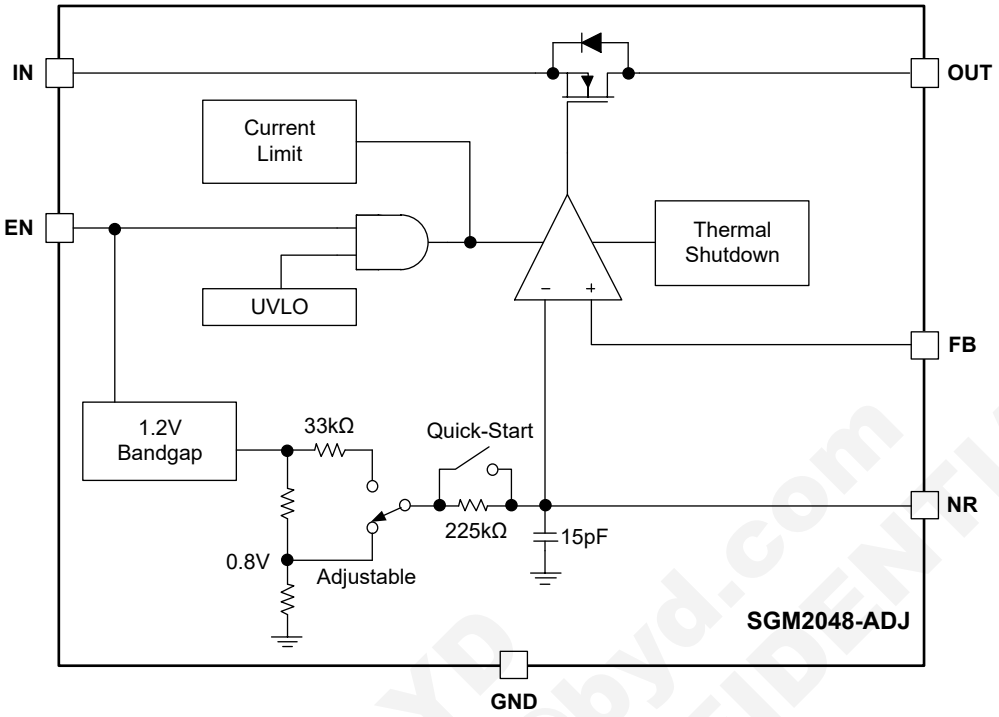


Figure 4. Adjustable Output Voltage Internal Block Diagram

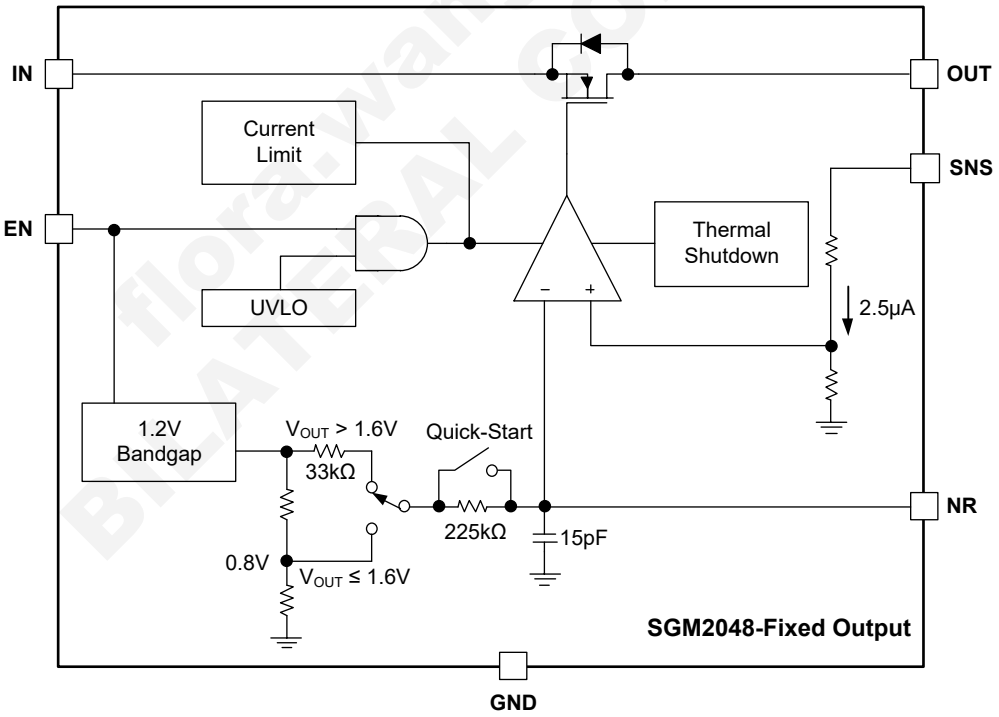


Figure 5. Fixed Output Voltage Internal Block Diagram

DETAILED DESCRIPTION

The SGM2048 is a high current, low dropout voltage regulator designed for applications requiring very low dropout voltage and ultra-high power supply ripple rejection at up to 1A output current. It also equipped with noise-reduction pin for noise sensitive applications. A noise-reduction capacitor at the NR pin decreases noise generated by the bandgap reference to improve PSRR. The internal compensation network is well designed to achieve fast transient response with good stability. The SGM2048 offers sub-bandgap output voltages, current limit and thermal protection and is fully specified from -40℃ to +125℃.

Internal Current Limit

The internal current limit circuit incorporates protection against over-current due to any short or overload condition applied to the output pin. In the event of an overload condition, the LDO may begin to cycle on and off due to the die temperature exceeding thermal fault condition and subsequently cooling down after the power device is turned off. For reliable operation, do not operate the device in a current limit state for extended periods of time.

The SGM2048 has a built-in body diode that conducts current when the voltage at OUT pin exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting is required.

Shutdown

The enable pin (EN) is active high. The SGM2048 goes into shutdown mode when the EN pin is in a logic low condition. If the shutdown mode is not required, the EN pin can be directly tied to IN pin to keep the LDO on.

Start-Up

The SGM2048 has a quick-start circuit to charge the noise-reduction capacitor (C_{NR}). The switch of the quick-start circuit is closed at start-up. To reduce the noise from bandgap, there is a low-pass (RC) filter consists of the C_{NR} and the resistance which is connected with bandgap, as shown in Functional Block Diagram. At the start-up, the quick-start switch is closed, with only 33kΩ resistance between bandgap and NR pin. The quick-start switch opens approximate 2ms after the device is enabled; the resistance between NR and bandgap is approximately 250kΩ to form a very good low-pass (RC) filter. This low-pass filter achieves very good noise-reduction for the reference voltage. It is recommended the C_{NR} value larger than 0.01μF to reduce noise, and low leakage ceramic capacitors are suitable. However, with too large C_{NR} will extend the start-up time. That is, if C_{NR} is not fully charged during this 2ms period, C_{NR} finishes charging through a higher resistance of 250kΩ and takes much longer to fully charge.

Under-Voltage Lockout (UVLO)

The SGM2048 utilizes an under-voltage lockout circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature on the input, and it typically ignores under-shoot transients if they are less than 50μs duration.

Device Functional Modes

EN pin driving is to control device function mode. When the EN pin is over 1.2V for V_{IN} from 2.2V to 7V, the regulator turns on. When the EN pin is below 0.4V, it causes the regulator to enter shutdown mode. The current consumption of the device is reduced to typically 0.84μA in shutdown mode.

APPLICATION INFORMATION

The required output voltage of adjustable can be adjusted from 0.8V to 6V using two external resistors. Figure 2 gives the connections for the adjustable output version. Figure 3 shows the connections for the fixed voltage version.

Dropout Voltage

The SGM2048 uses a PMOSFET pass transistor to achieve low dropout. When (V_{IN} - V_{OUT}) is less than the dropout voltage (V_{DROP}) as with any linear regulator, PSRR and transient responses are degraded as (V_{IN} - V_{OUT}) approaches dropout. For normal operation, the suggested LDO operating range is (V_{IN} > V_{OUT} + V_{DROP}) for good transient responses and PSRR ability.

Minimum Load

The SGM2048 employs an innovative low-current mode circuit which increase loop gain under very light or no-load conditions, this benefits the result of output voltage regulation performance down to zero output current. The SGM2048 is stable with no output load.

Input and Output Capacitor Requirements

Like any low dropout regulator, the external capacitors of the SGM2048 must be carefully selected for regulator stability and performance. This capacitor counteracts reactive input sources and improves transient response, noise rejection and ripple rejection. If source impedance is not sufficiently low, a 1μF input capacitor may be necessary to provide stability. Any good quality ceramic capacitor can be used across the input supply near the regulator. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response.

The SGM2048 is designed to be stable with standard ceramic output capacitors of 4.7μF or greater of capacitance. The device is evaluated using a 4.7μF ceramic capacitor of 10V rating, 10% tolerance, X5R type and 0805 size (2mm × 1.25mm).

X5R and X7R type capacitors are highly recommended because they have minimal variation in value and ESR over-temperature. Maximum ESR should be less than 0.5Ω.

The SGM2048 implements an innovative internal compensation circuit that does not require a feedback capacitor across R_2 for stability. Do not use a feedback capacitor for this device.

Detailed Design Procedure

The output voltage is determined by the ratio of FB reference. The values of R_1 and R_2 on the FB pin can be calculated for any voltage using the formula as below:

$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \times 0.800$$

For common output voltages, sample resistor values are shown in Table 1. In Table 1, E96 series resistors are used and all values meet 1% of the target V_{OUT}, assuming resistors with zero error. Using lower values for R_1 and R_2 reduces the noise injected from the FB pin.

Table 1. Sample 1% Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
0.8V	0Ω (Short)	Do not populate
1V	2.49kΩ	10kΩ
1.2V	4.99kΩ	10kΩ
1.5V	8.87kΩ	10kΩ
1.8V	12.5kΩ	10kΩ
2.5V	21kΩ	10kΩ
3.3V	30.9kΩ	10kΩ
5V	52.3kΩ	10kΩ

Output Noise

For most LDOs, the dominant noise source is from the internal bandgap. With the noise-reduction capacitor connecting to the NR pin of the SGM2048, the bandgap does not contribute significantly to noise. Instead, the most noise source comes from the output resistor divider and the error amplifier input. For general application to minimize noise, using a 0.01μF noise-reduction capacitor (C_{NR}) is recommended.

Power Supply Recommendations

The SGM2048 is designed to operate with an input voltage supply range from 2.2V to 7V. Due to the nature of an LDO, V_{IN} must be some margin higher than V_{OUT} plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from VIN to VOUT. Additional input capacitors with low ESR can help improve the output noise performance.

APPLICATION INFORMATION (continued)

Layout Guidelines

The performances of this LDO depend greatly on the care taken in designing the PC board. For good PSRR, output noise and transient response performance, it's recommended to design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Thermal Considerations

Thermal protection disables the output when the junction temperature exceeds +170℃. The internal pass element then turns off. The pass element turns on again after the junction temperature cools down by 20℃. Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink.

The thermal protection circuit may cycle on and off to limit the dissipation of the regulator, protecting it from overheating damage.

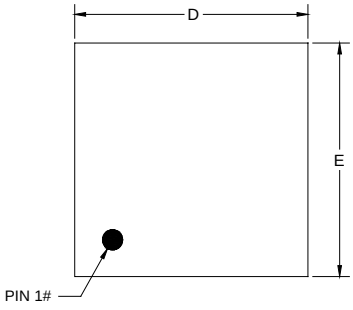
For good reliability, thermal protection should trigger at least 35℃ above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125℃ at the highest expected ambient temperature and worst-case load. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For reliable operation, junction temperature should be limited to +125℃ maximum.

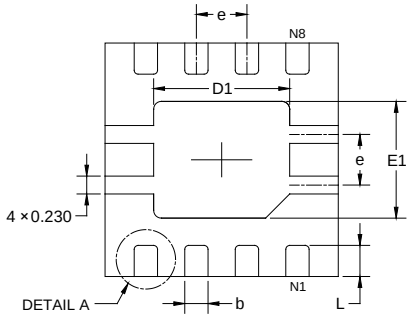
The internal protection circuitry of the SGM2048 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the SGM2048 into thermal shutdown degrades device reliability.

PACKAGE OUTLINE DIMENSIONS

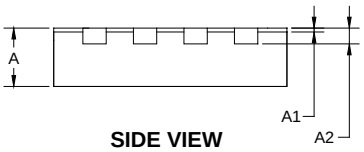
TDFN-3×3-8CL



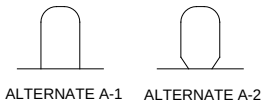
TOP VIEW



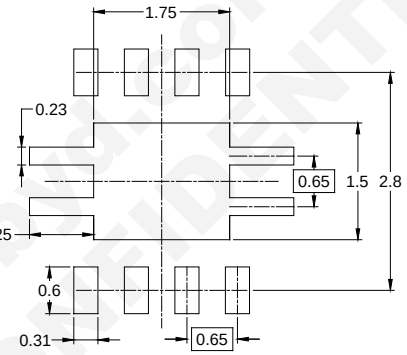
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



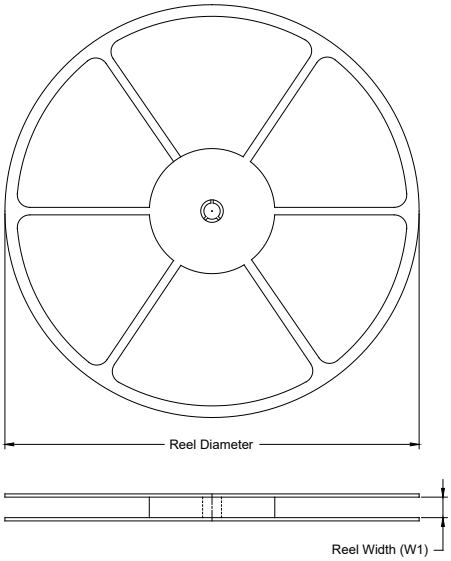
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	-	-	0.050
A2	0.203 REF		
D	2.950	3.000	3.050
D1	1.700	1.750	1.800
E	2.950	3.000	3.050
E1	1.450	1.500	1.550
b	0.250	0.300	0.350
e	0.650 BSC		
L	0.350	0.400	0.450

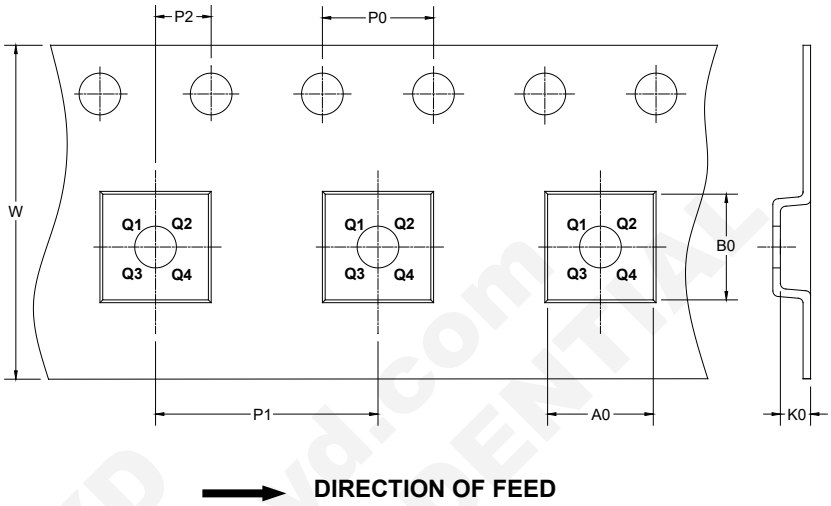
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



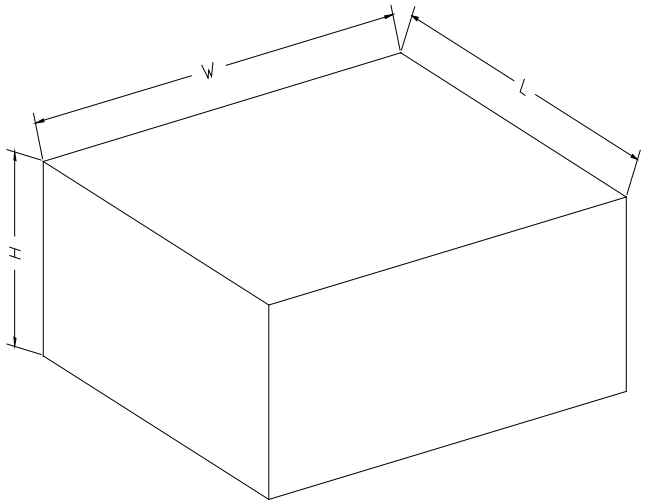
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-8CL	13″	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002