SGM31324
I²C Programmable RGB LED Driver with Auto Blink Mode

GENERAL DESCRIPTION

The SGM31324 is a fully programmable, constant current RGB LED driver with a flexible control interface. The device is ideally powered from 1-cell Lithium-Ion/ Polymer, 3-cell NiCd/NiMH/Alkaline batteries, or systems with 3.3V or 5V supplies. It provides 3 independent programmable constant current sinks without requiring any external components.

With an on-chip timing control unit, LED blink rate, fade-in and fade-out are user-adjustable resulting in unique color lighting patterns.

Ten internal registers are programmed via the I²C control interface with a built-in decoder allowing individual control of the LED channels' ON/OFF state and current level. A total of 192 current levels are available for each channel from 0.125mA to 24mA with a 0.125mA step.

An Auto Blink mode automatically turns on and off LED1 (on D1 pin) at 8mA every 2s after EN pin goes high. In this mode, a phone with a discharged battery connected to a charger can have LED1 blink to notify that the battery is charging.

In shutdown mode, the quiescent current is reduced to less than 1μA.

The device is available in Green UTDFN-1.5×1.5-8L package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Ultra Low Dropout Regulated 3-CH Current Sinks**
  - **30mV (TYP) at 10mA per Channel**
- **Programmable LED Setting by I²C Compatible Interface**
- **Individual Channel Control**
  - **ON/OFF Interval Time Control**
  - **Dimming Up/Down Time**
  - **RGB LED Color Control**
- **192 Current-Level Setting**
  - **0.125mA ~ 24mA, 0.125mA Step**
- **Auto Blink LED1 (D1 Pin) Mode**
  - **Blinking Period: 2s**
  - **Current Setting: 8mA**
- **No Noise, Non-Pulsating LED Current**
- **Fast, Smooth Start-Up**
- **Input Voltage Range: 2.5V to 5.5V**
- **Less than 1μA Shutdown Current**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green UTDFN-1.5×1.5-8L Package**

APPLICATIONS

RGB Indicator LEDs
Mobile Phones and Handheld Devices
Digital Cameras

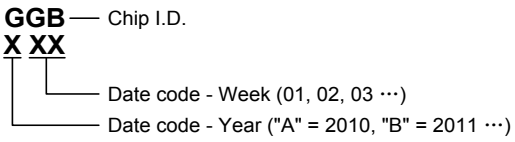
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM31324	UTDFN-1.5×1.5-8L	-40℃ to +85℃	SGM31324YUDW8G/TR	GGB XXX	Tape and Reel, 4000

NOTE: XXX = Date Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

MARKETING INFORMATION



ABSOLUTE MAXIMUM RATINGS

VIN, D1, D2, D3 to GND ..... -0.3V to 6V
EN to GND ..... -0.3V to 6V
SCL, SDA to GND ..... -0.3V to V_{IN} + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering 10 sec) ..... +260℃
ESD Susceptibility
HBM 4000V
MM 400V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.5V to 5.5V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

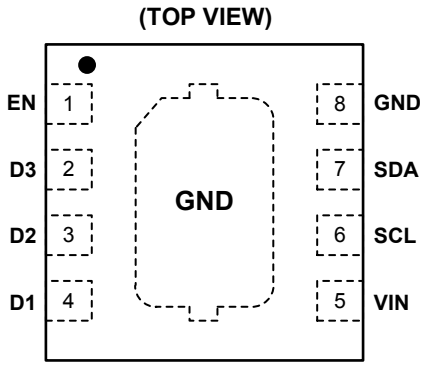
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION



PIN DESCRIPTION

NAME	PIN	TYPE	FUNCTION
EN	1	I	Auto Blink Mode Enable Input Pin. Input logic high to enable the auto blink mode and logic low to disable the auto blink mode. Other functions are not controlled by the EN pin.
D3	2	O	Regulated Output Current Sink D3. Current level and ON/OFF selections are controlled by serial interface.
D2	3	O	Regulated Output Current Sink D2. Current level and ON/OFF selections are controlled by serial interface.
D1	4	O	Regulated Output Current Sink D1. Current level and ON/OFF selections are controlled by serial interface.
VIN	5	P	Input Power for the IC.
SCL	6	I	Clock of the I²C Interface.
SDA	7	I/O	Data of the I²C Interface.
GND	8	G	Ground Pin.
GND	Exposed Pad	—	The exposed pad should be soldered to the ground.

NOTE: I: input; O: output; I/O: input or output; G: ground; P: power for the circuit.

TYPICAL APPLICATION CIRCUITS

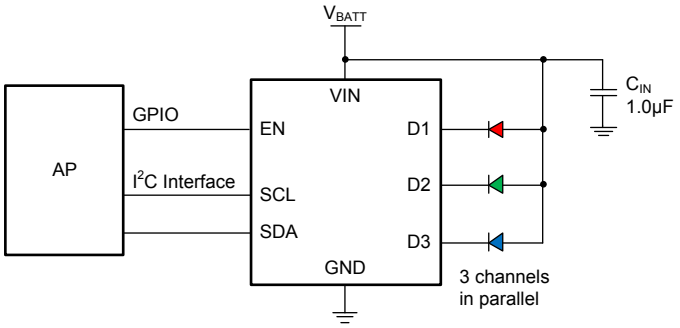


Figure 1. Typical Application Circuit

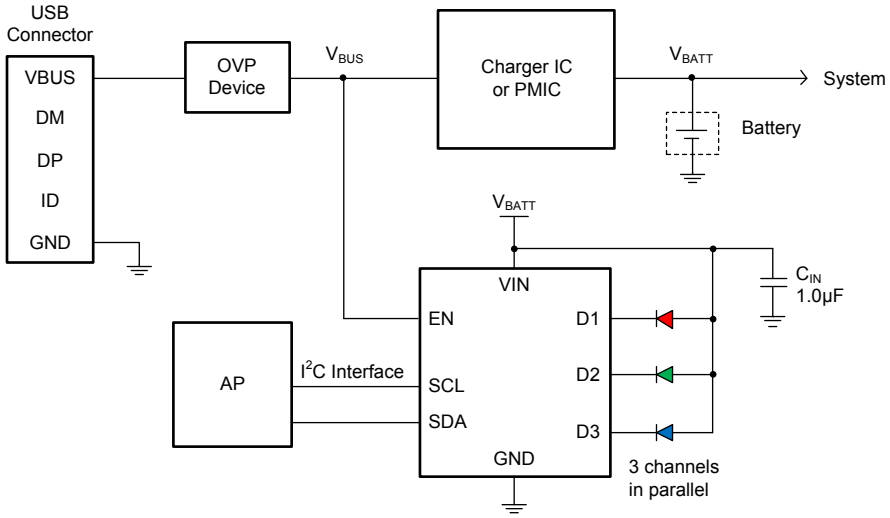


Figure 2. Application Circuit with External Charger and VBUS Detection

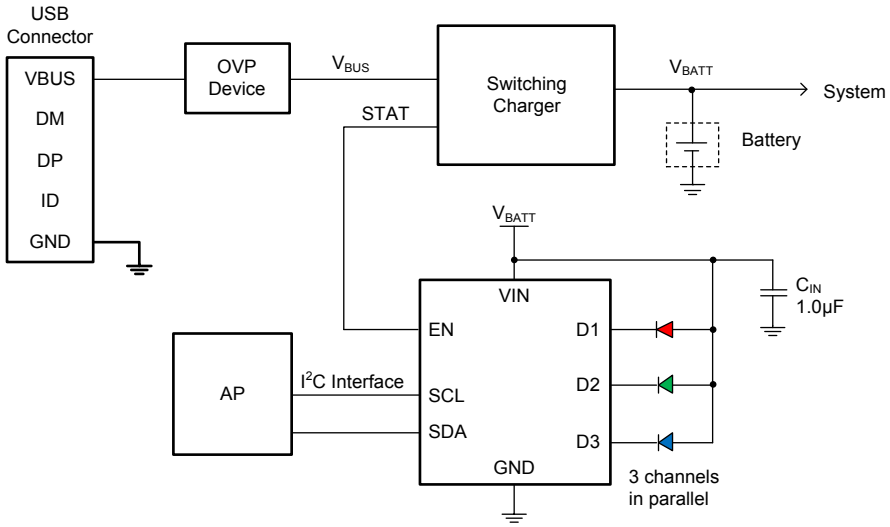


Figure 3. Application Circuit with Internal Charger IC Status Detection

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
POWER SUPPLY							
Input Operating Range	V_{IN}		Full	2.5		5.5	V
Sink Pin (Dx) Dropout Voltage (90% of Nominal Current)	V_{D_MIN}	All channels set to 24mA, Reg6-8 = BFh	+25℃		65	90	mV
Output Current Accuracy		All channels set to 10mA, Reg6-8 = 4Fh	+25℃	-5		5	%
Output Current Matching		Max($\|I_{Dx} - I_{AVG}\|$)/I_{AVG}, all channels set to 10mA, Reg6-8 = 4Fh	+25℃	-5		5	%
Supply Current	I_{IN}	All channels set to 20mA, Reg6-8 = 9Fh	+25℃		280	340	μA
		One channel set to 20mA, other channels off	+25℃		120	150	
Quiescent Current	I_Q	Device on, all LEDs OFF, Reg4 = 0	+25℃		41	52	μA
Shutdown Current	I_{SHDN}	V_{IN} = V_{OUT} = 3.6V, SCL = 0V, SDA = 0V	+25℃		0.3	1	μA
CONTROL AND I²C-COMPATIBLE PIN VOLTAGE SPECIFICATIONS (SCL, SDA) (1)							
Input Logic Low Threshold	V_{IL}	SDA, SCL	+25℃			0.4	V
Input Logic High Threshold	V_{IH}	SDA, SCL	+25℃	1.2			V
I²C-COMPATIBLE TIMING SPECIFICATIONS (SCL, SDA), SEE Figure 4							
SCL (Clock Period)	t_1		+25℃	2.5			μs
Low Period of The SCL Clock	t_2		+25℃	1.3			μs
DATA_IN Setup Time to SCL High	t_3		+25℃	350			ns
DATA_IN Hold Time after SCL Low	t_4		+25℃	0		0.8	μs
DATA_OUT Stable after SCL Low	t_5		+25℃	350			ns
SDA Low Setup Time to SCL Low (Start)	t_6		+25℃	600			ns
SCL High Setup Time to SDA High (Stop)	t_7		+25℃	600			ns
THERMAL SHUTDOWN							
Thermal Shutdown Threshold					140		℃
Thermal Shutdown Hysteresis					15		℃

NOTE:
1. SCL and SDA must be glitch-free in order for proper brightness control to be realized.

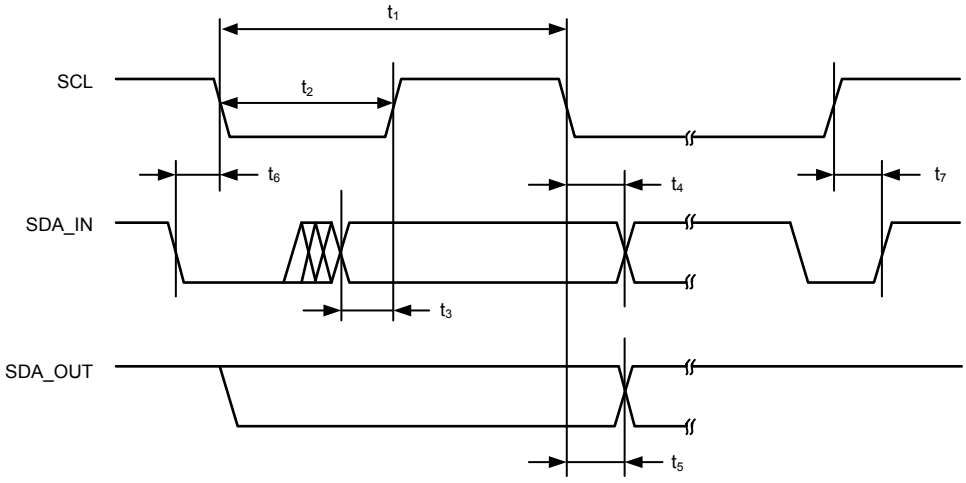
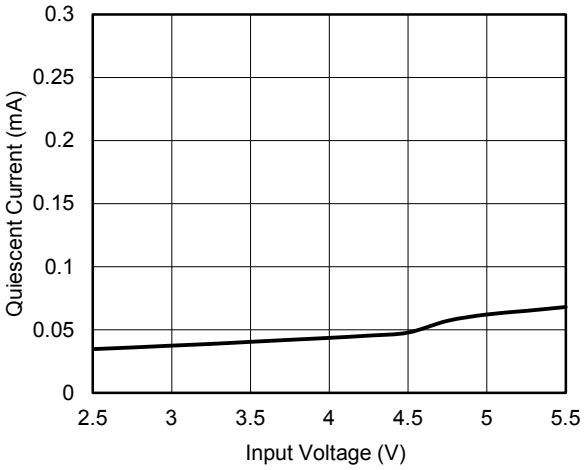


Figure 4. I²C Compatible Interface Timing

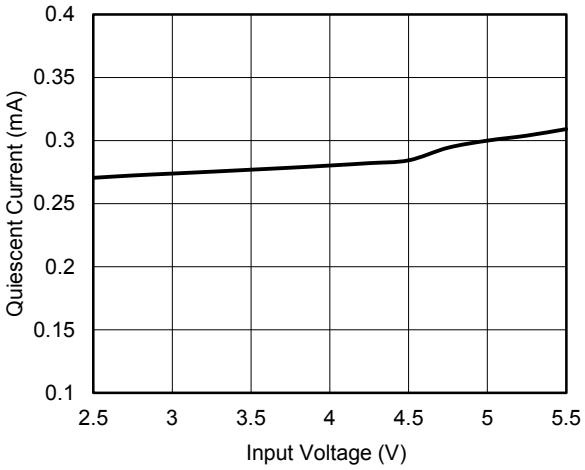
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 3.6V, C_{IN} = 1μF, unless otherwise noted.

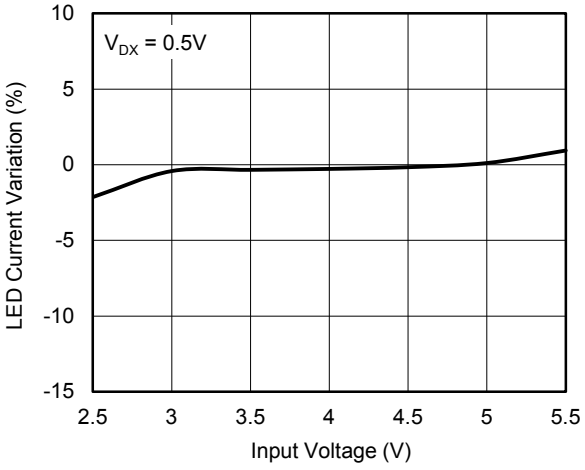
Quiescent Current vs. Input Voltage (LEDs Off)



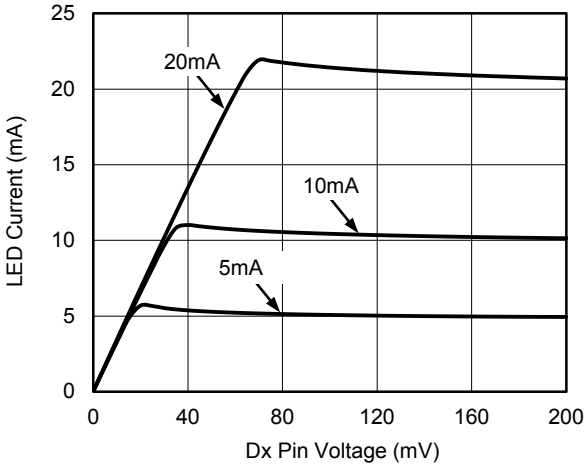
Quiescent Current vs. Input Voltage (LEDs On)



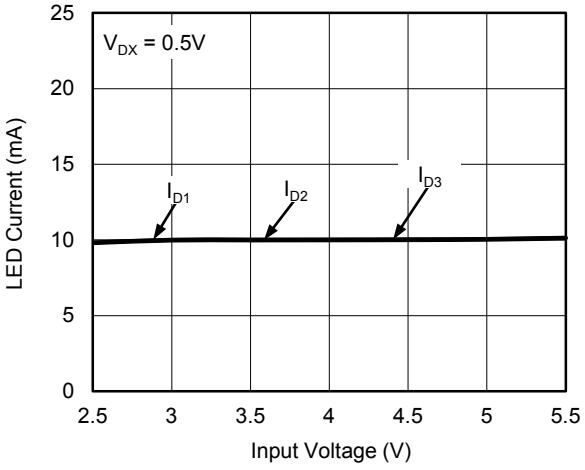
LED Current Variation vs. Input Voltage (at 10mA)



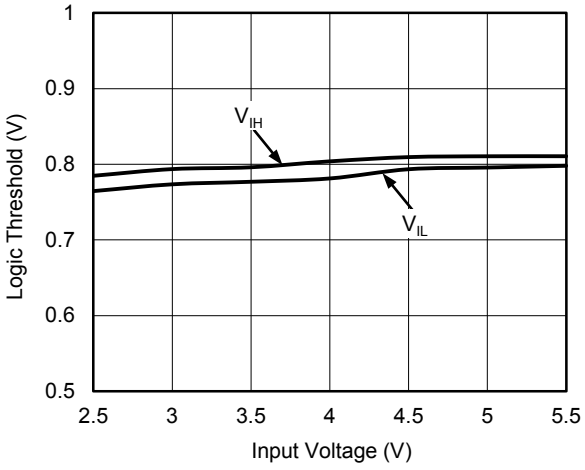
LED Current vs. Dx Pin Voltage



LED Current vs. Input Voltage (10mA per Channel)



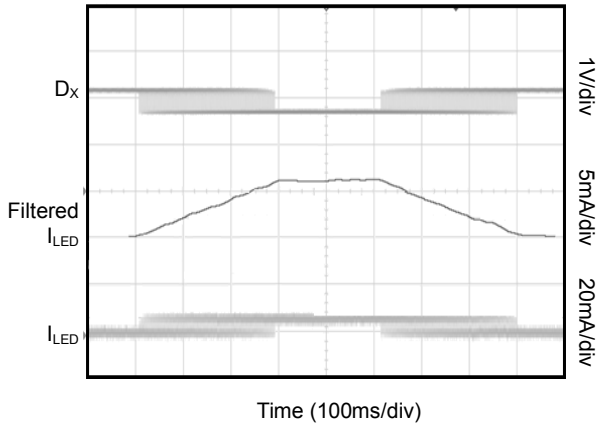
Logic Threshold vs. Input Voltage



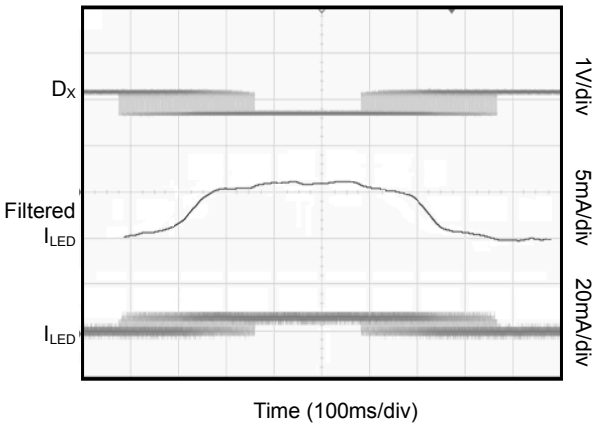
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 3.6V, C_{IN} = 1μF, unless otherwise noted.

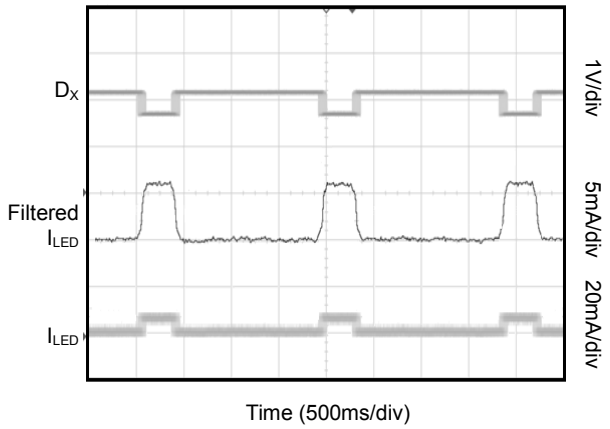
Linear Ramps



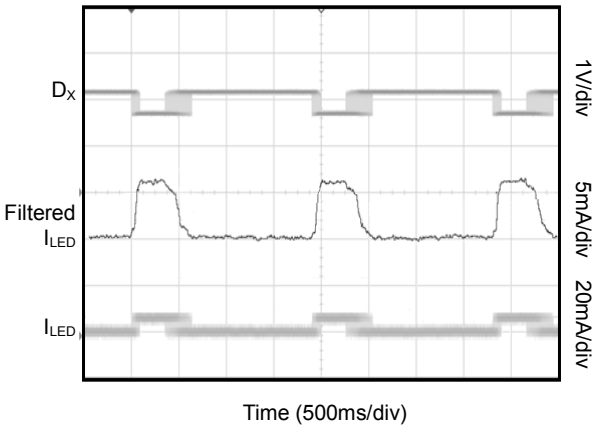
Logarithmic-S Ramps



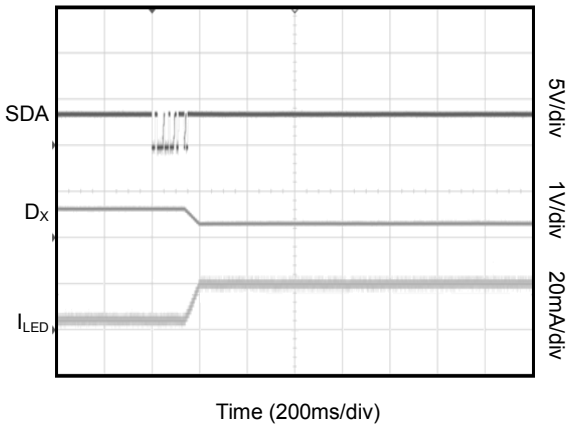
Flashing LED, 2ms Period



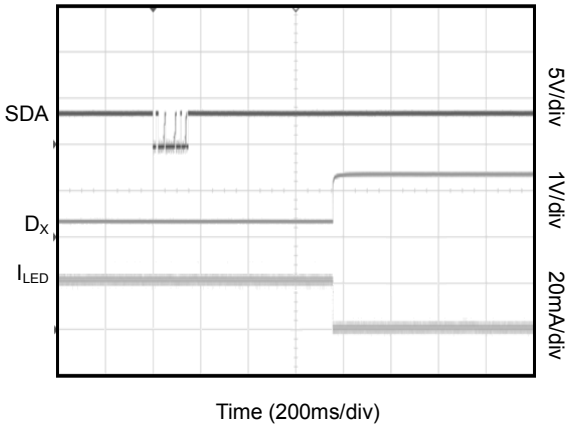
Flashing LED, Extended Falling Ramp



LED Current Transient 5mA to 20mA



Shutdown Mode Delay (Enable Control SDA toggling)



FUNCTIONAL BLOCK DIAGRAM

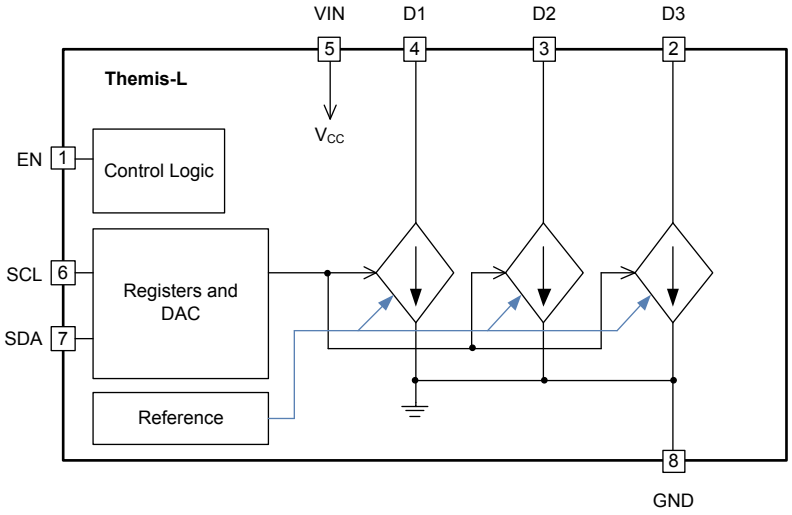


Figure 5. Block Diagram

FUNCTIONAL DESCRIPTION

The SGM31324 is a 3-channel output current sink device, offering constant current regulation with high efficiency and ultra-low internal voltage drop. High integration and small size make it ideal for driving RGB LEDs from a 1-cell Lithium-Ion/Polymer battery. With a wide supply voltage range, SGM31324 is equally suitable for 3- or 4-cell NiCd/NiMH/Alkaline devices or systems with 3.3V or 5V supplies.

The SGM31324 can be programmed via an I²C compatible interface. Each current sink can be configured independently to one of the 192-step current levels or turned off.

LED Current Programming

The individual channel brightness is controlled by the LEDx I_{OUT} registers Reg6 to Reg8. Each channel has a dedicated 8-bit register for setting the current value. The LED channel current is constant, non-pulsating, except when it is being ramped up and down.

The ramp up and down are automatically generated using a PWM scheme where the duty cycle is continuously changing (either increasing or decreasing) to provide a smooth LED current transition between the ON and OFF states. The ramp times, for rise and fall, are separately programmable through an internal ramp register Reg5 with 4 bits for rise and 4 bits for fall. The ramping can be configured to linear or quasi-logarithmic/s-curve by setting register Reg1 bit 7 to 1 or 0 respectively.

Flashing LEDs can be performed by programming the time period (t_{FLASH}) between two consecutive flashes in the flash period register Reg1. Two flash on timer 1/2 registers, Reg2 and Reg3, allow to set the LED on time as a percentage of the flash period. The on time (t_{ON}), shown in Figure 6, includes the ramp-up t_{RISE} and the full on time. Two timer registers are available to support two or more LEDs to flash independently.

Each channel can be configured to timer1 or timer2 with the channel control register Reg4.

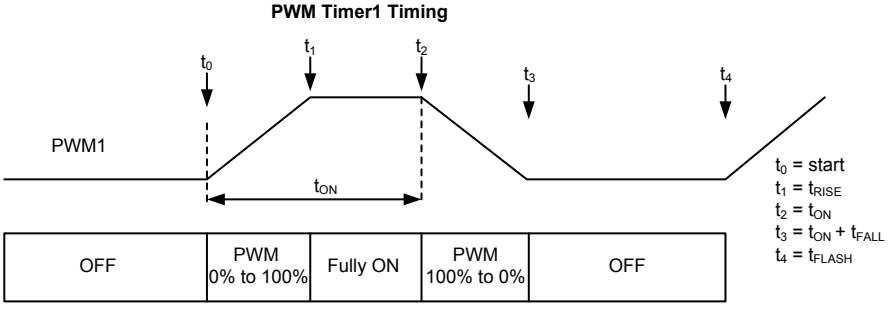


Figure 6. Channel Timing Diagram

FUNCTIONAL DESCRIPTION (continued)

Timer Slot Control

The timing diagrams for the four time slots are illustrated below.

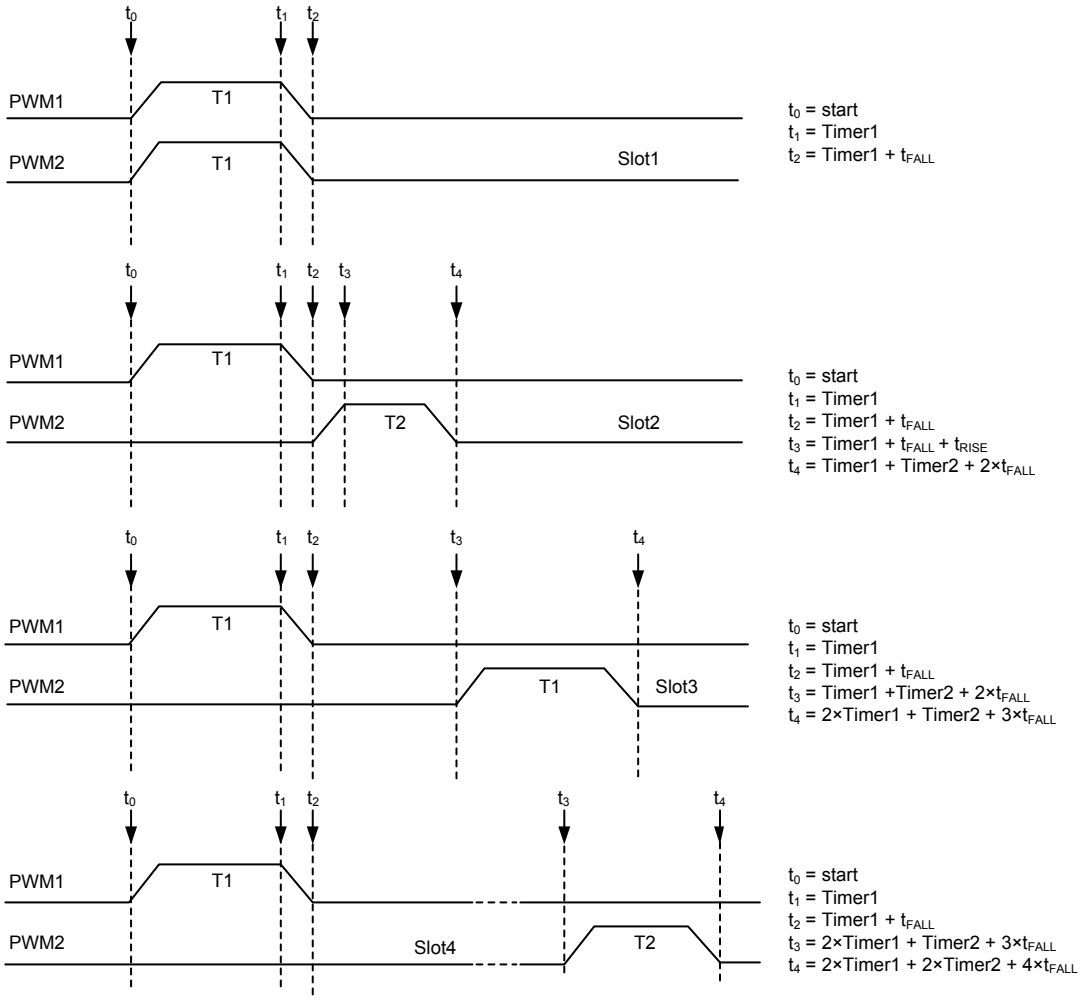
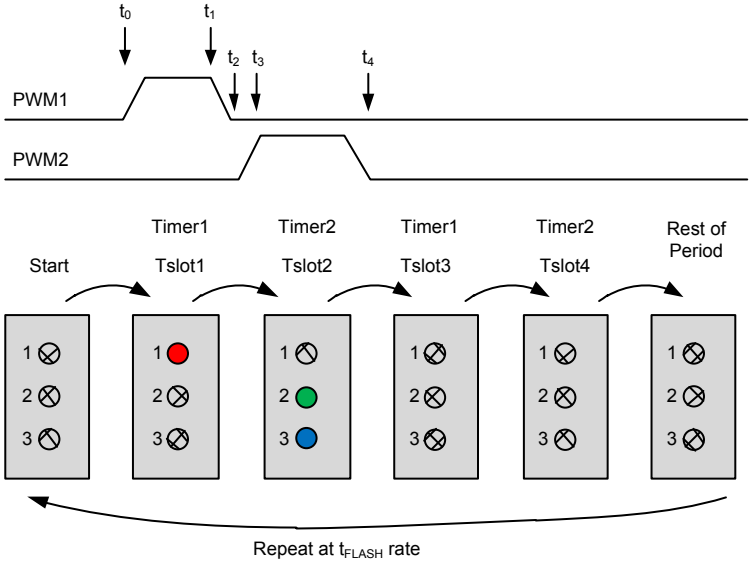


Figure 7. Timer Slot Timing Diagram

FUNCTIONAL DESCRIPTION (continued)



t_0 = start
t_1 = Timer1
t_2 = Timer1 + t_{FALL}
t_3 = Timer1 + t_{FALL} + t_{RISE}
t_4 = Timer1 + Timer2 + 2×t_{FALL}

Channel Control Register:

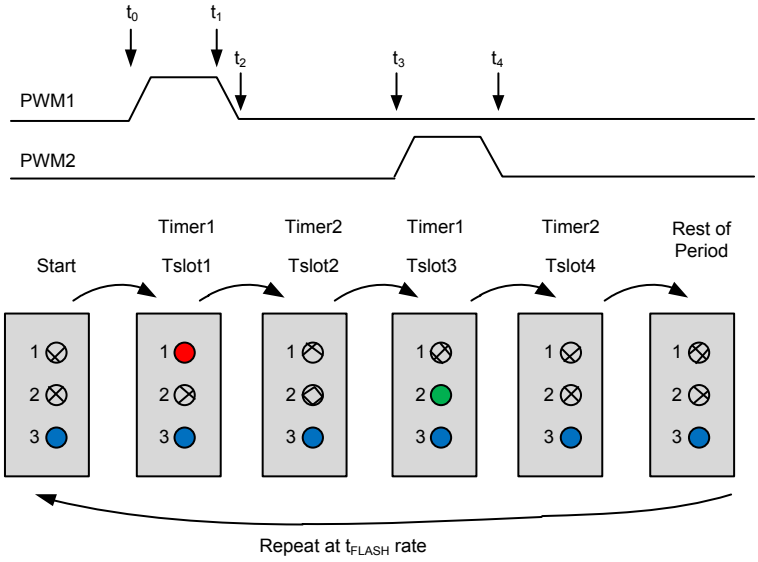
CH1 = 10 => CH1 = PWM1
CH2 = 11 => CH2 = PWM2
CH3 = 11 => CH3 = PWM2

Timer Slot Control Register:

TimerCtrl = 01 => PWM2 = Tslot2

Note: PWM1 is always in Tslot1

Figure 8. Timer Slot2 Example



t_0 = start
t_1 = Timer1
t_2 = Timer1 + t_{FALL}
t_3 = Timer1 + Timer2 + 2×t_{FALL}
t_4 = 2×Timer1 + Timer2 + 3×t_{FALL}

Channel Control Register:

CH1 = 10 => CH1 = PWM1
CH2 = 11 => CH2 = PWM2
CH3 = 01 => CH3 = Always On

Timer Slot Control Register:

TimerCtrl = 10 => PWM2 = Tslot3

Note: PWM1 is always in Tslot1

Figure 9. Timer Slot3 Example

FUNCTIONAL DESCRIPTION (continued)

Each channel can be assigned to one of the 4 timer slots, or always OFF or always ON. The timer slot control register bits define the timing of the second PWM waveform.

The duty cycle of each flash waveform is set by the timer and can be set with 8-bit resolution (256 steps) between 0 and 99.6%. The period of the flash repetition rate can also be set with a 7-bit resolution up to 8 seconds (256ms steps starting at 64ms). The flash repetition period is the same for all outputs. If the programmed total time of the timers exceed the flash repetition rate then the PWM2 slot will be terminated and the timers reset to start position. This may cause the PWM2 signal to be instantly reduced to zero.

Rise/Fall Times

The ramp-up and ramp-down can be linear or S-shaped profile. The S-shape is the default. The ramp-up transitions from 0% to 100% of the I_{SET} value (ON state) and ramp-down to 0% (OFF state).

LED Basic Control

The brightness setting of each channel is internally controlled by 48 current units of 0.5mA. Output current resolution is increased to an effective 0.125mA steps.

REGISTER MAP

Table 1. Register Map

	Reg#	NAME	RESET VALUES
Register Bank	0	Register/Control	0x00
	1	Flash Period	0x00
	2	Flash On Time1	0x81
	3	Flash On Time2	0x01
	4	Channel Control	0x82
	5	Ramp Rate	0x00
	6	LED1 I_{OUT}	0x3F
	7	LED2 I_{OUT}	0x9F
	8	LED3 I_{OUT}	0x9F
	9	Auto Blink	0xAF

RESET/CONTROL: Reg0	
0 (LSB)	Timer Slot Control/ Reset Control
1	
2	Reset/Offset Cancel
3	Enable Ctrl
4	
5	Rise/Fall Scaling
6	
7 (MSB)	Reserved (Test Only)

FLASH PERIOD: Reg1	
0 (LSB)	Flash Period
1	
2	
3	
4	
5	
6	
7 (MSB)	Ramp Linear

FLASH ON TIME1: Reg2	
0	PWM1 Timer Percentage of Period
1	
2	
3	
4	
5	
6	
7	

FLASH ON TIME2: Reg3	
0	PWM2 Timer Percentage of Period
1	
2	
3	
4	
5	
6	
7	

CHANNEL CONTROL: Reg4	
0 (LSB)	LED1 Enable/Timer1/2
1	
2	LED2 Enable/Timer1/2
3	
4	LED3 Enable/Timer1/2
5	
6	Device Enable
7 (MSB)	Not Used

RAMP RATE: Reg5	
0	t_{RISE}
1	
2	
3	
4	t_{FALL}
5	
6	
7	

LED1 I_{OUT}: Reg6	
0	I_{OUT} 0.125mA to 24mA in 0.125mA Steps
1	
2	
3	
4	
5	
6	
7	

LED2 I_{OUT}: Reg7	
0 (LSB)	I_{OUT} 0.125mA to 24mA in 0.125mA Steps
1	
2	
3	
4	
5	
6	
7 (MSB)	

LED3 I_{OUT}: Reg8	
0	I_{OUT} 0.125mA to 24mA in 0.125mA Steps
1	
2	
3	
4	
5	
6	
7	

AUTO BLINK : Reg9	
0	Enable Auto Blink Mode
1	1*
2	1*
3	Not Used
4	
5	
6	
7	Auto Started (Read Only)

REGISTER DESCRIPTION

Reg0 EN/RST

Reg0 [2:0] Timer Slot Control/Reset Control

TCtrl/RESET MODES			
Reg0 [2:0]			Function
D2	D1	D0	
0	0	0	TCtrl: Tslot1
0	0	1	TCtrl: Tslot2
0	1	0	TCtrl: Tslot3
0	1	1	TCtrl: Tslot4
1	0	0	Do Nothing (Bit Cleared)
1	0	1	Reset Registers Only
1	1	0	Reset Main Digital Only
1	1	1	Reset Complete Chip

After power-up or V_{IN} dropping below 2.5V, the device should be reset by writing Reg0 = 111 binary. All registers are then restored to their default reset values.

Reg0 [4:3] Enable Control

The device enable condition is defined by the two bits Reg0 [4:3]. Four different conditions can trigger the device to turn on depending on the SDA or SCL inputs.

ENABLE CONTROL				
Reg0 [4:3]		Device on Condition		Device Enters Shutdown Mode Condition
D1	D0	SCL	SDA	
0	0	High	High	Either SDA or SCL goes low
0	1	High	SDA Toggling (1)	Either SCL goes low or SDA stops toggling (1)
1	0	High	Don't Care	SCL goes low
1	1	Always ON		Device always ON

Reg0 [6:5] Rise/Fall Time Scaling

These two bits allow to scale the rise and fall time defined in Reg5 ramp rate register.

For example, Reg0 [6:5] = 01 (2× slower scaling) and Reg5 = 1, then the rise time = 96ms × 2 = 192ms.

RISE/FALL TIME SCALING (2)		
Reg0 [6:5]		Scaling Factor
D1	D0	
0	0	1× Normal
0	1	2× Slower
1	0	4× Slower
1	1	8× Faster

NOTES:

1. Device enters shutdown/sleep mode with a delay t_{SHDN} (600μs, TYP) after the last falling edge of SDA.
2. Bit Reg0 [7] must be kept to 0 and is not used in normal operation (reserved for factory test).

REGISTER DESCRIPTION (continued)

Reg1 Flash Period and Reg2/Reg3 ON Timer 1/2

The three registers Reg1, Reg2 and Reg3 allow configuration of the blinking time for the two timers 1/2, associated with PWM1 and PWM2. Reg2 and Reg3 define the LED ON time as a percentage of the period defined in Reg1. The ON time (t_{ON}) includes the ramp rise time as shown in Figure 6.

For example, for Reg1 = 3 and Reg2 = 5, ON timer 1 is equal to 2% of 0.64s = 12.8ms.

Reg1 [7] Ramp Linear

The default setting, bit Reg1 [7] = 0, provides with a logarithmic-like S ramp up and down curve. By setting this bit to 1, the ramp becomes a simple linear up and down waveform.

Reg1 [6:0] FLASH PERIOD		
Dec	Binary	Period (s)
0	0000000	0.128
1	0000001	0.384
2	0000010	0.512
3	0000011	0.640
4	0000100	0.768
5	0000101	0.896
6	0000110	1.024
7	0000111	1.152
8	0001000	1.28
9	0001001	1.408
10	0001010	1.536
11	0001011	1.664
12	0001100	1.792
13	0001101	1.92
…	…	…
111	1101111	14.46
112	1110000	14.59
113	1110001	14.72
114	1110010	14.85
115	1110011	14.98
116	1110100	15.10
117	1110101	15.23
118	1110110	15.36
119	1110111	15.49
120	1111000	15.62
121	1111001	15.74
122	1111010	15.87
123	1111011	16.0
124	1111100	16.13
125	1111101	16.26
126	1111110	16.38
127	1111111	16.51

Reg2/Reg3 FLASH ON TIMER 1/2		
Dec	Binary	Percentage of Period (%)
0	00000000	0.0%
1	00000001	0.4%
2	00000010	0.8%
3	00000011	1.2%
4	00000100	1.6%
5	00000101	2.0%
6	00000110	2.3%
7	00000111	2.7%
8	00001000	3.1%
9	00001001	3.5%
10	00001010	3.9%
11	00001011	4.3%
12	00001100	4.7%
13	00001101	5.1%
…	…	…
239	11101111	93.4%
240	11110000	93.8%
241	11110001	94.1%
242	11110010	94.5%
243	11110011	94.9%
244	11110100	95.3%
245	11110101	95.7%
246	11110110	96.1%
247	11110111	96.5%
248	11111000	96.9%
249	11111001	97.3%
250	11111010	97.7%
251	11111011	98.0%
252	11111100	98.4%
253	11111101	98.8%
254	11111110	99.2%
255	11111111	99.6%

REGISTER DESCRIPTION (continued)

Reg4 [5:0] LED Enable Control

Register Reg4 sets the mode of each LED channel to either always ON/OFF or PWM1/PWM2.

For example, Reg4 = 01000001 (binary), sets LED1 ON and other channels OFF.

LED ENABLE (1/2/3)		
Dec	**Binary**	**Function**
0	00	Always OFF
1	01	Always ON
2	10	PWM1
3	11	PWM2

Reg4 [6] Device Enable

To operate the device and turn on the LEDs outside of auto blink mode, the bit Reg4 [6] must be set to 1.

If Reg4 [6] = 0, it is possible to write to I²C registers, but all LEDs stay off until the bit equals to 1. By default, the bit is 0.

When auto blink mode is disabled (enable auto blink bit Reg9 [0] = 0):

- If Reg4 [6] = 0 then all LEDs are off. I²C write is still possible.
- If Reg4 [6] = 1 then LEDs turn on according to the register settings.

This is independent of EN pin input state high or low.

Reg5 Ramp Times

The register Reg5 sets the rise and fall time durations for the LED current ramp transitioning between 0mA and the nominal current. The rise and fall ramp times are defined by 4 bits Reg5 [3:0] and Reg5 [7:4] respectively.

For example, Reg5 = 4 and Reg0 [6:5] = 0 (1× ramp scaling), the rise time is equal to 384ms.

t_{RISE} Reg5 [3:0]		Ramp Time (ms)			
t_{FALL} Reg5 [7:4]		Ramp Scaling (3)			
Dec	**Binary**	**00 1×**	**01 2× slower**	**10 4× slower**	**11 8× faster**
0	0000	1.5	1.5	1.5	1.5
1	0001	96	192	384	12
2	0010	192	384	768	24
3	0011	288	576	1152	36
4	0100	384	768	1536	48
5	0101	480	960	1920	60
6	0110	576	1152	2304	72
7	0111	672	1344	2688	84
8	1000	768	1536	3072	96
9	1001	864	1728	3456	108
10	1010	960	1920	3840	120
11	1011	1056	2112	4224	132
12	1100	1152	2304	4608	144
13	1101	1248	2496	4992	156
14	1110	1344	2688	5376	168
15	1111	1440	2880	5760	180

NOTE:

3. There is only one ramp scaling register for both the rise and fall times.

REGISTER DESCRIPTION (continued)

Reg6, Reg7, Reg8 LED Current Setting

Registers Reg6 to Reg8 define the LED current setting for the channels D1 to D3 respectively. The LED current can be programmed with 192 steps between 0.125mA minimum and 24mA maximum.

For example, 24mA is set by the code BFh (191 decimal, 10111111 binary) or any higher code value. 10mA current is set by the code 4Fh (79 decimal, 01001111 binary).

I_{OUT} (mA)	Data Dec	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0.125	0 (default)	00h (default)	0	0	0	0	0	0	0	0
0.25	1	01h	0	0	0	0	0	0	0	1
0.38	2	02h	0	0	0	0	0	0	1	0
0.50	3	03h	0	0	0	0	0	0	1	1
…	…	…	…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…	…	…	…
10.00	79	4Fh	0	1	0	0	1	1	1	1
10.13	80	50h	0	1	0	1	0	0	0	0
…	…	…	…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…	…	…	…
20.00	159	9Fh	1	0	0	1	1	1	1	1
20.13	160	A0h	1	0	1	0	0	0	0	0
…	…	…	…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…	…	…	…
23.88	190	BEh	1	0	1	1	1	1	1	0
24.00	191	BFh	1	0	1	1	1	1	1	1
24.00	192	C0h	1	1	0	0	0	0	0	0
…	…	…	…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…	…	…	…
24.00	254	FEh	1	1	1	1	1	1	1	0
24.00	255	FFh	1	1	1	1	1	1	1	1

REGISTER DESCRIPTION (continued)

Auto Blink Mode Operation

The Auto Blink mode automatically turns on and off LED1 (on D1 pin) after EN pin goes high without the need to send an I²C command. When a phone with a discharged battery is connected to a charger, the phone is off (black screen) and LED1 is blinking to notify that the battery is charging.

Without this feature, during a deeply discharged battery charge stage, the battery indicator light may be off and it appears as though the battery is not charging.

Figure 10 illustrates LED1 (connected to D1 pin) pulsing on/off with 2s period (1s ON, 1s OFF) and 8mA max current (I_{MAX}), all other channels are turned off. Other LED1 current options can be requested at the factory for 2mA, 4mA and 6mA.

Once EN input is set to low, the auto blink mode stops.

Reg9 Auto Blink Mode

The Auto Blink mode is controlled by the enable Auto Blink mode bit Reg9 [0]. By default, Auto Blink mode is enabled with Reg9 [0] = 1. By setting this bit to 0, the Auto Blink mode can be disabled.

To disable Auto Blink mode, write Reg9 = 0x06 to set the enable Auto Blink bit Reg9 [0] to 0. Next time EN input goes high, the device will not enter Auto Blink mode.

To enable Auto Blink mode, write Reg9 = 0x07 to set the enable auto blink bit Reg9 [0] to 1. When EN input goes high, the device enters auto blink mode.

Once the Auto Blink mode starts, 4s after EN goes high, the auto started bit Reg9 [7] is set to 1. Reg9 [7] is a read only bit.

Important Note: It is recommended that SGM31324 is in the reset state (default state after power-up) before the Auto Blink mode is activated. If the SGM31324 registers are modified and the Auto Blink mode is activated without a register reset, the blinking operation might be incorrect.

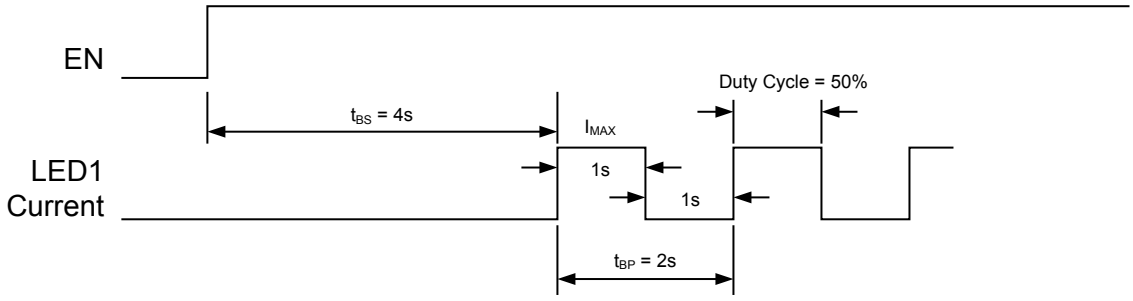
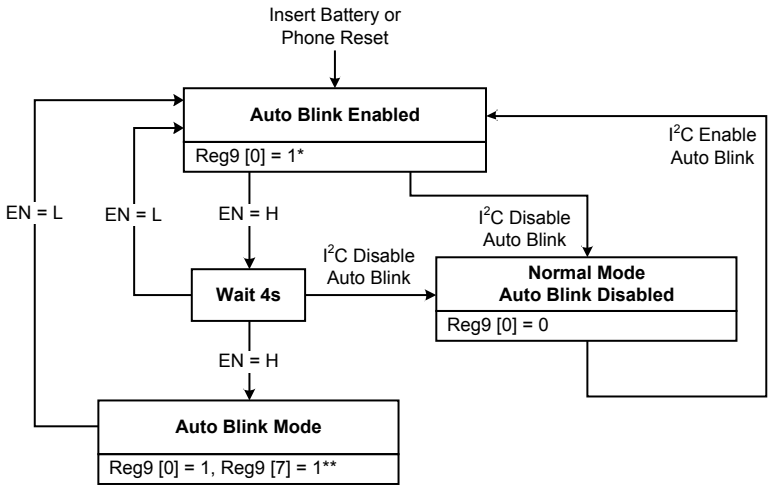


Figure 10. Auto Blink Mode Timing Diagram

REGISTER DESCRIPTION (continued)



* Enable Auto Blink bit Reg9 [0]
** Auto Blink Started bit Reg9 [7]

Figure 11. Auto Blink Mode

Initial Condition	
Phone Operation	SGM31324 Interface
Battery discharged (V_{BAT} < 3.2V) Phone turned off (LCD off) Reset SGM31324 SGM31324 Auto Blink Mode is enabled (default)	 Set SGM31324 EN pin high Write Reg0 = 0x07 Set SGM31324 EN pin low Reg9 [0] = 1*
Plug in the charger ↓ After 4s LED1 starts blinking ↓ Auto Blink Mode on ↓ Battery recharged (V_{BAT} > 3.6V) Phone turns on SGM31324 Auto Blink Mode is disabled ↓ LED1 stops blinking	Set SGM31324 EN pin high Reg9 [0] = 1, Reg9 [7] = 1** To disable Auto Blink Mode Write Reg9 [0] = 0 or set EN pin low

* Enable Auto Blink bit Reg9 [0]
** Auto Blink Started bit Reg9 [7]

Figure 12. Smartphone Auto Blink Mode Operation

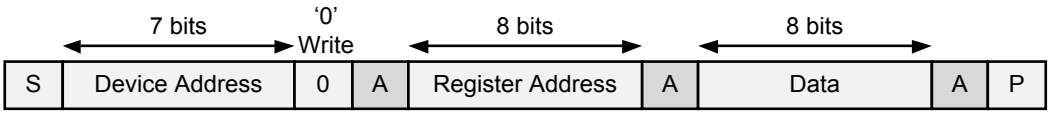
APPLICATION INFORMATION

I²C Interface Protocol

On the SGM31324, the 10 internal registers Reg0 to Reg9 can be accessed via the I²C interface. The I²C device address is 0x30 hexadecimal or 110000 binary. The read and write commands allow to modify the content of each register. For further details on the I²C protocol, please refer to the I²C−Bus Specification, document number 9398 393 40011, from Philips Semiconductors.

The protocol for Write and Read is the following.

Write:



Where S = START condition
P = STOP condition
Device Address = 0110000 (7 bits, MSB first)
Register Address = Reg0 - Reg9 address (8 bits)
Data = data to read or write (8 bits)
1 = Read command bit
0 = Write command bit
A = acknowledge (SDA low)
A* = not acknowledge (SDA high)

From master to slave (SGM31324)

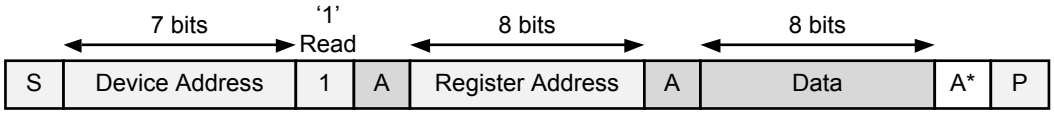
From slave (SGM31324) to master

For example, the command to write SGM31324 register Reg4 (address 4) = 0, LEDs always OFF:

S	0110000	0	A	00000100	A	00000000	A	P

NOTE: For the I²C Reset commands (“reset register only” and “reset complete chip”), the last byte is followed by a “not acknowledge” (SDA high). For these two commands, the lack of acknowledge at the end of the command is to be ignored.

Read:



APPLICATION INFORMATION (continued)

Power Saving, Sleep Mode

When the SGM31324 is not driving LEDs, for example when all LEDs are off, the driver current consumption can be set to “zero current” by putting the device into shutdown or sleep mode.

The register content is preserved while the device goes into shutdown/sleep mode. To restart with LEDs off, LEDs should be turned off by writing zero into the LED enable control register Reg4 before entering the sleep mode.

This can be done by writing into the enable control mode register Reg0 [4:3] = 01 and select the option “SCL= High & SDA Toggling”. The device remains in sleep mode while there is no activity on the SDA line.

The following sequence shows an example where LED3 is flashing initially, then the device is set to sleep mode, then the part is restarted.

LED3 (blue) is flashing. SGM31324 VIN pin current (I_{IN}) = 120μA.

To enter sleep mode: write enable control mode register Reg0 [4:3] = 01, for option “SCL = High & SDA Toggling”.

LEDs are off. I_{IN} = “zero” when there is no activity on the SDA line.

To restart the driver: Write enable control mode register Reg0 [4:3] = 00, for option “SCL & SDA High”.

LED3 (blue) is flashing. I_{IN} = 120μA.

Voltage Headroom

The lowest headroom voltage is critical for systems with supply voltages nearing 3V, such as battery operated or regulated 3.3V systems. The advancement of LED technologies has made possible lower LED current and lower forward voltage drop (V_F). For example, the majority of vendors’ Blue LED’s V_F at 5mA is 3.15V or below. With the cut-off voltage for most 1-cell Li+ powered systems set to 3.3V ~ 3.5V, it is possible to drive RGB LEDs without voltage step-up as long as the internal voltage drop for the driver circuit is specially designed for the lowest voltage possible.

Each current sink of the SGM31324 is designed to allow the lowest operating input voltage without voltage step-up while maintaining current regulation, thus extending the battery run time. When input voltage is low, the internal low impedance current sink adds merely 65mV (TYP) headroom on top of the LED forward voltage at 24mA per channel.

The formula is: $V_{IN(MIN)} = V_{F(MAX)} + V_{SINK(MIN)}$,

where V_{IN} is the driving voltage applied to the anode of each LED, V_F is the forward voltage drop of the LED, and V_{SINK} is the voltage at each Dx. When V_{IN} is high (fully charged battery), V_{SINK} is internally regulated to take the voltage difference between V_{IN} and V_F. For instance, if V_{IN} is 4V and V_F for LED1 is 3.1V, then V_{SINK} at D1 pin is 0.9V.

When V_{IN} decreases (as the battery discharges), $V_{IN(MIN)}$ governs the lowest supply voltage for the LEDs without losing regulation. The design rule of thumb is to make sure the cut-off voltage is higher than $V_{IN(MIN)}$ for all conditions. It is important to emphasize the definition of “losing regulation”; in this datasheet it is defined as when the LED current drops to 90% of the nominal programmed current level.

At 24mA, the typical V_{SINK} can be as low as 65mV for each Dx pin. Since every LED has a slightly different V_F at a given current, the minimum V_{IN} is determined by the highest V_F plus 65mV typical. For the case of 24mA programmed current and highest V_F of 3.2V, V_{IN} in can go as low as 3.265V without losing LED current regulation. When V_{IN} drops further while the $V_{SINK(MIN)}$ remains constant, V_F will be forced lower. As a result, the LED current will reduce according to each LED’s V-I curve.

REVISION HISTORY

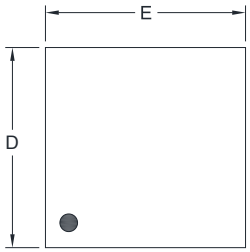
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (JULY 2017) to REV.A

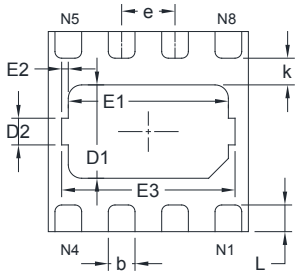
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

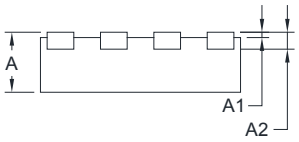
UTDFN-1.5×1.5-8L



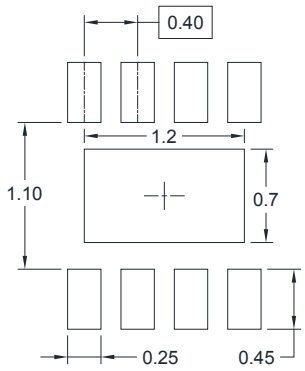
TOP VIEW



BOTTOM VIEW



SIDE VIEW

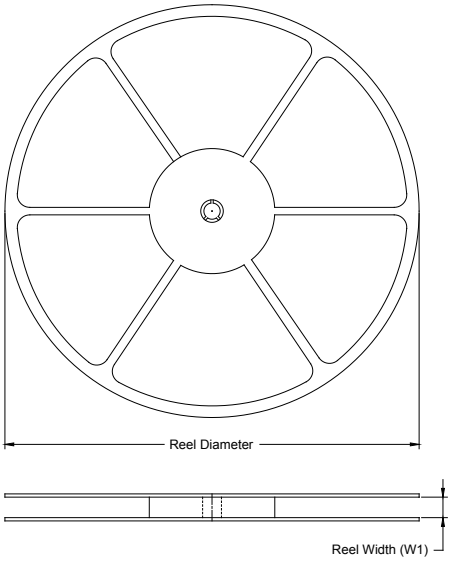


RECOMMENDED LAND PATTERN

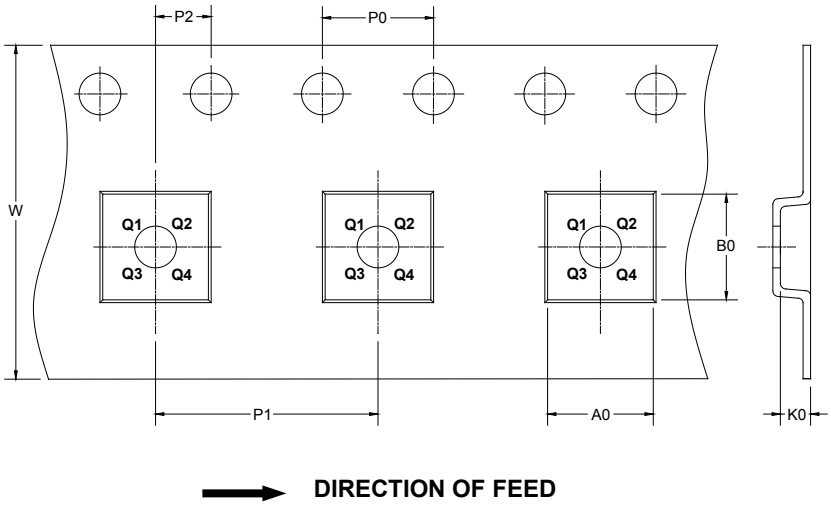
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.400	0.500	0.016	0.020
A1	0.000	0.050	0.000	0.002
A2	0.127 REF		0.005 REF	
D	1.450	1.550	0.057	0.061
D1	0.600	0.800	0.024	0.031
D2	0.200 REF		0.008 REF	
E	1.450	1.550	0.057	0.061
E1	1.100	1.300	0.043	0.051
E2	0.050 REF		0.002 REF	
E3	1.200	1.400	0.047	0.055
k	0.200 REF		0.008 REF	
b	0.150	0.250	0.006	0.010
e	0.400 BSC		0.016 BSC	
L	0.150	0.250	0.006	0.010

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



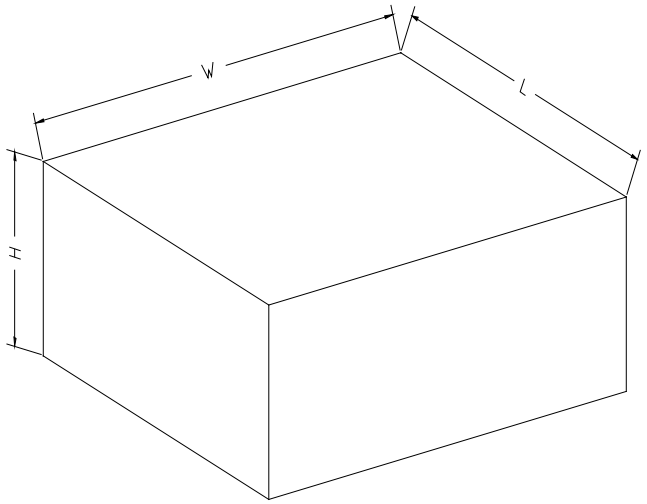
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-1.5×1.5-8L	7″	9.0	1.70	1.70	0.75	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002