SGM4073
Configurable Reset Timer with Integrated Load Switch

GENERAL DESCRIPTION

The SGM4073 is both a timer for resetting a mobile device and an advanced load management switch for applications requiring a highly integrated solution.

If the mobile device is off, holding nSR0 low (by pressing power-on key) for 1.9s turns on the PMIC.

As a reset timer, it has one input and one fixed delay output. It generates a fixed delay of 7.7s by disconnecting the PMIC from the battery power supply for 468ms. Then the load switch is turned on again to reconnect the battery to the PMIC such that PMIC goes into power-on sequence. The reset delay can be customized by connecting an external resistor to the DELAY_ADJ pin. Refer to Table 4.

As an advanced load management switch, the SGM4073 disconnects loads powered from the DC power rail (< 6V) with stringent off-state current targets and high load capacitances (up to 200μF). The SGM4073 consists of a slew rate controlled low-impedance MOSFET switch (20mΩ typical at 3.6V) that has exceptionally low off-state current drain to facilitate compliance with standby power requirements. The slew rate controlled turn-on characteristic prevents inrush current and the resulting excessive voltage drop on power rails.

The low I_Q enables direct interface to lower-voltage chipsets without external translation, while maintaining low power consumption.

The SGM4073 operates over an ambient temperature range of -40℃ to +85℃. It is available in Green WLCSP-1.31×1.62-12B package.

FEATURES

- **Input Voltage Operating Range: 1.5V to 5.5V**
- **Factory Programmed Reset Delay: 7.7s**
- **Factory Programmed Reset Pulse: 468ms**
- **Factory Customized Turn-On Time: 1.9s**
- **Factory Customized Turn-Off Delay: 7.7s**
- **Adjustable Reset Delay Option with External Resistor**
- **Low I_Q Saves Power Interfacing to Low-Voltage Chips**
- **OFF Pin Turns Off Load Switch to Maintain Battery Charge during Shipment and Inventory. Ready to Use Right Out of the Box**
- **Typical R_{ON}: 20mΩ (TYP) at V_{BAT} = 3.6V**
- **Slew Rate/Inrush Control with t_R: 3ms (TYP)**
- **6A Maximum Continuous Current**
- **Output Capacitor Discharge Function during Reset Period**
- **Zero-Second Test-Mode Enable**
- **Available in Green WLCSP-1.31×1.62-12B Package**

APPLICATIONS

Smart Phones, Tablet PCs
Storage, DSLR and Portable Devices

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4073	WLCSP-1.31×1.62-12B	-40℃ to +85℃	SGM4073YG/TR	XXXX 4073	Tape and Reel, 3000

NOTE: XXXX = Date Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{BAT} to GND ..... -0.3V to 6.5V
V_{OUT} to GND ..... -0.3V to 6.5V
Maximum Continuous Switch Current 6A
Power Dissipation, P_D @ T_A = 25℃, I_{OUT} = 6A, R_{ON} = 20mΩ 0.72W
Package Thermal Resistance
WLCSP-1.31×1.62-12B, θ_{JA} ..... 86℃/W
DC Input Voltage
nSR0, DSR, OFF, DELAY_ADJ, SYS_WAKE .. -0.5V to 6.5V
DC Input Diode Current, V_{BAT} < 0V ..... -50mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD
HBM 8000V
MM 400V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range
V_{BAT} ..... 1.5V to 5.5V
nSR0, DSR, OFF, SYS_WAKE ..... 0V to 5.5V
Output Voltage Range ..... 0V to V_{BAT}
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

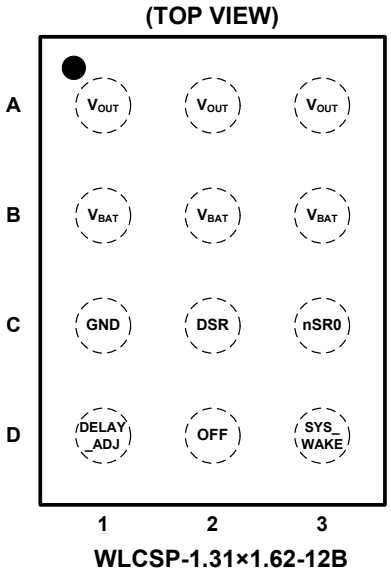
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION

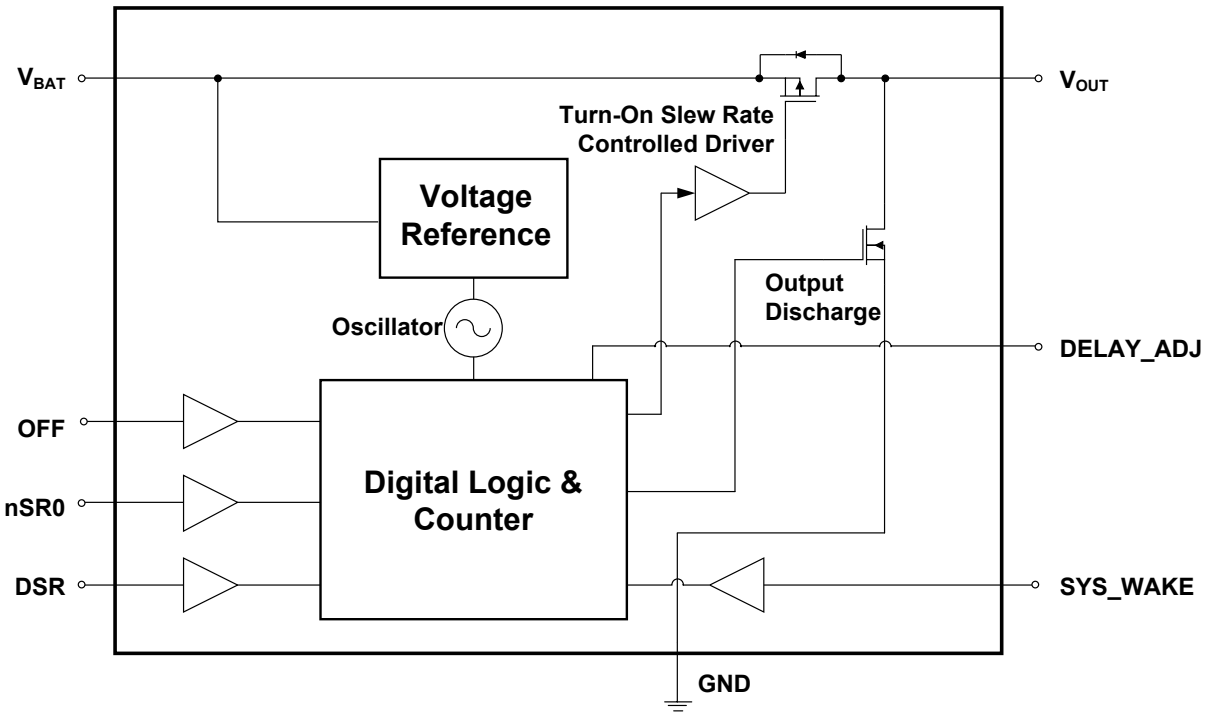


WLCSP-1.31×1.62-12B

PIN DESCRIPTION

PIN	NAME	FUNCTION	
		Normal Operation	Zero-Second Factory-Test Mode (Only for t_{VON} and t_{PHL})
A1, A2, A3	V_{OUT}	Switch Output.	Switch Output.
B1, B2, B3	V_{BAT}	Supply Input.	Supply Input.
C1	GND	Ground.	Ground.
C2	DSR	Delay Selection Input. It's connected to GPIO with 100kΩ pull-up or to V_{BAT} directly without pull-up resistor.	Logic LOW.
C3	nSR0	Power-On or Reset Input. Active LOW. Dampproof and anti-creeping input.	Logic LOW.
D1	DELAY_ADJ	Reset Delay Adjustment. Must tie to V_{BAT} directly if not used. To adjust the reset delay, a resistor (R_{ADJ}) is connected between this pin and ground.	Connected to V_{BAT} or GND.
D2	OFF	Load Switch Disable. Rising edge triggered, changes load switch from ON state to OFF state. The OFF pin cannot be left floating.	High or Low.
D3	SYS_WAKE	System Wake-Up Input. Changes load switch from OFF state to ON state. Dampproof and anti-creeping input.	High or Low.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

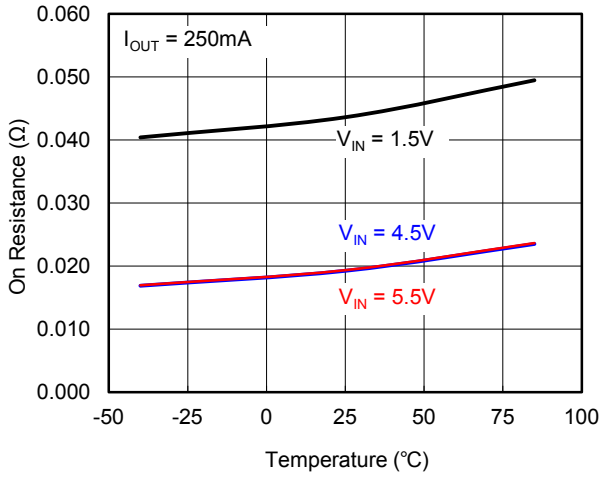
(V_{BAT} = 3.6V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BASIC OPERATION						
Shutdown Current	I_{SD}	VOUT Floating, Load Switch = OFF		0.7	1.5	μA
On Resistance	R_{ON}	V_{BAT} = 5.5V, I_{OUT} = 500mA		18	36	mΩ
		V_{BAT} = 3.6V, I_{OUT} = 500mA		20	37	
		V_{BAT} = 1.5V, I_{OUT} = 500mA		42	87	
Output Discharge $R_{PULL-DOWN}$	R_{PD}	Reset Period, I_{FORCE} = 10mA		65	90	Ω
Input High Voltage	V_{IH}		1.2			V
Input Low Voltage	V_{IL}				0.4	V
Input Leakage Current (1)	I_{IN}	0V ≤ V_{BAT} ≤ 5.5V			1.5	μA
Power-On Reset Threshold	V_{POR}			1.38	1.5	V
	V_{HYS}			0.1		
Quiescent Current	I_Q	nSR0 = 3.6V, DSR = 3.6V, SYS_WAKE = GND, OFF = GND, I_{OUT} = 0mA, Load Switch = ON		1	2	μA
Force Voltage Threshold	V_{COERU}	SYS_WAKE up going		0.7		V
	V_{COERD}	nSR0 down going		0.6		
Force Current Threshold	$I_{COERSNK}$	SYS_WAKE up going		-50		μA
	$I_{COERSRC}$	nSR0 down going		45		
Discharging Residual Voltage	V_{DIS}			0.4		V
POWER-ON AND RESET TIMING						
Turn-On Time for V_{OUT}	t_{VON}	R_L = 5kΩ, DSR = HIGH, Figure 1	1.4	1.9	2.4	s
Timer Delay before Reset	t_{PHL}	R_L = 5kΩ, DSR = HIGH, Figure 2	6.2	7.7	9.2	s
Reset Timeout Delay of V_{OUT}	t_{REC}	R_L = 5kΩ, Figure 2	376	468	541	ms
LOAD SWITCH TURN-ON TIMING						
Turn-On Delay Time	t_{DON}	R_L = 5Ω, C_L = 100μF, Figure 3		4		ms
V_{OUT} Rise Time	t_R			3		ms
Turn-On Time, SYS_WAKE to V_{OUT}	t_{ON}			7		ms
LOAD SWITCH TURN-OFF WITH DELAY						
Delay to Turn Off Load Switch	t_{SD}	R_L = 150Ω, C_L = 100μF, DSR = HIGH, Figure 4	6.2	7.7	9.2	s
V_{OUT} Fall Time	t_F			10		ms
Turn-Off Time	t_{OFF}			7.7		s
LOAD SWITCH ZERO-SECOND TURN-OFF						
Delay to Turn Off Load Switch	t_{SD}	R_L = 150Ω, C_L = 100μF, DSR = LOW, Figure 4		2		ms
V_{OUT} Fall Time	t_F			10		ms
Turn-Off Time	t_{OFF}			12		ms
ZERO-SECOND FACTORY-TEST MODE						
Turn-On Time for V_{OUT}	t_{VON}	C_L = 5pF, R_L = 5kΩ, Load Switch = OFF, DSR = LOW, Figure 1		6.3		ms
Timer Delay before Reset	t_{PHL}	C_L = 5pF, R_L = 5kΩ, Load Switch = ON, DSR = LOW, Figure 2		1.4		ms

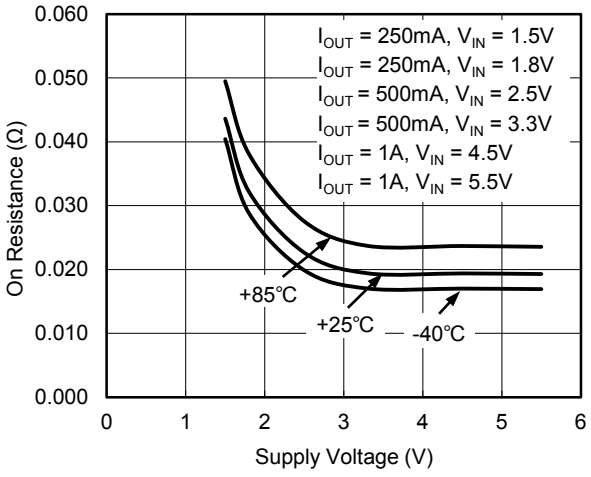
NOTE 1: Input pins are nSR0, OFF, DSR, and SYS_WAKE.

TYPICAL PERFORMANCE CHARACTERISTICS

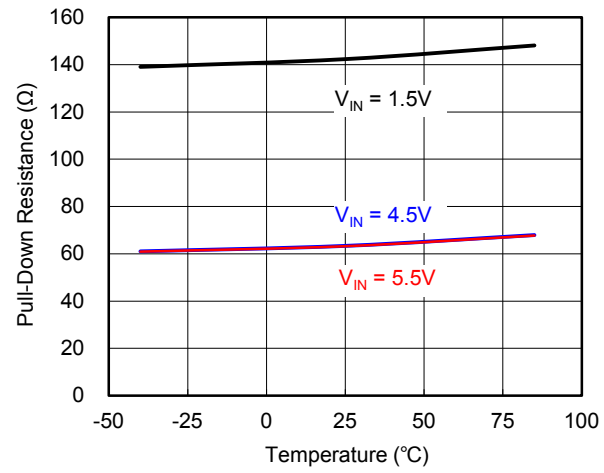
On Resistance vs. Temperature



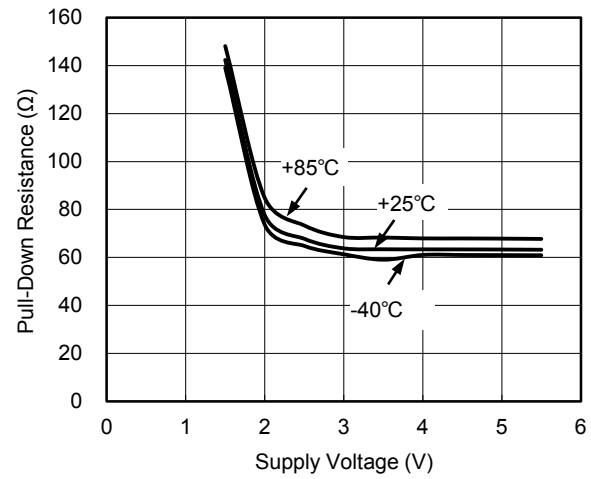
On Resistance vs. Supply Voltage



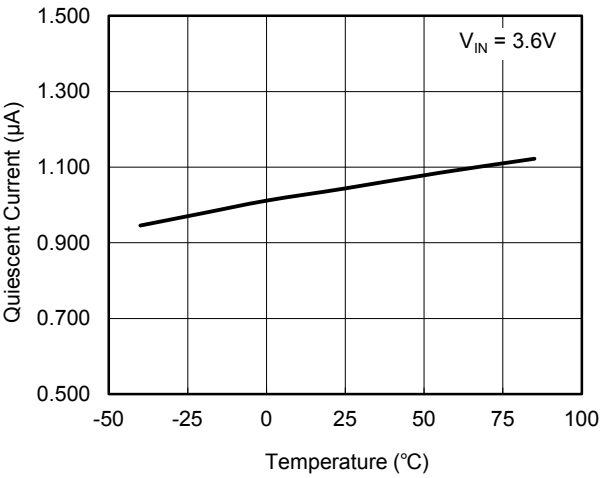
Pull-Down Resistance vs. Temperature



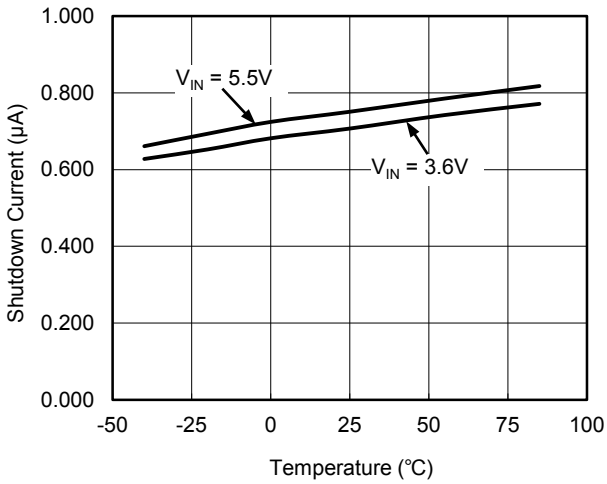
Pull-Down Resistance vs. Supply Voltage



Quiescent Current vs. Temperature

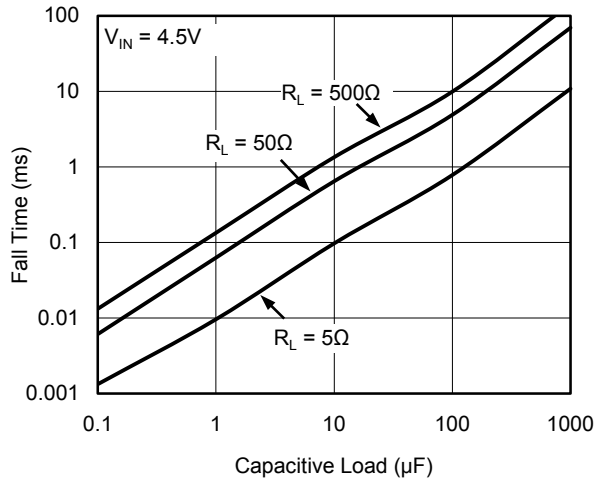


Shutdown Current vs. Temperature

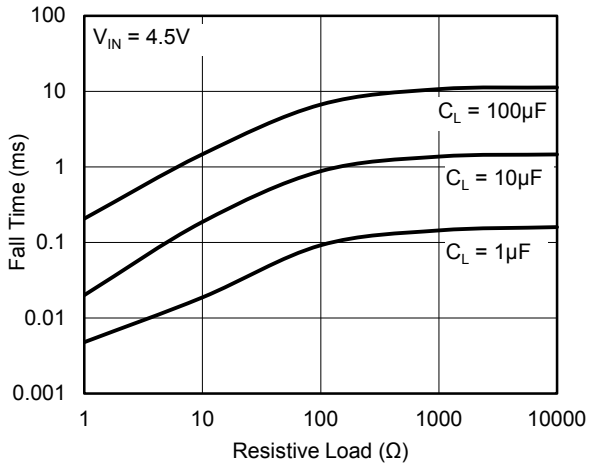


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

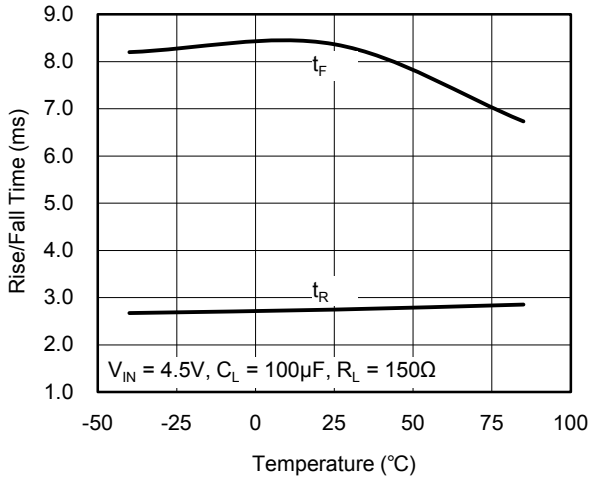
Fall Time vs. Capacitive Load



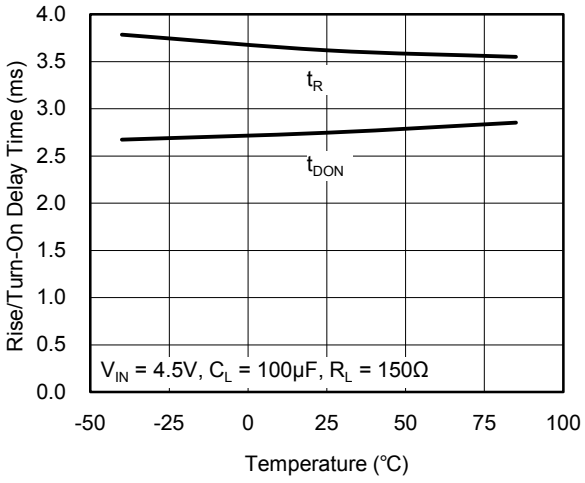
Fall Time vs. Resistive Load



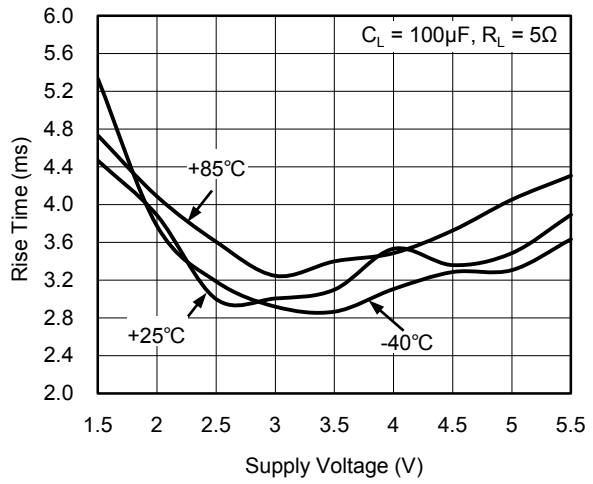
Rise/Fall Time vs. Temperature



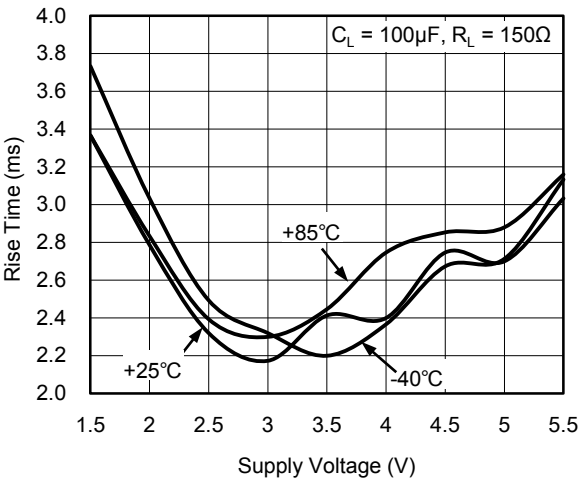
Rise/Turn-On Delay Time vs. Temperature



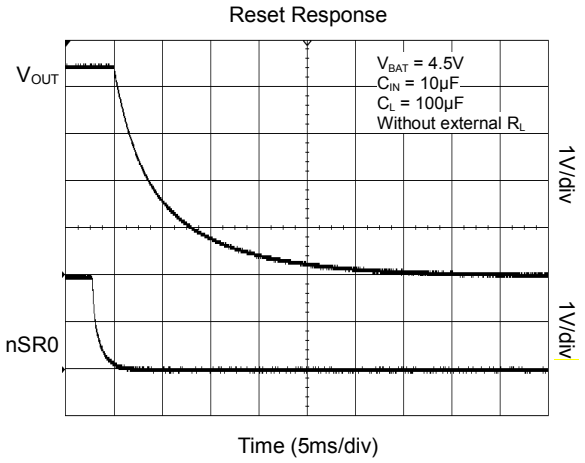
Rise Time vs. Supply Voltage



Rise Time vs. Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)



TIMING DIAGRAMS

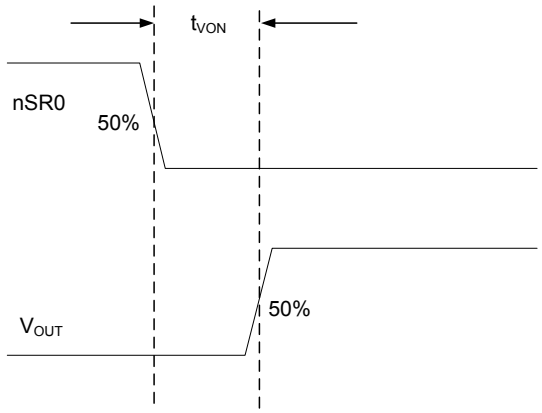


Figure 1. Power-On with nSR0

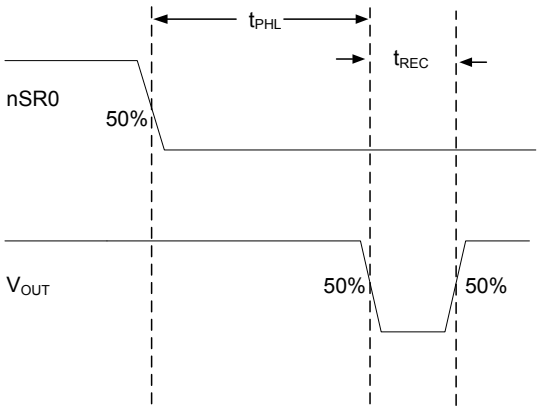


Figure 2. RESET Timing

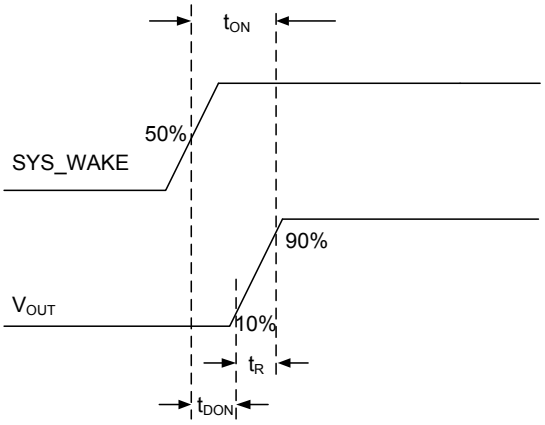


Figure 3. Timing Diagram (SYS_WAKE vs. VOUT)

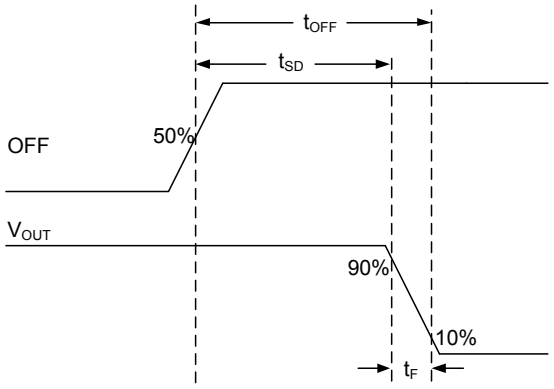


Figure 4. Timing Diagram (OFF vs. VOUT)

TYPICAL APPLICATION CIRCUITS

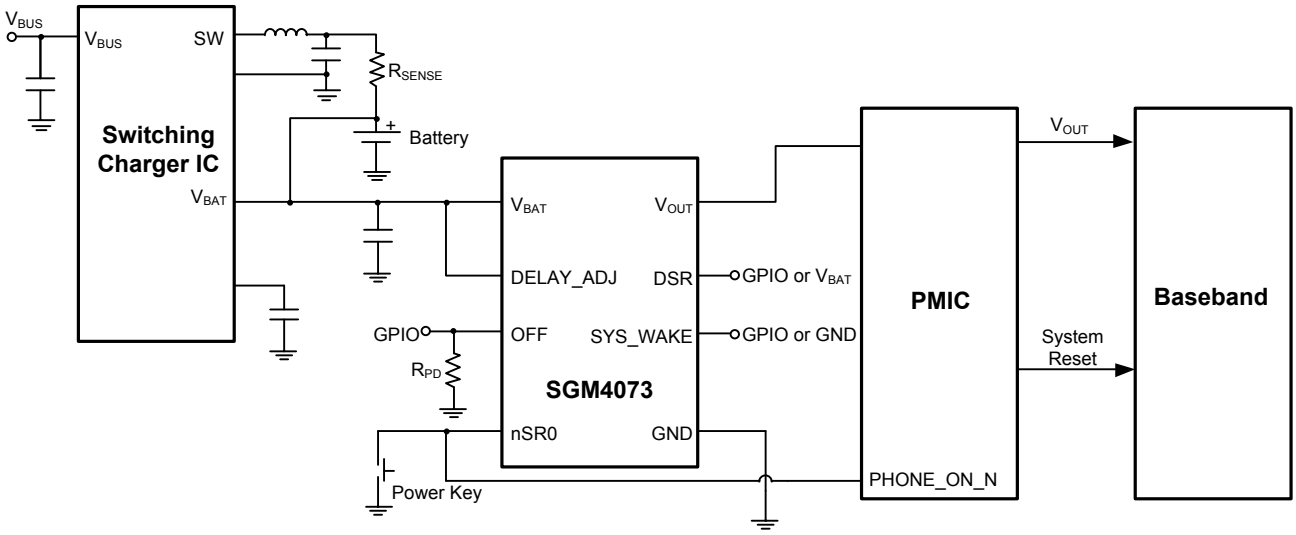


Figure 5. Typical Application with a Stand Alone Switching Charger IC

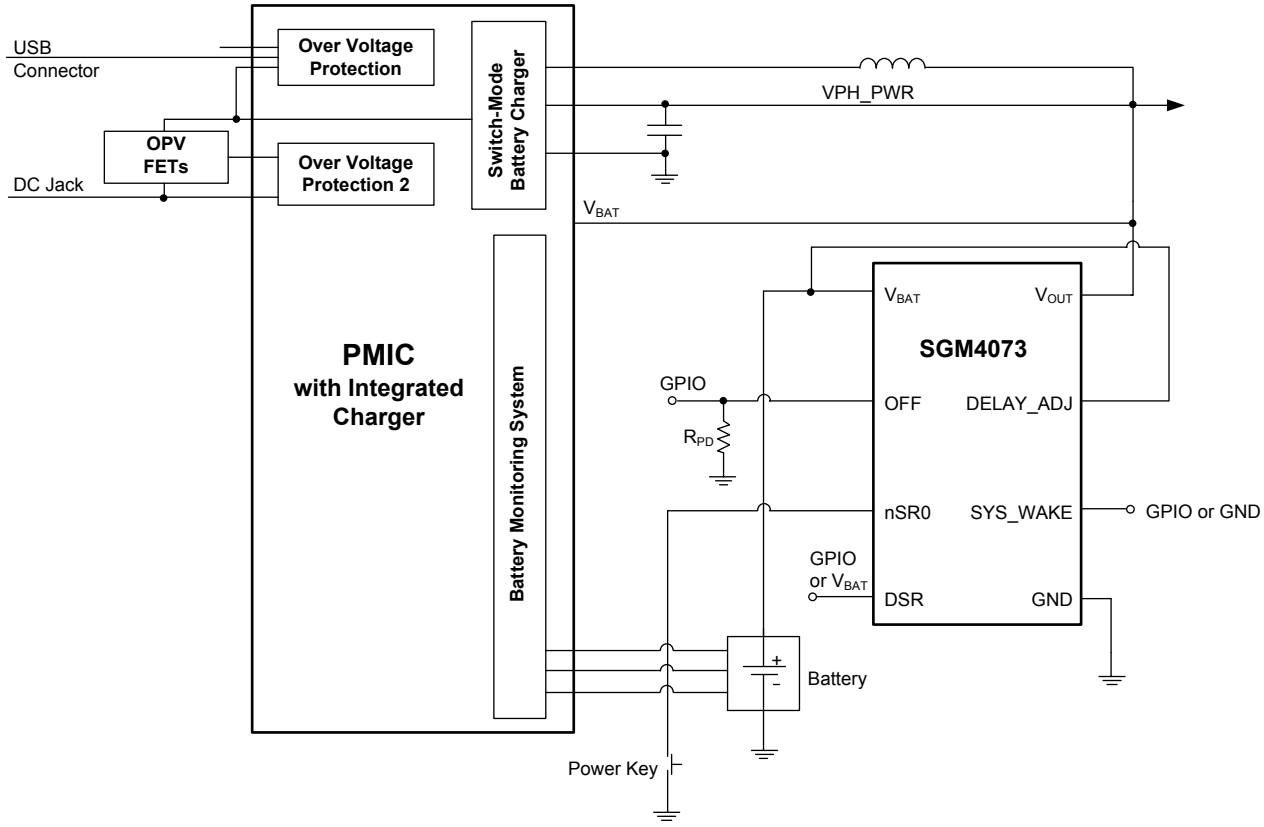


Figure 6. Typical Application PMIC with a Integrated Charger

APPLICATION INFORMATION

Reset Timer and Advanced Load Management

The SGM4073 is both a reset IC and an advanced load management device. Typical applications are shown in Figure 5 and Figure 6. SGM4073 does not need pull-up circuit like *75939 for nSR0 pin's anti-creeping. Dampproof makes it more robust, and SGM4073 can also replace *75939 in circuit directly.

Power-On

There are two methods to turn on the load switch to wake up the PMIC. When a HIGH is applied to the SYS_WAKE pin or when nSR0 is held LOW for > 1.9s (see Figure 1), the SGM4073 turns on its load switch to allow PMIC to connect to the battery. The reset feature is disabled when V_{OUT} is toggled from OFF to ON. Continuously holding nSR0 LOW does not trigger a reset event.

To enable the reset feature, nSR0 must return to HIGH such that SGM4073 resets its internal counter.

Reset Timer

During normal operation of a mobile device, if a reset operation is needed for mobile equipment, holding the power switch, to which nSR0 is connected and is forced LOW, for at least 7.7s, causes the SGM4073 to cut off the supply power to PMIC for 468ms by turning off the load switch. If after 468ms, V_{OUT} is less than V_{DIS} (0.4V), the SGM4073 then automatically turns on the load switch to reconnect the PMIC to battery. If after 468ms, V_{OUT} is larger than V_{DIS} (0.4V), the SGM4073 will not turn on the load switch to reconnect the PMIC to battery until V_{OUT} is less than V_{DIS}. This forces PMIC to enter a power-on sequence.

If the power switch is released and nSR0 is returned to HIGH within 7.7s, the SGM4073 resets its counter and V_{OUT} remains in ON state; there is no change on V_{OUT} and a reset does not occur.

Disconnect PMIC from Battery (Turn-Off)

After holding the DSR pin HIGH, changing the OFF pin from LOW to HIGH (rising edge triggered) and holding it HIGH for at least 2ms, the SGM4073 triggers an internal counter to allow a factory-customized 7.7s delay before turning off internal load switch. The delay is intended to allow the PMIC to complete a power-down sequence before safely disconnected from the power supply. However, the turn-off sequence is terminated if a higher priority input is detected in t_{SD} period (see Resolving Input Conflicts section).

Alternatively, after holding the DSR pin LOW, changing the OFF pin from LOW to HIGH (rising edge triggered) and holding it HIGH for at least 2ms, the SGM4073 triggers the zero-second turn-off. Delay t_{SD} is significantly reduced to 2ms to avoid the default delay time to turn off load switch.

With its low shutdown current, the SGM4073 significantly reduces the current drain on a battery when the PMIC is turned off. In other words, it preserves the battery power for a longer period when a mobile device is in shutdown mode.

Power-On Reset

When SGM4073 is connected to a battery (V_{BAT} ≥ 1.38V), the part gets into Power-On Reset (POR) Mode. All internal registers are reset and V_{OUT} is ON at the end of POR sequence (see Table 2).

Table 1. V_{OUT} and Input Conditions

FUNCTION	INITIAL CONDITIONS (t = 0s)				ASSOCIATED DELAY	V_{OUT}	
	nSR0	SYS_WAKE	OFF	DSR		BEFORE	AFTER
Power-On	LOW	X	X	LOW	t_{VON} = 10ms	OFF	ON
	LOW	X	X	HIGH	t_{VON} = 1.9s	OFF	ON
Reset	LOW	X	X	LOW	t_{PHL} = 2ms	ON	High to Low to High
	LOW	X	X	HIGH	t_{PHL} = 7.7s t_{REC} = 468ms	ON	High to Low to High
Turn-Off	HIGH	LOW	Rising Edge	LOW	t_{SD} = 2ms	ON	OFF
	HIGH	LOW	Rising Edge	HIGH	t_{SD} = 7.7s	ON	OFF

NOTE: X = HIGH or LOW.

Table 2. Pin Condition after POR

PIN NAME	nSR0	DSR	SYS_WAKE	OFF	V_{OUT}
Default State (after POR)	1	1	0	0	ON

NOTE: 1 = Input Logic HIGH, 0 = Input Logic LOW, ON = Load switch is ON state.

APPLICATION INFORMATION (continued)

Zero-Second Factory-Test Mode

SGM4073 includes a Zero-Second Factory Test Mode to shorten the turn-on time for V_{OUT} (t_{VON}) and timer delay before reset (t_{PHL}) for factory testing.

When V_{OUT} is OFF, the default turn-on time (t_{VON}) is 1.9s. If the DSR pin is LOW prior to nSR0 going LOW, the SGM4073 bypasses the 1.9s delay and V_{OUT} is changed from OFF to ON immediately.

Similarly, default reset delay (t_{PHL}) is 7.7s. If V_{OUT} is ON and the DSR pin is LOW prior to nSR0 going LOW, the SGM4073 enters Zero-Second Factory Test Mode and bypasses the default reset delay of 7.7s; V_{OUT} is pulled from ON to OFF immediately. The reset pulse (t_{REC}) remains at 468ms in Zero-Second Factory Test Mode.

The DSR pin should never be left floating during normal operation.

Resolving Input Conflicts

The SGM4073 allows multiple simultaneous inputs and can resolve conflicts based on the priority level (see Table 3). When two input pins are triggered at the same time, only the higher priority input is served and the lower priority input is ignored. To have the lower priority signal serviced, it must be repeated.

Table 3. Input Priority

INPUT	PRIORITY (1 = HIGHEST)
nSR0	1
SYS_WAKE	2
OFF	3

Special Note on OFF Pin

In the t_{SD} period (DSR = HIGH only, see Figure 4), if nSR0 or SYS_WAKE is triggered when $0 < t < t_{SD}$, the SGM4073 exits the turn-off sequence and V_{OUT} remains in ON state. The higher priority input is served regardless of the condition of the OFF pin.

In order to re-initiate the turn-off sequence, the OFF pin must return to LOW, then toggle from LOW to HIGH again. The same input priority applies (Table 3) if DSR = HIGH.

Adjustable Reset Delay with an External Resistor and DSR

The reset delay is adjustable by connecting a commonly available, low-power, ±5%, POHS-compliant resistor between the DELAY_ADJ pin and the GND pin (Table 4). To disable the adjustable delay feature, DELAY_ADJ should be tied to V_{BAT} directly.

The reset delay is factory programmed at 7.7s.

The additional power consumption caused by using an external resistor is negligible. The external resistor is normally disconnected and is connected for milliseconds when nSR0 is pulled LOW.

This external adjustment feature provides a simple alternative method for controlling delay time for engineering and production at customer's location.

We can also factory program a wide range of turn-on times for V_{OUT} (t_{VON}) , timer delay before reset (t_{PHL}), reset timeout delay for V_{OUT} (t_{REC}), and load switch turn-off time (t_{OFF}) to match customer applications. In this case, the external resistor (R_{ADJ}) can be eliminated.

Table 4. Delay Adjustment vs. External Resistor

EXTERNAL RESISTOR R_{ADJ} (kΩ)	DELAY MULTIPLIER
Tie to GND (No Resistor)	0.50 × t_{PHL}
3.9	0.75 × t_{PHL}
10	1.25 × t_{PHL}
22	1.50 × t_{PHL}
47	1.75 × t_{PHL}
120	2.00 × t_{PHL}
Tie to V_{BAT} (No Resistor)	1.00 × t_{PHL}

Input Capacitor

The switch inside the reset timer doesn't require an input capacitor. To reduce device inrush current, a 0.1μF ceramic capacitor, C_{IN}, is recommended close to the V_{BAT} pin. A higher value of C_{IN} can be used to reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

While the load switch works without an output capacitor, if parasitic board inductance forces V_{OUT} below GND when switching off, a 0.1μF capacitor, C_{OUT}, should be placed between V_{OUT} and GND.

Fall Time

Device output fall time can be calculated based on the RC constant of the external components, as follows:

$$t_F = R_L \times C_L \times 2.2 \quad (1)$$

where t_F is 90% to 10% fall time; R_L is output load; and C_L is output capacitor.

Output Discharge

The device contains a R_{PD} = 65Ω on-chip pull-down resistor for quick output discharge. The resistor is activated only during the switch reset time. In this way, the load I_Q can be tested easily, as showed in Figure 6.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MAY 2017 – REV.A.2 to REV.A.3

Change the Tape and Reel, 5000 to 3000 2

DECEMBER 2016 – REV.A.1 to REV.A.2

Change the Maximum Continuous Current 1, 2

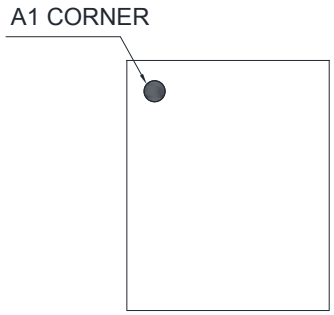
OCTOBER 2016 – REV.A to REV.A.1

Change the OFF pin description 3, 10

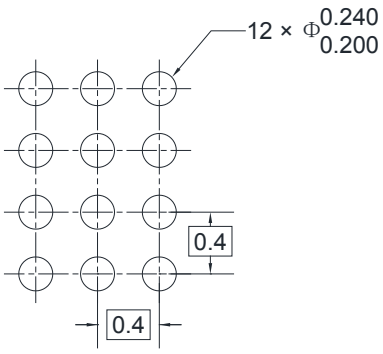
Changes from Original (MAY 2016) to REV.A

PACKAGE OUTLINE DIMENSIONS

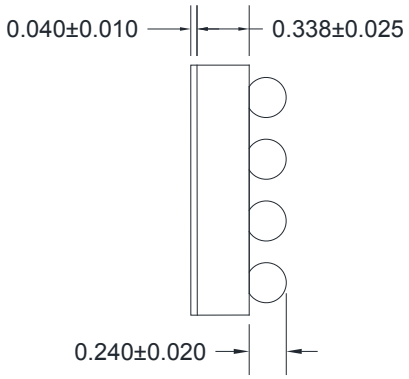
WLCSP-1.31×1.62-12B



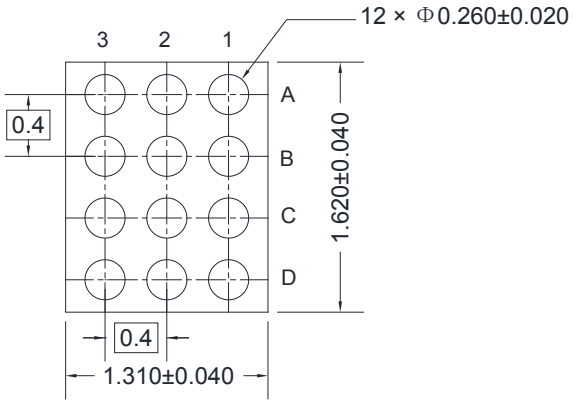
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

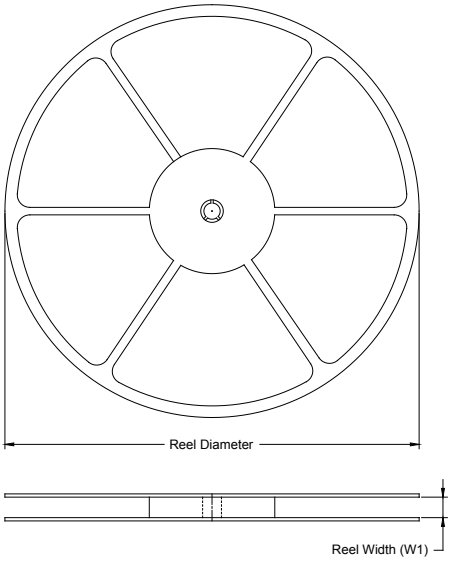


BOTTOM VIEW

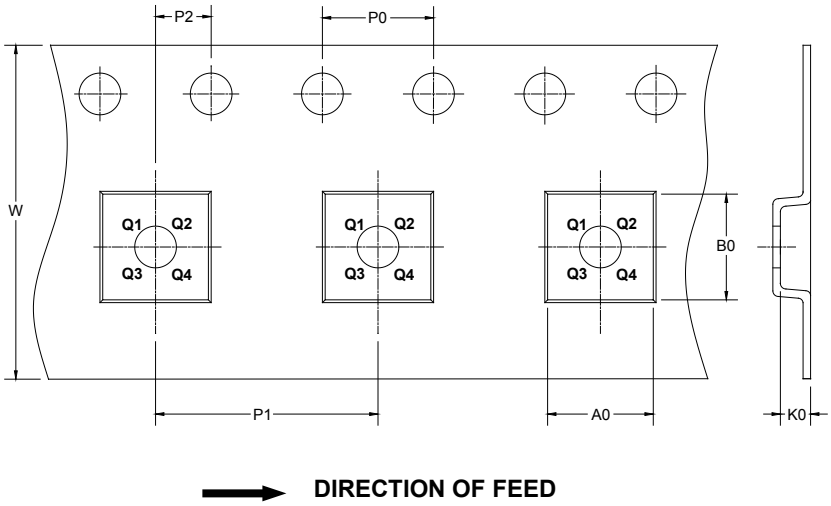
NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

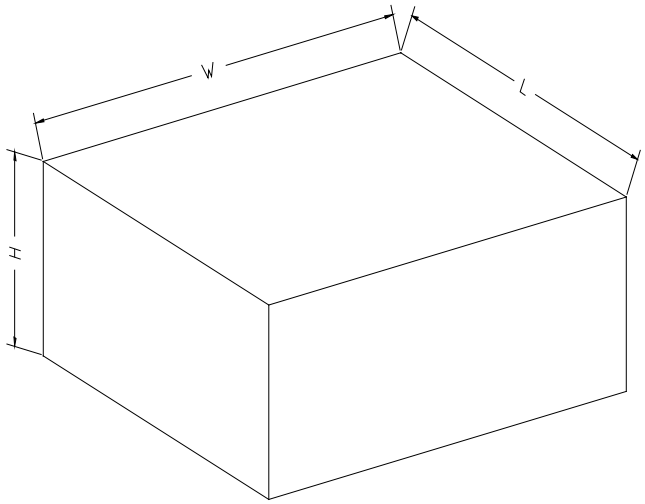
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.31×1.62-12B	7″	9.2	1.42	1.75	0.71	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002