SGM4062
Overvoltage and Overcurrent Protection IC and Li+ Charger Front-End Protection IC with LDO Mode

GENERAL DESCRIPTION

The SGM4062 is a charger front-end integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuitry. The IC continuously monitors the input voltage and the battery voltage. The device operates like a linear regulator, maintaining a 5.1V output with input voltages up to the Input overvoltage threshold (V_{OVP} = 6.8V). During input overvoltage conditions, the IC immediately turns off the internal pass FET disconnecting the charging circuitry from the damaging input source. Additionally, if the battery voltage rises to unsafe levels while charging, power is removed from the system. The IC checks for short-circuit or overload conditions at its output when turning the pass FET on, and if it finds unsafe conditions, it switches off, and then rechecks the conditions. Additionally, the IC also monitors its die temperature and switches off if it exceeds 150°C. When the IC is controlled by a processor, the IC provides status information about fault conditions to the host.

The SGM4062 is available in Green TDFN-2×2-8L package and is rated over the -40°C to +85°C temperature range.

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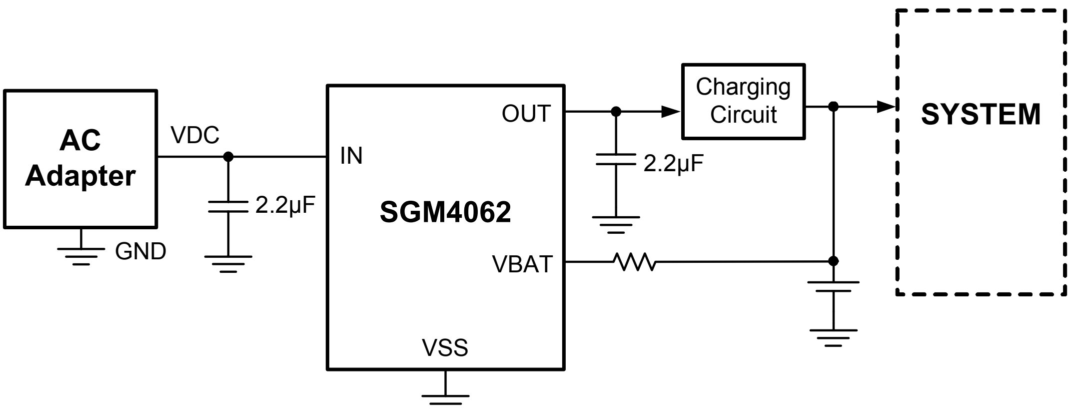
FEATURES

- **Input Overvoltage Protection**
- **Accurate Battery Overvoltage Protection**
- **Output Short-Circuit Protection**
- **Soft-Start to Prevent Inrush Currents**
- **Soft-Stop to Prevent Voltage Spikes**
- **24V Maximum Input Voltage**
- **Supports up to 1.5A Load Current**
- **Thermal Shutdown**
- **Enable Function**
- **Fault Status Indication**
- **Available in Green TDFN-2×2-8L Package**

APPLICATIONS

Smart Phones, Mobile Phones
PDAs
MP3 Players
Low-Power Handheld Devices

APPLICATION SCHEMATIC



PACKAGE/ORDERING INFORMATION

MODEL	ORDER NUMBER	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	PACKAGE OPTION	MARKING INFORMATION
SGM4062	SGM4062YDE8G/TR	TDFN-2×2-8L	-40℃ to +85℃	Tape and Reel, 3000	4062

ABSOLUTE MAXIMUM RATINGS

IN (with respect to VSS)…………………………...……-0.3V to 26V
OUT (with respect to VSS)…………………….............-0.3V to 6V
$\overline{\text{FAULT}}$, $\overline{\text{CE}}$, VBAT (with respect to VSS) ..…...........-0.3V to 6V
Output Source Current (OUT Pin)……………………….……….2A
Output Sink Current ($\overline{\text{FAULT}}$ Pin) …....…...….……………..15mA
Package Thermal Resistance
TDFN-2×2-8L, θ_{JA}……………………………….…………75℃/W
Storage Temperature Range..……….…...…... -65℃ to +150℃
Junction Temperature………………………...…………150℃
Operating Temperature Range………...………-40℃ to +85℃
Lead Temperature Range (Soldering 10 sec)
…………………………………………………….……….. 260℃
ESD Susceptibility
HBM…………………………………....……………………8000V
MM…………………………………………….……………400V

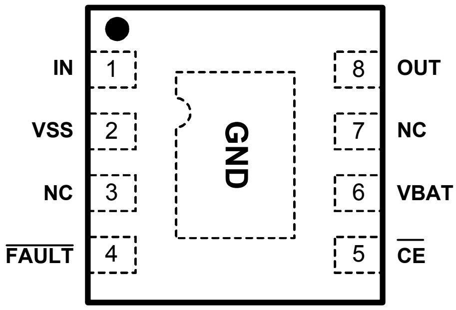
NOTE:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

PIN CONFIGURATION (TOP VIEW)



TDFN-2×2-8L

PIN DESCRIPTION

NUMBER	NAME	FUNCTION
1	IN	Input Power, Connected to External DC Supply. Bypass IN to VSS with a ceramic capacitor (1μF Min).
2	VSS	Ground Terminal. Connect to the thermal pad and to the ground rail of the circuit.
3, 7	NC	Do not connect to any external circuit.
4	$\overline{\text{FAULT}}$	Open-drain Device Status Output. $\overline{\text{FAULT}}$ is pulled to VSS internally when the input pass FET has been turned off due to input overvoltage or output short-circuit conditions, an over-temperature condition, or because the battery voltage is outside safe limits. $\overline{\text{FAULT}}$ is high impedance during normal operation.
5	$\overline{\text{CE}}$	Active-Low Chip Enable Input. Connect $\overline{\text{CE}}$ = "HIGH" to turn the input pass FET off. Connect $\overline{\text{CE}}$ = "LOW" to turn the internal pass FET on and connect the input to the charging circuitry. $\overline{\text{CE}}$ is Internally pulled down, pull down resistor is about 200kΩ.
6	VBAT	Battery Voltage Sense Input. Connected to pack positive terminal through a 100kΩ resistor.
8	OUT	Output Terminal to the Charging System. Bypass OUT to VSS with a ceramic capacitor (1μF Min).
Exposed Pad	GND	The thermal pad is electrically connected to VSS internally. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
IN Voltage Range	V_I	3.3	24	V
Current, OUT Pin	I_O		1.5	A
Junction Temperature	T_J	-40	125	℃

ELECTRICAL CHARACTERISTICS

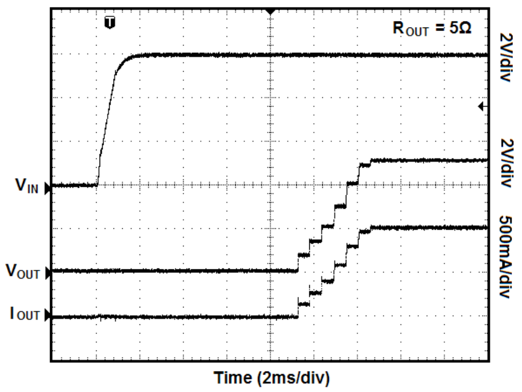
(Over junction temperature range -40℃ ≤ T_J ≤ +125℃ and typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
Under Voltage Lock Out, Input Power Detected Threshold	UVLO	$\overline{CE}$ = LOW, V_{IN} = 0V to 3V		2.65		V
Hysteresis on UVLO	$V_{hys(UVLO)}$	$\overline{CE}$ = LOW, V_{IN} = 3V to 0V		225		mV
Deglitch Time, Input Power Detected Status	$t_{DGL(PGOOD)}$	$\overline{CE}$ = LOW, Time measured from V_{IN} = 0V to 5V 1μs rise-time		9		ms
Operating Current	I_{DD}	$\overline{CE}$ = LOW, V_{IN} = 5V, no load on OUT pin		185		μA
Standby Current	I_{STDBY}	$\overline{CE}$ = HIGH, V_{IN} = 5.5V		0.6		μA
INPUT-TO-OUTPUT CHARACTERISTICS						
Dropout Voltage IN to OUT	V_{DO}	$\overline{CE}$ = LOW, V_{IN} = 5V, I_{OUT} = 1A		270		mV
Q1 Off-state Leakage Current	I_{OFF}	$\overline{CE}$ = LOW, V_{IN} = 5.5V				μA
INPUT OVERVOLTAGE PROTECTION						
Output Voltage	$V_{O(REG)}$	$\overline{CE}$ = LOW, V_{IN} = 5.5 to V_{OVP} - $V_{hys(OVP)}$		5.1		V
Input Overvoltage Protection Threshold	V_{OVP}	$\overline{CE}$ = LOW		6.8		V
Hysteresis on OVP	$V_{hys(OVP)}$	$\overline{CE}$ = LOW		155		mV
Input OV Propagation Delay	$t_{PD(OVP)}$ (1)	V_{IN} = 9V to 12V		200		ns
Recovery Time from Input Overvoltage Condition	$t_{REC(OVP)}$	$\overline{CE}$ = LOW, Time measured from V_{IN} = 12V to 9V 1μs fall-time		9		ms
OUTPUT SHORT-CIRCUIT PROTECTION (only at start-up)						
Short-Circuit Detection Threshold	$I_{O(SC)}$	V_{IN} = 5.5V		1.6		A
Retry Interval if Short-Circuit Detected	$t_{REC(SC)}$			64		ms
BATTERY OVERVOLTAGE PROTECTION						
Battery Overvoltage Protection Threshold	BV_{OVP}	$\overline{CE}$ = LOW, V_{OVP} - $V_{hys(OVP)}$ > V_{IN} > 4.5V		4.33		V
Hysteresis on BV_{OVP}	$V_{hys(BVovp)}$	$\overline{CE}$ = LOW, V_{OVP} - $V_{hys(OVP)}$ > V_{IN} > 4.5V		240		mV
Input Bias Current on VBAT Pin	I_{VBAT}	T_J = +25℃		20		nA
Deglitch Time, Battery Overvoltage Detected	$t_{DGL(BVovp)}$	V_{IN} > 4.5V, $\overline{CE}$ = LOW, Time measured from V_{VSAT} rising from 4.1V to 4.4V to $\overline{FAULT}$ going low.		170		μs
THERMAL PROTECTION						
Thermal Shutdown Temperature	$T_{J(OFF)}$			150		℃
Thermal Shutdown Hysteresis	$T_{J(OFF-HYS)}$			10		℃
LOGIC LEVELS ON $\overline{CE}$						
Logic LOW Input Voltage	V_{IL}				0.4	V
Logic HIGH Input Voltage	V_{IH}		1.4			V
Input LOW Current	I_{IL}			0.3		μA
Input HIGH Current	I_{IH}	$V_{\overline{CE}}$ = 1.8V		7.4		μA
LOGIC LEVELS ON $\overline{FAULT}$						
Output LOW Voltage	V_{OL}	I_{SINK} = 5mA		0.14		V
Off-state Leakage Current, HI-Z	I_{lkg}	$V_{\overline{FAULT}}$ = 5V		0.01		μA

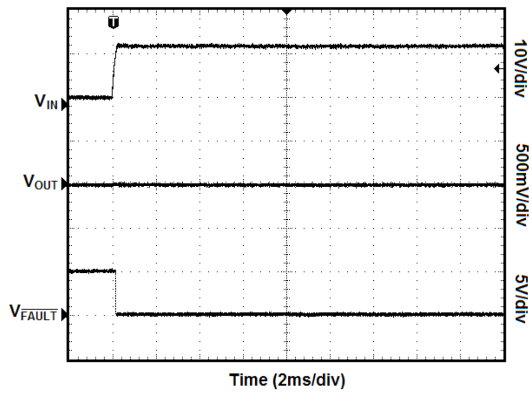
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25℃, C_{IN} = C_{OUT} = 2.2μF, unless otherwise noted.

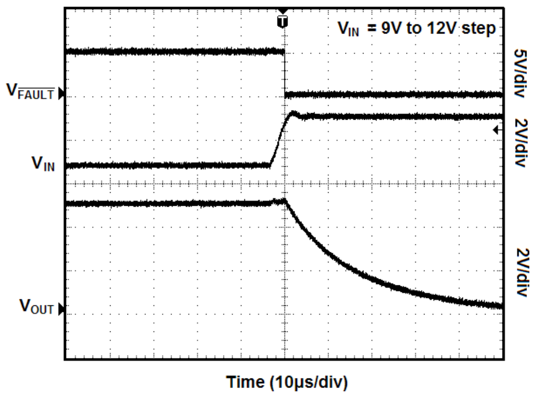
Normal Power-On Showing Soft-Start



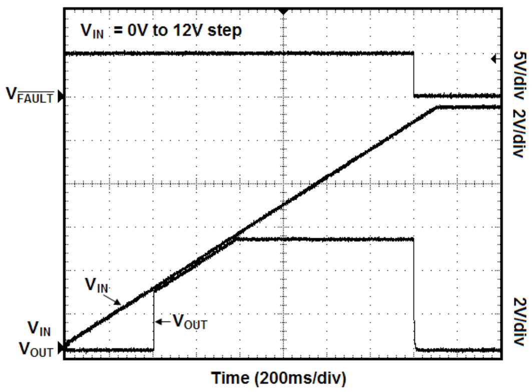
OVP at Power-On



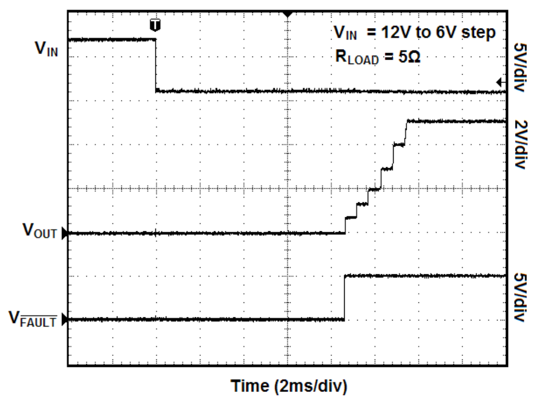
OVP Response for Input Step



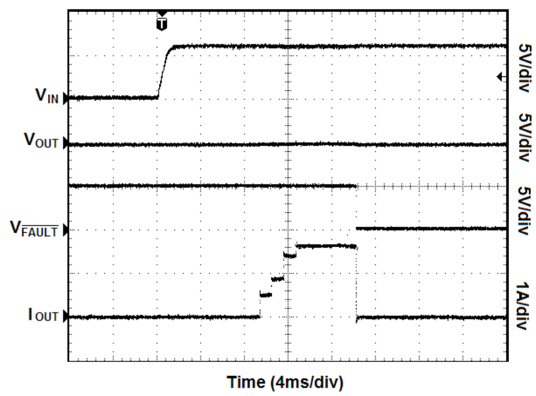
Slow Input Ramp into OVP Event



Recovery from OVP



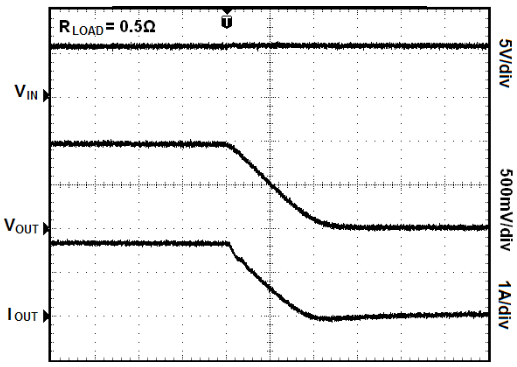
Power Up into Short Circuit



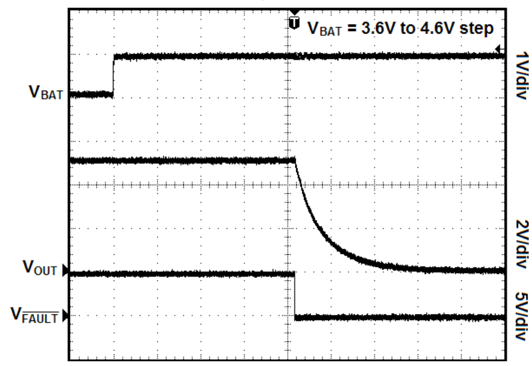
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25℃, C_{IN} = C_{OUT} = 2.2μF, unless otherwise noted.

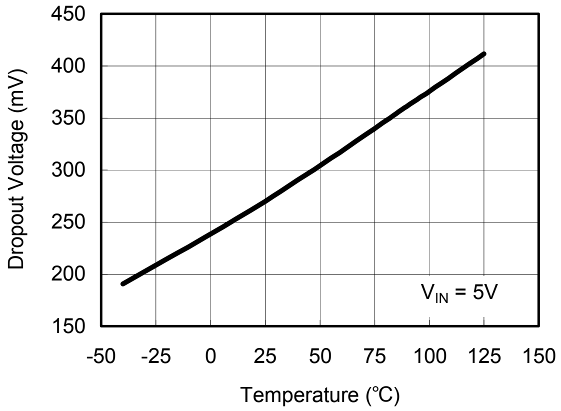
Soft-Stop during OCP Event



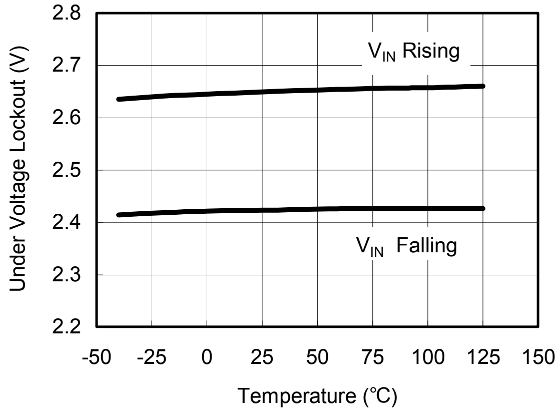
Battery OVP Event



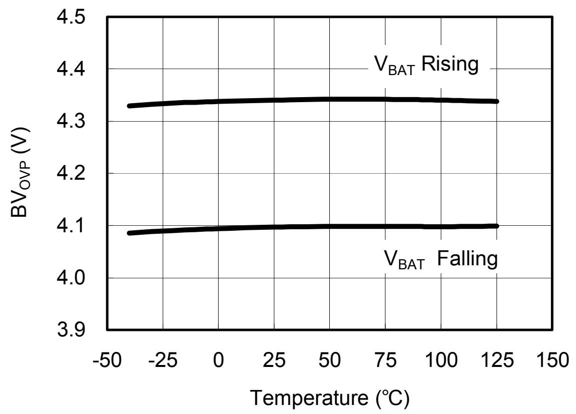
Dropout Voltage vs. Temperature



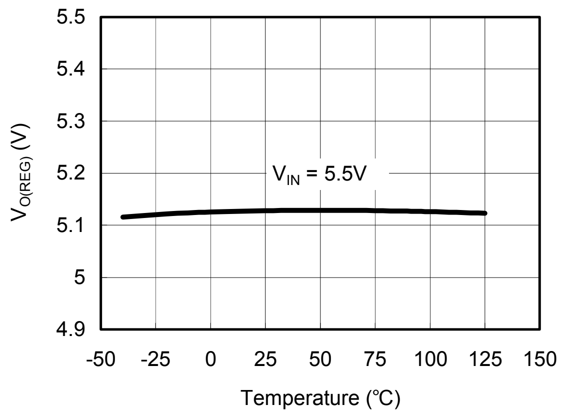
Under Voltage Lockout vs. Temperature



Battery Overvoltage Protection Threshold vs. Temperature

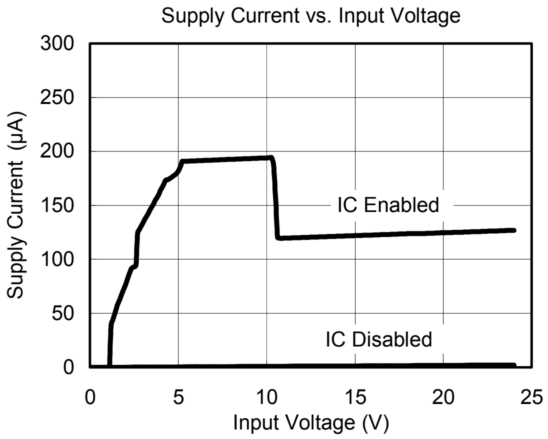


Output Voltage Regulation vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25℃, C_{IN} = C_{OUT} = 2.2μF, unless otherwise noted.



DETAILED FUNCTIONAL DESCRIPTION

The SGM4062 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit and the input source. The IC continuously monitors the input voltage and the battery voltage. The device operates like a linear regulator, maintaining a 5.1V output with input voltages up to the input overvoltage threshold (V_{OVP} = 6.8V). If the input voltage exceeds V_{OVP}, the IC shuts off the pass FET and disconnects the system from input power. Additionally, if the battery voltage rises above 4.33V, the IC switches off the pass FET, removing the power from the system until the battery voltage falls to safe levels. The IC also monitors its die temperature and switches the pass FET off if it exceeds 150°C.

The IC can be controlled by a processor, and also provides status information about fault conditions to the host.

Power Down

The device remains in power-down mode when the input voltage at the IN pin is below the undervoltage threshold (UVLO) of 2.65V. The FET connected between the IN and OUT pins is off, and the status output, $\overline{\text{FAULT}}$, is set to high impedance.

Power-On Reset

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. During power-on reset, the IC waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are within operation limits, the pass FET is turned ON. The IC has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input due to the resonant circuit formed by the parasitic inductance of the adapter cable and the input bypass capacitor. During the soft-start time, t_{SStart}, the current limit is increased in several steps. Each step is 625μs. After the soft-start sequence is over, the IC samples the load current. If the load current exceeds $I_{O(SC)}$, the IC initiates short circuit protection. See the Startup Short-Circuit Protection section for details. If no overcurrent event is measured, the current monitoring circuitry is disabled for normal operation.

In the event a short-circuit is detected at power-on, to prevent the input voltage from spiking up when the pass FET is switched off (due to the inductance of the input cable), the pass FET is turned off by gradually reducing its gate-drive, resulting in a soft-stop (t_{SStop}).

DETAILED FUNCTIONAL DESCRIPTION

The device continuously monitors the input voltage and the battery voltage as described in detail below:

Input Overvoltage Protection

The output voltage at OUT pin of the SGM4062 operates similar to a linear regulator. While the input voltage is less than $V_{O(REG)}$, and above the UVLO, the output voltage tracks the input voltage (less the drop caused by $R_{DS(on)}$ of the pass FET). When the input voltage is greater than $V_{O(REG)}$ (plus the $R_{DS(on)}$ drop) and less than V_{OVP}, the output voltage is regulated to $V_{O(REG)}$. $V_{O(REG)}$ is 5.1V for the SGM4062. If the input voltage is increased above V_{OVP}, the internal pass FET is turned off, removing power from the charging circuitry connected to OUT. The $\overline{\text{FAULT}}$ output is then asserted low. When the input voltage drops below V_{OVP} - $V_{hys(OVP)}$ (but is still above UVLO), the pass FET is turned on after a deglitch time of $t_{REC(OVP)}$. The deglitch time ensures that the input supply has stabilized.

Battery Overvoltage Protection

The battery overvoltage threshold BV_{OVP} is internally set to 4.33V for the SGM4062. If the battery voltage exceeds the BV_{OVP} threshold for longer than $t_{DGL(BVovp)}$, the pass FET is turned off (using soft-stop), and $\overline{\text{FAULT}}$ is asserted low. The pass FET is turned on (using the soft-start sequence) once the battery voltage drops to BV_{OVP} - $V_{hys(BVovp)}$.

Start-Up Short-Circuit Protection

The SGM4062 features overload current protection during start-up. If after the eight soft-start steps are complete, and the current limit is exceeded, the IC initiates a short-circuit check timer ($t_{CHK(SC)}$). During this check, the current is clamped to $I_{O(SC)}$. If the 5ms $t_{CHK(SC)}$ timer expires and the current remains clamped by the current limit, the internal pass FET is turned off using the soft-stop method, $\overline{\text{FAULT}}$ is pulled low and the $t_{REC(SC)}$ timer begins. Once the $t_{REC(SC)}$ timer expires, $\overline{\text{FAULT}}$ becomes high impedance and the soft-start sequence restarts. The device repeats the start/fail sequence until the overload condition is removed. Once the overload condition is removed, the current limit circuitry is disabled and the device enters normal operation. Additionally, if the current is not limited after the completion of the soft-start sequence, the $t_{CHK(SC)}$ timer does not start and the current limit circuitry is disabled for normal operation.

Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the pass FET is turned off, and the $\overline{\text{FAULT}}$ output is asserted low. The FET is turned on when the junction temperature falls below $T_{J(OFF)}$ - $T_{J(OFF-HYS)}$.

Enable Function

The IC has an enable pin which is used to enable and disable the device. Connect the $\overline{\text{CE}}$ pin high to turn off the internal pass FET. Connect the $\overline{\text{CE}}$ pin low to turn on the internal pass FET and enter the start-up routine. The $\overline{\text{CE}}$ pin has an internal pulldown resistor and can be left unconnected. The $\overline{\text{FAULT}}$ pin is high impedance when the $\overline{\text{CE}}$ pin is high.

Fault Indication

The $\overline{\text{FAULT}}$ pin is an active-low, open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting $\overline{\text{CE}}$ high. With $\overline{\text{CE}}$ low, the $\overline{\text{FAULT}}$ pin goes low whenever any of these events occurs:

1. Output short-circuit at power-on
2. Input overvoltage
3. Battery overvoltage
4. IC overtemperature

See Figure 2 for an example of $\overline{\text{FAULT}}$ conditions during these events. Connect the $\overline{\text{FAULT}}$ pin to the desired logic level voltage rail through a resistor between 1kΩ and 50kΩ.

APPLICATION INFORMATION

Selection of R_{BAT}

It is recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 24V, and applying 24V to the battery may cause failure of the device and can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in the event of failure. For safety, R_{BAT} must have a high value. The problem with a large R_{BAT} is that the voltage drops across the resistor because of the VBAT bias current, I_{VBAT}, which causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.33V BV_{OVP} threshold.

Choosing R_{BAT} in the range of 100kΩ to 470kΩ is a good compromise. If the IC fails with R_{BAT} equal to 100kΩ, the maximum current flowing into the battery would be (24V - 3V)/100kΩ = 210μA, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 100kΩ results in a worst-case voltage drop of $R_{BAT} \times I_{VBAT} \approx$ 2mV. This is negligible compared to the internal tolerance of 50mV on the BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin can either be connected to VSS or left floating.

Selection of R_{CE}

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left unconnected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As with the VBAT pin (see previous discussion), the $\overline{CE}$ pin must be connected to the host GPIO pin through as large a resistor as possible. The drop across the resistor is given by $R_{CE} \times I_{IH}$, the limitation of R_{CE} is computed by equation:

$$V_{OH} - R_{CE} \times I_{IH} > V_{IH}$$

V_{OH} is the voltage of logic High from host I/O.

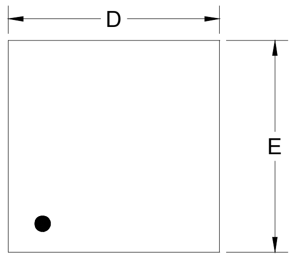
Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure 1 is for decoupling and serves an important purpose. Whenever a step change downwards in the system load current occurs, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from over-shooting to dangerous levels. It is recommended that a ceramic capacitor of at least 1μF be used at the input of the device. It must be located in close proximity to the IN pin.

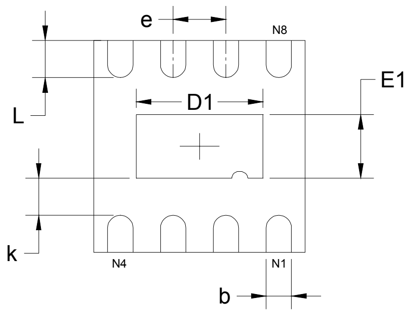
C_{OUT} in Figure 1 is also important. During an overvoltage transient, this capacitance limits the output overshoot until the power FET is turned off by the overvoltage protection circuitry. C_{OUT} must be a ceramic capacitor of at least 1μF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

PACKAGE OUTLINE DIMENSIONS

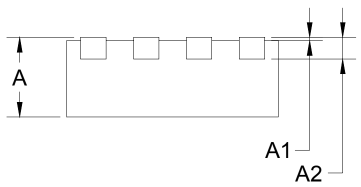
TDFN-2×2-8L



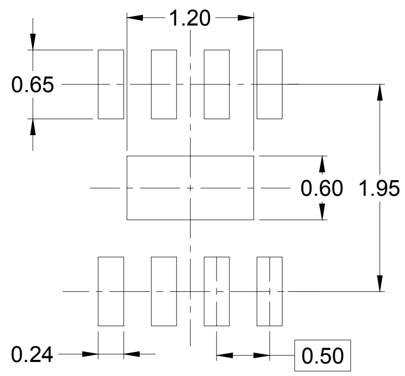
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	**MAX**	**MIN**	**MAX**
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E	1.900	2.100	0.075	0.083
E1	0.500	0.700	0.020	0.028
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.250	0.450	0.010	0.018