SGM40656/SGM40657/SGM40658
High-Current Over-Voltage Protector
Upgrade Replacement to *14653/4/5

GENERAL DESCRIPTION

The SGM40656/7/8 over-voltage protection devices feature a low 25mΩ (TYP) R_{ON} internal FET and protect low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the devices from surges up to +120V. When the input voltage exceeds the over-voltage threshold, the internal FET is turned off to prevent damage to the protected downstream components.

The over-voltage protection threshold can be adjusted with optional external resistors to any voltage between 4V and 20V. With the OVLO input set below the external OVLO select voltage, the SGM40656/7/8 automatically choose the accurate internal trip thresholds. The internal over-voltage thresholds (OVLO) are preset to 15.39V/6.8V/5.95V typical (SGM40656/7/8). The devices feature an open-drain nACOK output indicating a stable supply between minimum supply voltage and V_{OVLO}. The SGM40656/7/8 are also protected against over-current events by an internal thermal shutdown.

The SGM40656/7/8 are available in Green 12-Ball CSP package and operate over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Protect High-Power Portable Devices**
  - **Wide Operating Input Voltage Protection from 2.5V to 28V**
  - **Integrated 25mΩ (TYP) N-Channel MOSFET Switch**
- **Flexible Overvoltage Protection Design**
  - **Adjustable Over-Voltage Protection Trip Level**
  - **Wide Adjustable OVLO Threshold Range from 4V to 20V**
  - **Preset Internal Accurate OVLO Thresholds:**
    15.39V (SGM40656)
    6.8V (SGM40657)
    5.95V (SGM40658)
- **Additional Protection Features Increase System Reliability**
  - **Surge Immunity to +120V**
  - **Soft-Start to Minimize In-Rush Current**
  - **Internal 18.5ms Startup Debounce**
  - **Thermal Shutdown Protection**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green WLCSP-1.30×1.83-12B Package**

APPLICATIONS

Smart Phones
Tablet PCs
Mobile Internet Devices

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PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM40656	WLCSP-1.30×1.83-12B	-40℃ to +85℃	SGM40656YG/TR	XXXXX GM2YG	Tape and Reel, 5000
SGM40657	WLCSP-1.30×1.83-12B	-40℃ to +85℃	SGM40657YG/TR	XXXXX GM3YG	Tape and Reel, 5000
SGM40658	WLCSP-1.30×1.83-12B	-40℃ to +85℃	SGM40658YG/TR	XXXXX GM4YG	Tape and Reel, 5000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN (with respect to GND)..... -0.3V to 28V
IN (with respect to GND)..... +120V, 1.2/50μs, 2Ω surge (1) (2)
OUT (with respect to GND)..... -0.3V to V_{IN} + 0.3V
OVLO..... -0.3V to 26.4V
nACOK (with respect to GND)..... -0.3V to 6V
Continuous IN, OUT Current (3)..... 4.5A
Peak IN, OUT Current (10ms)..... 8A
Junction Temperature..... +150℃
Storage Temperature Range..... -65℃ to +150℃
Lead Temperature (Soldering 10 sec)..... +260℃

NOTES:
1. Surge pulse in compliance with ICE61000-4-5 specification.
2. Survives burst pulse up to +120V with 2Ω series resistance.
3. Continuous current limited by thermal design.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range..... 2.5V to 28V
Operating Temperature Range..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

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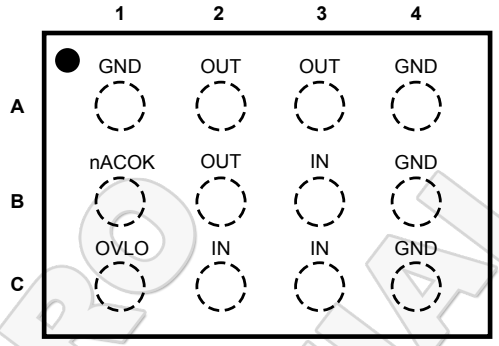
PIN CONFIGURATION

SGM40656/7/8 (TOP VIEW)



WLCSP-1.30×1.83-12B

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1, A4, B4, C4	GND	Ground. Connect GND pins together for proper operation.
A2, A3, B2	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.
B1	nACOK	Open-Drain Flag Output. nACOK is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce. Connect a pull-up resistor from nACOK to the logic I/O voltage of the host system. nACOK is high impedance after thermal shutdown.
B3, C2, C3	IN	Input Voltage. Bypass IN with a 0.1μF ceramic capacitor as close as possible to the device. Connect IN pins together for proper operation.
C1	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.

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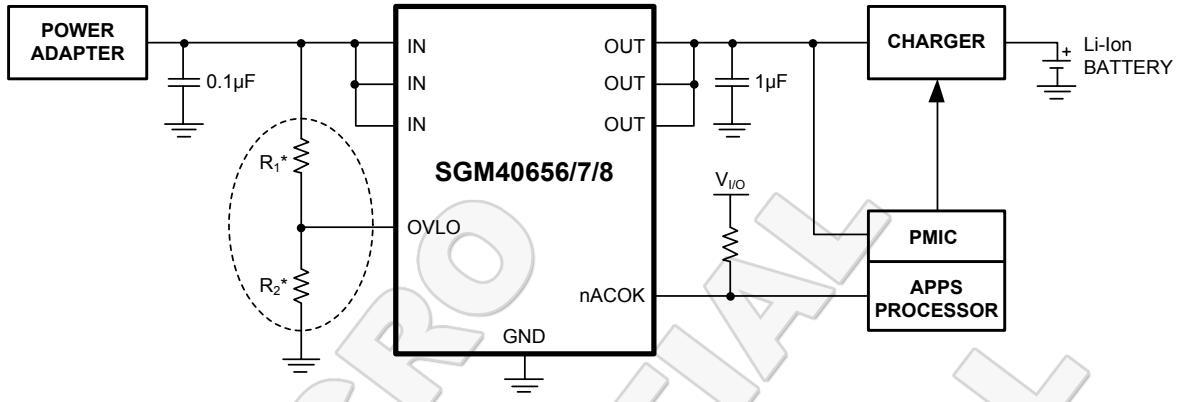
TYPICAL APPLICATION



* R_1 and R_2 are only required for adjustable OVLO; otherwise, connect OVLO to GND.

Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

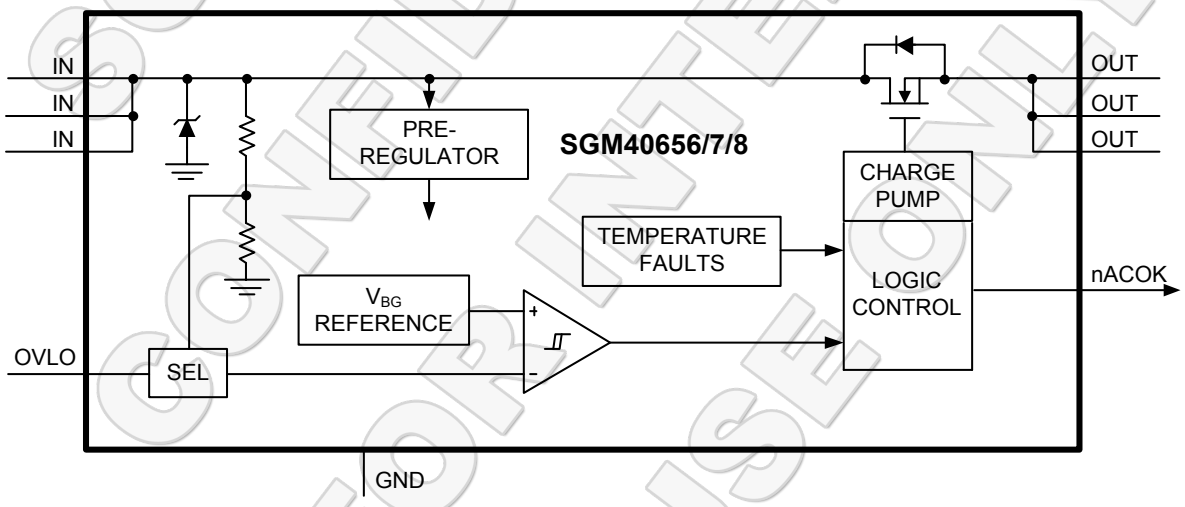


Figure 2. Block Diagram

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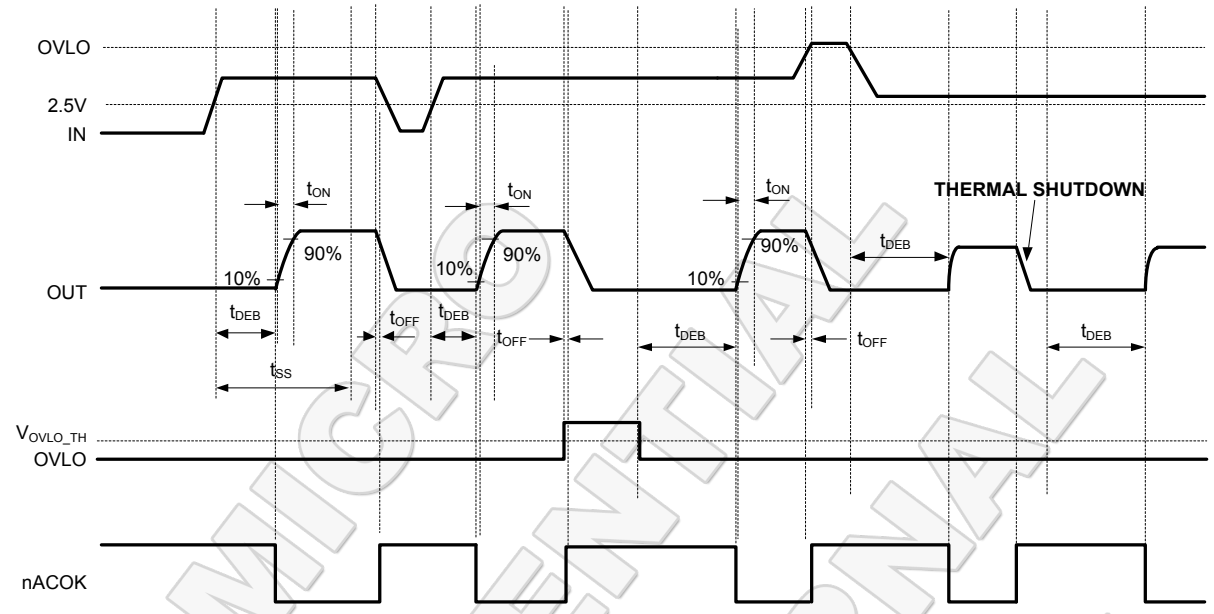
TIMING DIAGRAM



NOTE: Waveforms are not to scale.

Figure 3. Timing Diagram

SURGE UP TEST CIRCUIT

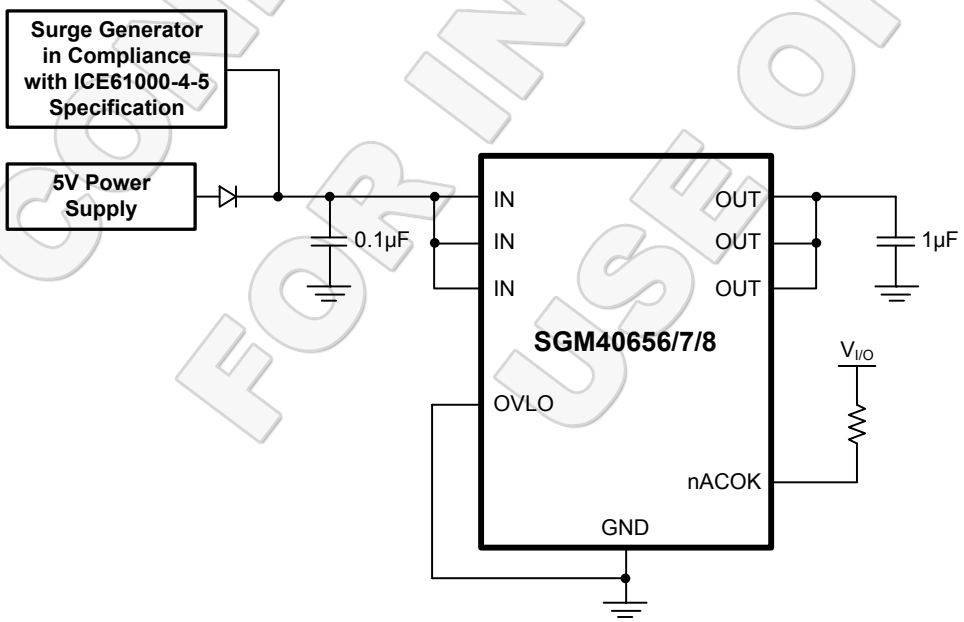


Figure 4. Surge Up Test Circuit

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DETAILED DESCRIPTION

The SGM40656/7/8 over-voltage protection devices feature a low on-resistance (R_{ON}) internal FET and protect low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the devices from surges up to +120V. Surge up tests are operated according to the test circuit in Figure 4. If the input voltage exceeds the over-voltage threshold, the internal FET is turned off to prevent damage to the protected components. The 18.5ms (TYP) debounce time built into the device prevents false turn on of the internal FET during startup.

Device Operation

The devices contain timing logic that controls the turn-on of the internal FET. The internal charge pump is enabled when $V_{IN} < V_{IN\_OVLO}$ if internal trip thresholds are used or when $V_{IN} < V_{OVLO\_TH}$ if external trip thresholds are used. The charge-pump startup, which occurs after a 18.5ms (TYP) debounce delay, turns the internal FET on (see Figure 2). After the debounce time, soft-start limits the FET inrush current for 18.5ms (TYP). At any time, if V_{IN} rises above V_{OVLO_THRESH}, OUT is disconnected from IN.

Internal Switch

The SGM40656/7/8 incorporate an internal FET with a 25mΩ (TYP) R_{ON}. The FET is internally driven by a charge pump that generates a necessary gate voltage above IN.

Over-Voltage Lockout (OVLO)

The SGM40656/7/8 has 15.39V/6.8V/5.95V (TYP) over-voltage threshold (OVLO).

Thermal Shutdown Protection

The SGM40656/7/8 feature thermal shutdown circuitry. The internal FET turns off when the junction temperature exceeds +138℃ (TYP). The device exits thermal shutdown after the junction temperature cools by +30℃ (TYP).

nACOK Output

An open-drain nACOK output gives the SGM40656/7/8 the ability to communicate a stable power source to the host system. nACOK is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce. Connect a pullup resistor from nACOK to the logic I/O voltage of the host system. nACOK is high impedance after thermal shutdown.

USB OTG Support

When used in an OTG application the SGM40656/7/8 can provide power from OUT to IN. Initially, the OTG voltage applied at OUT will forward bias the power switch bulk diode and present a voltage drop of approximately 0.7V between OUT and IN. This is purely a transitionary condition as once the voltage at IN exceeds the UVLO voltage of 2.4V (TYP) and the debounce time has elapsed, the main power switch will turn fully ON, significantly reducing the voltage drop from OUT to IN. In this mode，the part is able to supply the continuous current of 3.5A (TDFN package) to the OTG load.

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APPLICATION INFORMATION

Bypass Capacitor

For most applications, bypass IN to GND with a 0.1μF ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length, the device clamps the overshoot due to LC tank circuit.

Output Capacitor

The slow turn-on time provides a soft-start function that allows the SGM40656/7/8 to charge an output capacitor up to 1000μF without turning off due to an over-current condition.

External OVLO Adjustment Functionality

If OVLO is connected to ground, the internal OVLO comparator uses the internally set OVLO value.

If an external resistor-divider is connected to OVLO and V_{OVLO} exceeds the OVLO select voltage, V_{OVLO_SELECT}, the internal OVLO comparator reads the IN fraction fixed by the external resistor divider. R_1 = 1MΩ is a good starting value for minimum current consumption. Since V_{IN_OVLO}, V_{BG}, and R_1 are known, R_2 can be calculated from the following formula:

$$V_{IN\_OVLO} = V_{BG} \times \left[1 + \frac{R_1}{R_2}\right]$$

This external resistor-divider is completely independent from the internal resistor-divider.

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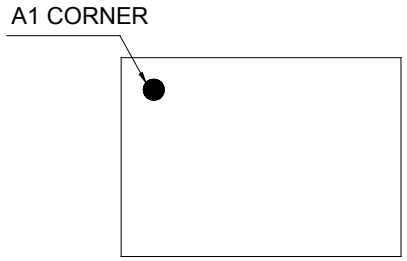
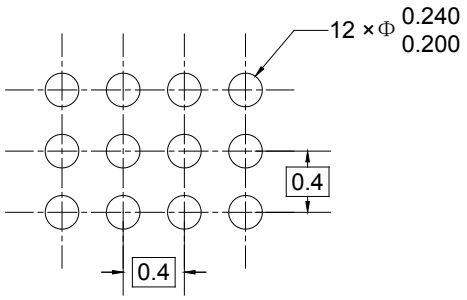
PACKAGE OUTLINE DIMENSIONS

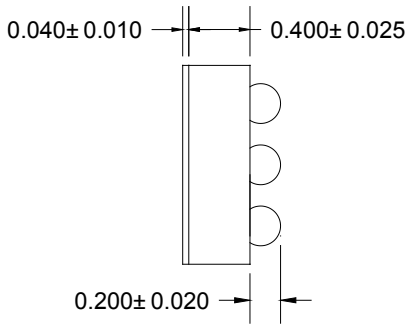
WLCSP-1.30×1.83-12B



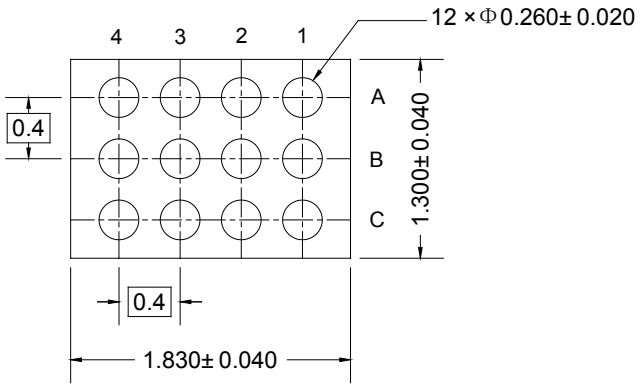
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

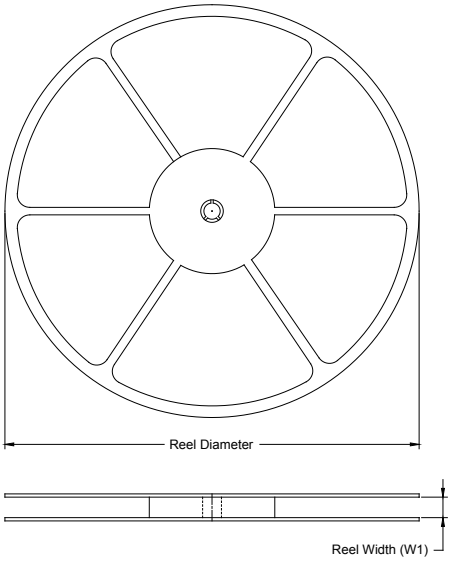


BOTTOM VIEW

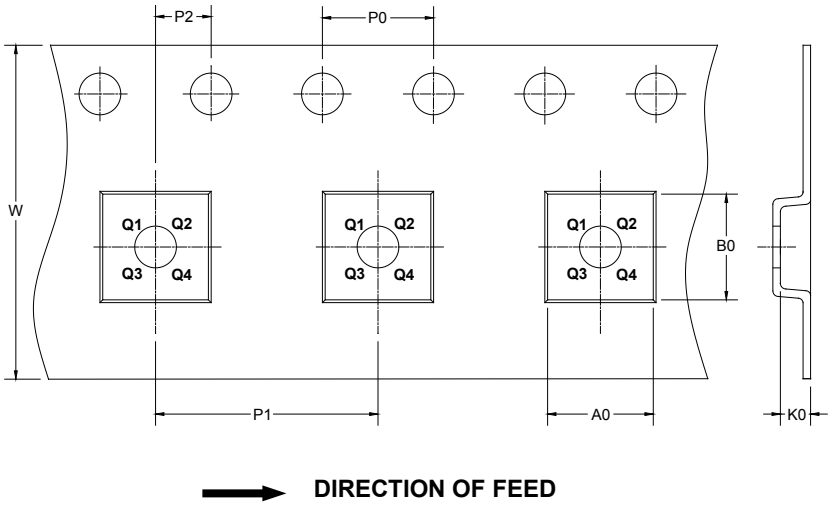
NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



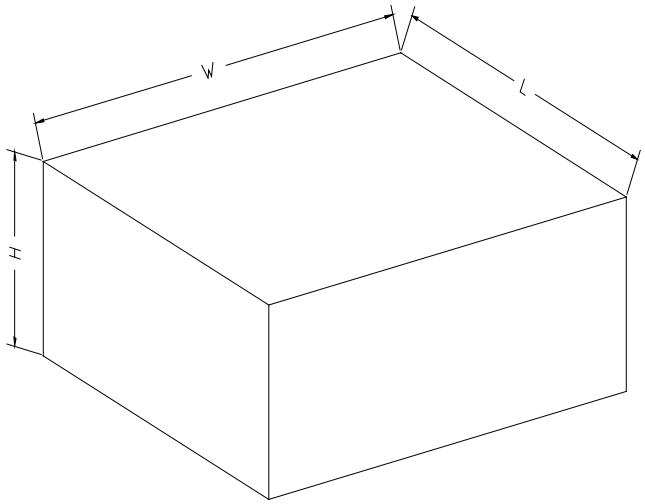
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.30×1.83-12B	7″	9.2	1.40	2.00	0.80	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002