SGM3838
Triple-Output 700mA AMOLED Display Power Supply

GENERAL DESCRIPTION

The SGM3838 is designed for powering AMOLED displays which requires V_{ELVDD}, V_{ELVSS} and V_{AVDD}. The device integrates two boost converters, VO1 for V_{ELVDD} and VO3 for V_{AVDD}, and a dual-phase inverting buck-boost converter VO2 for V_{ELVSS}. Output voltages of all the three converters can be programmed in digital steps through the digital interface control pin (SWIRE).

The SGM3838 is available in a Green WLCSP-2.5×2.5-36B package.

FEATURES

- **2.5V to 4.8V Input Supply Voltage Range**
- **Synchronous Boost Converter (ELVDD)**
  - **4.6V to 5.0V Output Voltage with 100mV Step**
  - **4.6V Default Output Voltage**
  - **0.5% Accuracy at 4.6V**
  - **700mA Output Current Capability**
  - **Output Voltage Sensing Pin for Path Loss Compensation (FBS)**
- **Synchronous Inverting Buck-Boost Converter (ELVSS)**
  - **-6.0V to -0.8V Output Voltage with 100mV Step**
  - **-3.0V Default Output Voltage**
  - **1% Accuracy at -3V**
  - **700mA Output Current Capability**
- **Synchronous Boost Converter (AVDD)**
  - **5.5V to 7.9V Output Voltage with 100mV Step**
  - **7.3V Default Output Voltage**
  - **1% Accuracy at 7.3V**
  - **150mA Output Current Capability**
- **V_{IN} and V_{OUT} Bi-Directional Isolation**
- **Short Circuit Protection (SCP)**
- **Overload Protection**
- **Thermal Shutdown**
- **V_{ELVSS} Start-Up Delay: 5ms**
- **Short Circuit and OLP Detect Time: 0.6ms**
- **Available in a Green WLCSP-2.5×2.5-36B Package**

APPLICATIONS

Smartphones & Tablets
Active Matrix OLED Displays

TYPICAL APPLICATION

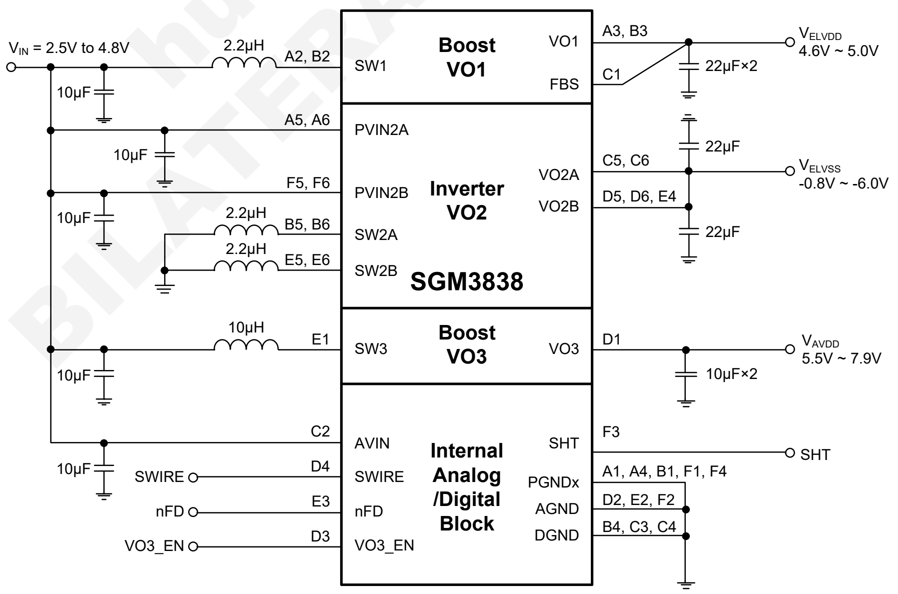


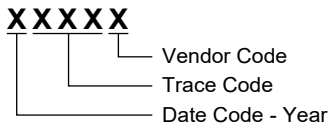
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3838	WLCSP-2.5×2.5-36B	-40℃ to +85℃	SGM3838YG/TR	SGM 3838YG XXXXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

PVIN2A, PVIN2B, AVIN, VO3_EN, SWIRE, nFD, VO1, FBS, SHT Voltages (1) ..... -0.3V to 6V
SW1 Voltage (1) ..... -0.3V to 7V
SW3, VO3 Voltages (1) ..... -0.3V to 9V
VO2A, VO2B Voltages (1) ..... -7V to 0.3V
SW2A, SW2B Voltages (1) ..... -7V to 6V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTE:
1. All voltages are with respect to network ground pin.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

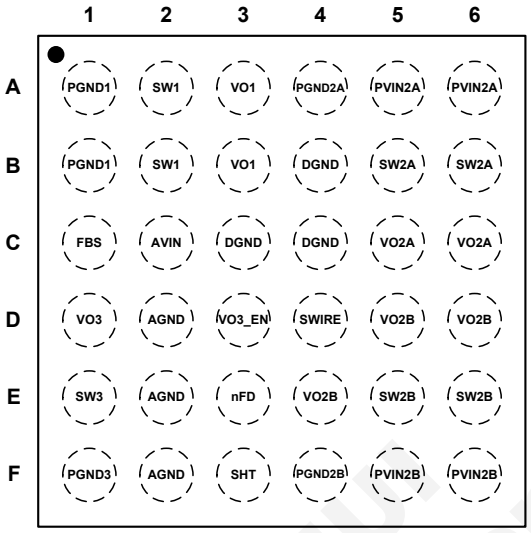
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.5×2.5-36B

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
A1, B1	PGND1	G	VO1 Boost Converter Power Ground.
C1	FBS	I	VO1 Boost Converter Output Sense Input (if connected externally to VO1). If connected to GND, internal feedback sensing.
D1	VO3	O	VO3 Boost Converter Output.
E1	SW3	I	VO3 Boost Converter Switching Node.
F1	PGND3	G	VO3 Boost Converter Power Ground.
A2, B2	SW1	I	VO1 Boost Converter Switching Node.
C2	AVIN	I	Analog Input Pin.
D2, E2, F2	AGND	G	Analog Ground Pin.
A3, B3	VO1	O	VO1 Boost Converter Output.
C3	DGND	G	Digital Ground Pin.
D3	VO3_EN	I	VO3 Boost Converter Enable Pin.
E3	nFD	I	Output Discharge Enable/Disable During Shutdown. Logic low level enables the discharge and logic high level disables the discharge.
F3	SHT	O	Fault Protection (SCP, UVLO) Status Pin.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	DESCRIPTION
A4	PGND2A	G	Power Ground Pin.
B4, C4	DGND	G	Digital Ground Pin.
D4	SWIRE	I	VO1/VO2 Converter Enable Pin.
E4	VO2B	O	VO2 Inverting Buck-Boost Converter B Output Pin.
F4	PGND2B	G	Power Ground Pin.
A5	PVIN2A	I	VO2 Inverting Buck-Boost Converter A Power Supply Input Pin.
B5	SW2A	I	VO2 Inverting Buck-Boost Converter A Switching Node.
C5	VO2A	O	VO2 Inverting Buck-Boost Converter A Output Pin.
D5	VO2B	O	VO2 Inverting Buck-Boost Converter B Output Pin.
E5	SW2B	I	VO2 Inverting Buck-Boost Converter B Switching Node.
F5	PVIN2B	I	VO2 Inverting Buck-Boost Converter B Power Supply Input Pin.
A6	PVIN2A	I	VO2 Inverting Buck-Boost Converter A Power Supply Input Pin.
B6	SW2A	I	VO2 Inverting Buck-Boost Converter A Switching Node.
C6	VO2A	O	VO2 Inverting Buck-Boost Converter A Output Pin.
D6	VO2B	O	VO2 Inverting Buck-Boost Converter B Output Pin.
E6	SW2B	I	VO2 Inverting Buck-Boost Converter B Switching Node.
F6	PVIN2B	I	VO2 Inverting Buck-Boost Converter B Power Supply Input Pin.

NOTE: I: input; O: output; I/O: input or output. G: Ground.

ELECTRICAL CHARACTERISTICS

(At T_J = +25℃, V_{IN} = 3.7V, V_{SWIRE} = V_{VO3_EN} = V_{IN}, V_{VO1} = 4.6V, V_{VO2} = -3V, V_{VO3} = 7.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current and Thermal Protection						
Input Voltage Range	V_{IN}		2.5		4.8	V
Shutdown Current into PVIN, AVIN	I_{SD}	V_{SWIRE} = V_{VO3_EN} = GND		0.5		μA
Quiescent Current into PVIN, AVIN	I_{QON}	V_{IN} = 3.7V, no load, V_{SWIRE} = V_{VO3_EN} = high		6		mA
Under-Voltage Lockout Threshold (AVIN)	V_{IT-}	V_{IN} falling		2.23		V
	V_{IT+}	V_{IN} rising		2.35		V
Thermal Shutdown Temperature	TSD	Junction temperature rising		145		℃
		Junction temperature falling		135		℃
Logic Signals (VO3_EN, SWIRE)						
Logic High Level Voltage	V_H	V_{IN} = 2.7V to 4.8V	1.2			V
Logic Low Level Voltage	V_L	V_{IN} = 2.7V to 4.8V			0.4	V
Pull-Down Resistor (VO3_EN, SWIRE)	R_{DOWN}			580		kΩ
Logic Signal (SHT)						
Pull-Up Resistor to AVIN	R_{UP}			330		kΩ
Pull-Down Current	I_{DOWN}	V_{IN} = 3.7V, output short, V_{SHT} = 1V		5.8		mA
Boost Converter (V_{VO1} = V_{ELVDD})						
Positive Output 1 Voltage	V_{VO1}	4.6V to 5.0V with 0.1V/step, default 4.6V	4.6	4.6	5.0	V
Positive Output 1 Voltage Accuracy		V_{VO1} = 4.6V, no load		±0.5		%
		V_{VO1} = 4.6V, no load, -40℃ ≤ T_J ≤ +85℃		±0.8		
SW1 MOSFET On-Resistance	$R_{DS(ON)11}$	I_{DS} = 100mA		70		mΩ
SW1 MOSFET Rectifier On-Resistance	$R_{DS(ON)12}$	I_{DS} = 100mA		160		
SW1 Switch Current Limit	I_{SW1}	Inductor valley current		2.0		A
SW1 Switching Frequency	f_{SW1}	I_{VO1} = 100mA		1.45		MHz
Output Current Capability	I_{OUT1}	V_{IN} = 2.7V to 4.8V	700			mA
Short Circuit Threshold in Operation	$V_{VO1(SCP)}$	Percentage of nominal V_{VO1}		81		%
Threshold of Output Sense with VO1	V_{TVO1}	V_{VO1} - V_{FBS} increasing		660		mV
Threshold of Output Sense with FBS	V_{TFBS}	V_{VO1} - V_{FBS} decreasing		460		mV
VO1 and FBS Leakage, No Discharge	I_{LEAK_VO1}	V_{SWIRE} = GND		0.8		μA
Pull-Down Resistance of FBS	R_{FBS}			5		MΩ
VO1 Discharge Resistance	$R_{VO1(DCG)}$	V_{SWIRE} = GND, I_{VO1} = 20mA		60		Ω
VO1 Discharge Time	t_{DVO1}	V_{SWIRE} = GND		10		ms
Line Regulation	$VO1_{LINEREG}$	I_{VO1} = 100mA, V_{IN} = 2.7V to 4.5V		±0.003		%/V
Line Regulation	$VO1_{LINEREG}$	No load, V_{IN} = 2.7V to 4.5V		±0.002		%/V
Output Voltage Ripple	$VO1_{RIPPLE}$	I_{VO1} = I_{VO2} = 0 to 150mA		10		mV_{PP}
Load Regulation	$VO1_{LOADREG}$	1mA ≤ I_{VO1} ≤ 700mA		±0.01		%/A

ELECTRICAL CHARACTERISTICS (continued)

(At T_J = +25℃, V_{IN} = 3.7V, V_{SWIRE} = V_{VO3_EN} = V_{IN}, V_{VO1} = 4.6V, V_{VO2} = -3V, V_{VO3} = 7.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Buck-Boost Converter (V_{VO2} = V_{ELVSS})						
Negative Output Voltage Range	V_{VO2}	-6.0V to -0.8V with 0.1V/step, default -3.0V	-6.0	-3.0	-0.8	V
Negative Output Voltage Accuracy		V_{VO2} = -3V, no load, -40℃ ≤ T_J ≤ +85℃		±30		mV
SW2 MOSFET On-Resistance-Phase A	$R_{DS(ON)A1}$	I_{DS} = 100mA		130		mΩ
SW2 MOSFET Rectifier On-Resistance-Phase A	$R_{DS(ON)A2}$	I_{DS} = 100mA		120		
SW2 MOSFET On-Resistance-Phase B	$R_{DS(ON)B1}$	I_{DS} = 100mA		130		mΩ
SW2 MOSFET Rectifier On-Resistance-Phase B	$R_{DS(ON)B2}$	I_{DS} = 100mA		120		
SW2 Switching Frequency	f_{SW2}	I_{VO2} = 100mA		1.25		MHz
Output Current Capability	I_{OUT2}	V_{IN} = 2.7V to 4.8V	700			mA
SW2 Switch Current Limit-Phase A	I_{SW2A}	Inductor peak current		2.8		A
SW2 Switch Current Limit-Phase B	I_{SW2B}	Inductor peak current		2.8		A
Average Load Current Threshold with Dual-Phase	$I_{RMSA\&B}$	Load current rising		260		mA
Average Load Current Threshold with Phase A Only	I_{RMSA}	Load current falling		150		mA
Short Circuit Threshold during start-up after 20ms	$V_{VO2(SCP)}$	Percentage of nominal V_{VO2}		82		%
VO2 Discharge Resistance	$R_{VO2(DCG)}$	V_{SWIRE} = GND, I_{VO2} = 20mA		60		Ω
VO2 Discharge Time	t_{DVO2}	V_{SWIRE} = GND		10		ms
VO2 Leakage, No Discharge	I_{LEAK_VO2}	V_{SWIRE} = GND		0.5		μA
Line Regulation	$VO2_{LINEREG}$	I_{VO2} = 100mA, V_{IN} = 2.7V to 4.5V		0.018		%/V
Output Voltage Ripple	$VO2_{RIPPLE}$	I_{VO1} = I_{VO2} = 0 to 150mA		10		mV_{PP}
Load Regulation	$VO2_{LOADREG}$	1mA ≤ I_{VO2} ≤ 700mA		0.15		%/A
Boost Converter (V_{VO3} = V_{AVDD})						
Positive Output 2 Voltage Range	V_{VO3}	5.5V to 7.9V with 0.1V/step, default 7.3V	5.5	7.3	7.9	V
Positive Output 2 Voltage Accuracy		V_{VO3} = 7.3V, no load, -40℃ ≤ T_J ≤ +85℃		±1		%
SW3 MOSFET On-Resistance	$R_{DS(ON)31}$	I_{DS} = 100mA		340		mΩ
SW3 MOSFET Rectifier On-Resistance	$R_{DS(ON)32}$	I_{DS} = 100mA		520		
SW3 Switch Current Limit	I_{SW3}	Inductor peak current		0.95		A
SW3 Switching Frequency	f_{SW3}	I_{VO3} = 30mA		1.45		MHz
Output Current Capacity	I_{OUT3}	V_{IN} = 2.7V to 4.8V	150			mA
Short Circuit Threshold in Operation	$V_{VO3(SCP)}$	Percentage of nominal V_{VO3}		88		%
VO3 Leakage, No Discharge	I_{LEAK_VO3}	V_{FD} = GND, V_{VO3_EN} = GND		2		μA
VO3 Discharge Resistance	$R_{VO3(DCG)}$	V_{VO3_EN} = GND, I_{VO3} = 20mA		150		Ω
VO3 Discharge Time	t_{DVO3}	V_{VO3_EN} = GND		10		ms
Line Regulation	$VO3_{RIPPLE}$	I_{VO3} = 30mA, V_{IN} = 2.7V to 4.5V		0.008		%/V
Load Regulation	$VO3_{LOADREG}$	1mA ≤ I_{VO3} ≤ 150mA		0.11		%/A

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Short-Circuit Timer					
VO1 Short Circuit Detection Time in Start-Up	$t_{VO1(SCP)}$		1.6		ms
VO1 Short Circuit Detection Time in Operation			0.6		
VO2 Short Circuit Detection Time in Start-Up	$t_{VO2(SCP)}$		5		
VO2 Short Circuit Detection Time in Operation			0.6		
VO3 Short Circuit Detection Time in Start-Up	$t_{VO3(SCP)}$		2.6		
VO3 Short Circuit Detection Time in Operation			0.6		
VOx Discharge Time after SWIRE Goes Low	t_{DISCHG}		10		
SWIRE Interface					
Initialization Time	t_{INIT}		350		μs
Shutdown Time Period	t_{OFF}		55		
Pulse High Level Time Period	t_{HIGH}		10		
Pulse Low Level Time Period	t_{LOW}		10		
Data Storage/Accept Time Period	t_{STORE}		55		
Power Sequence					
VO1 Start-Up Time	t_{SS1}		2.5		ms
VO2 Start-Up Time	t_{SS2}		2		
VO2 Start-Up Time Delay after VO1	t_{DELAY}		2.5		

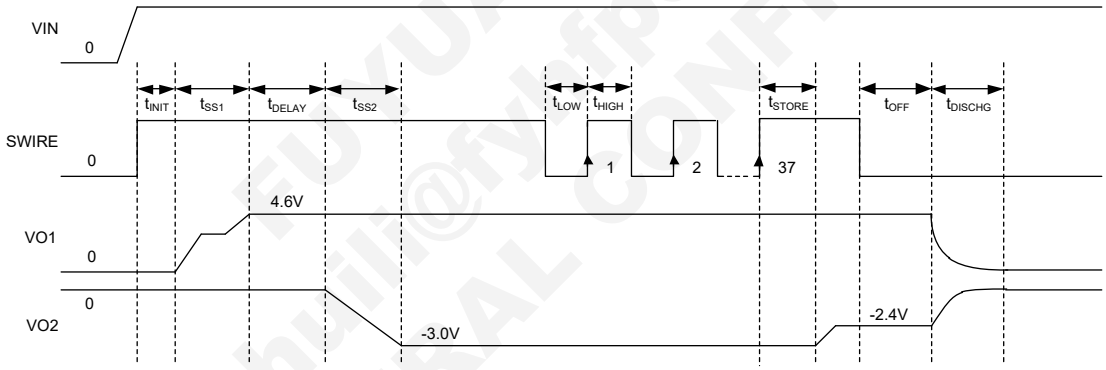


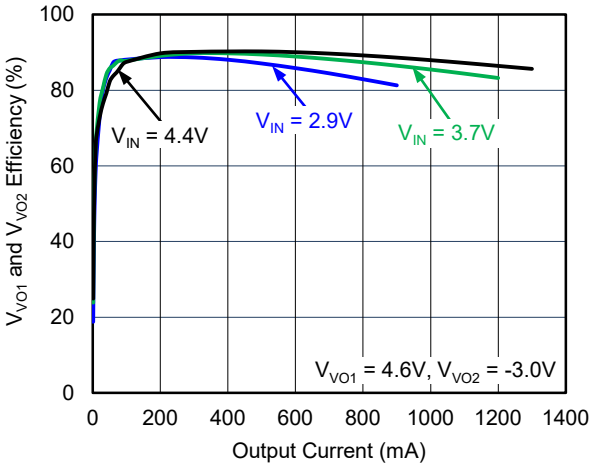
Figure 2. Timing Diagram

Figure 3. V_{ELVSS} Transition Time Control

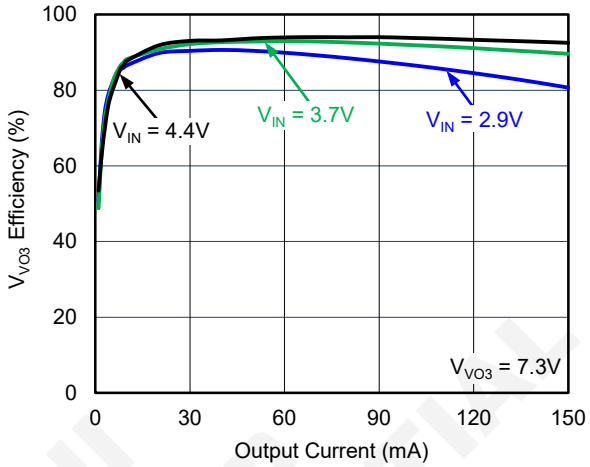
TYPICAL PERFORMANCE CHARACTERISTICS

At T_J = +25℃, V_{IN} = 3.7V, unless otherwise noted.

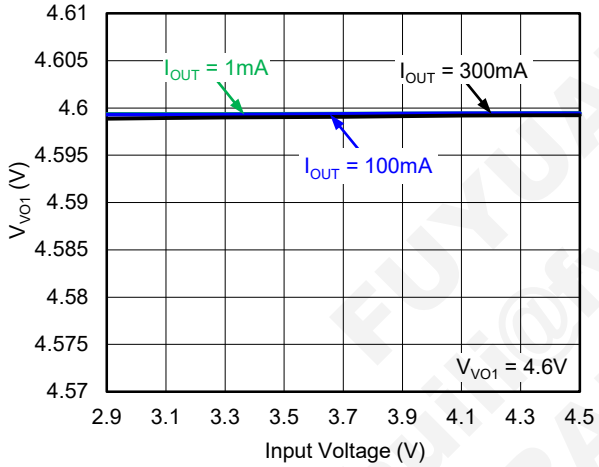
V_{VO1} and V_{VO2} Combined Efficiency vs. Output Current



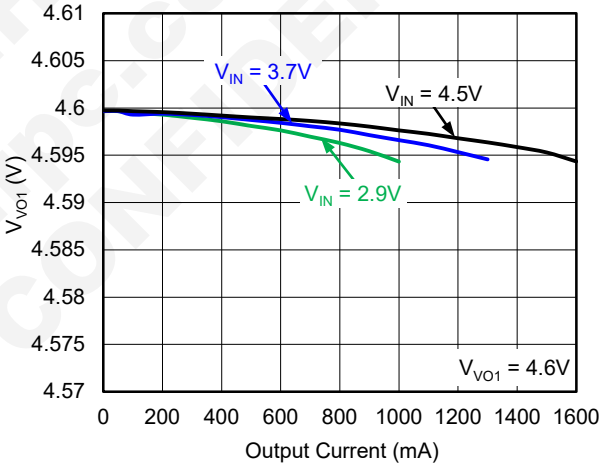
V_{VO3} Efficiency vs. Output Current



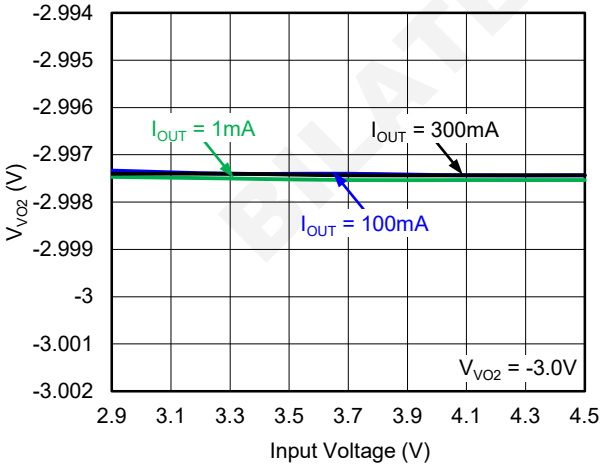
V_{VO1} Line Regulation



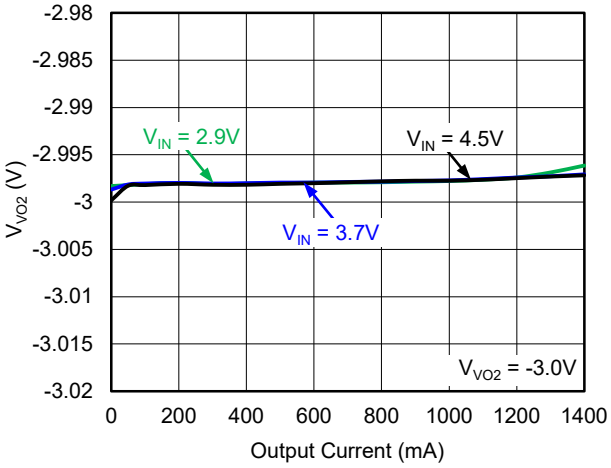
V_{VO1} Load Regulation



V_{VO2} Line Regulation



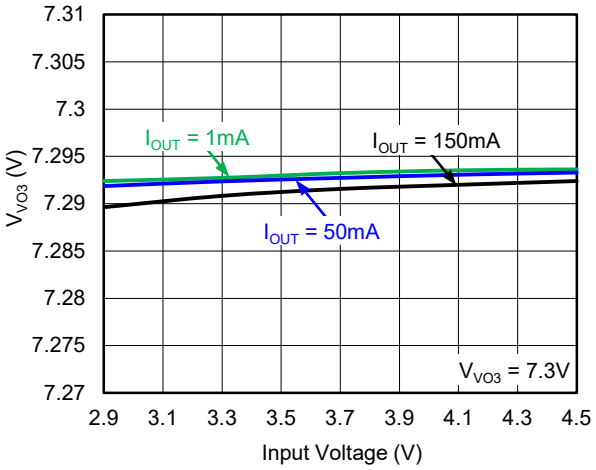
V_{VO2} Load Regulation



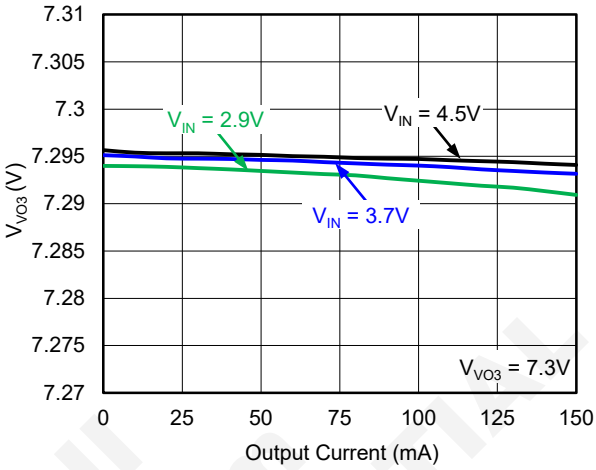
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = +25℃, V_{IN} = 3.7V, unless otherwise noted.

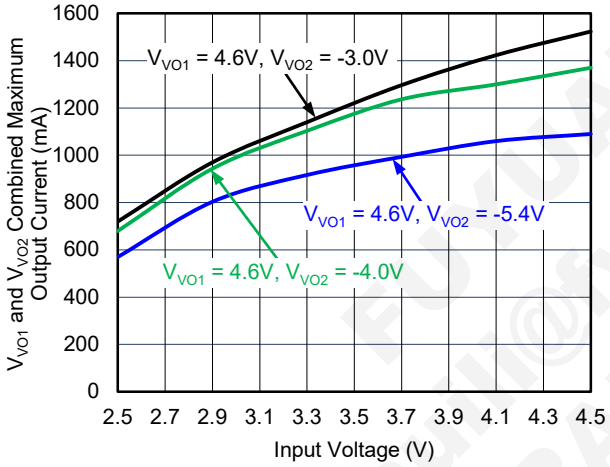
V_{VO3} Line Regulation



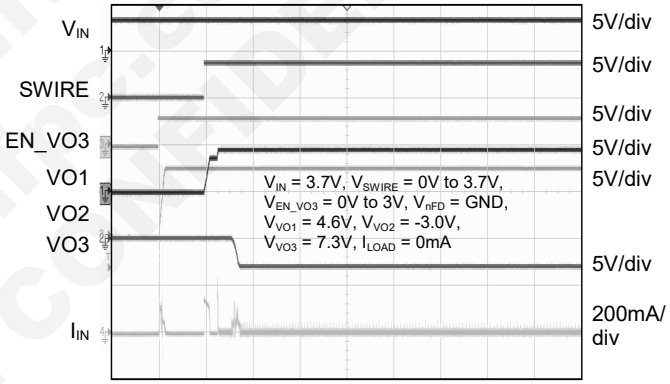
V_{VO3} Load Regulation



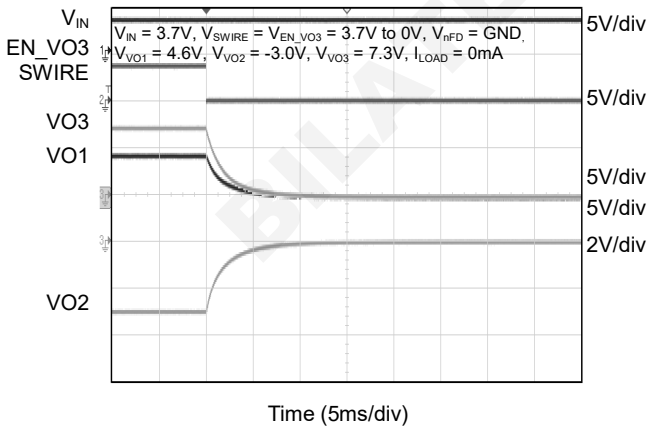
V_{VO1} and V_{VO2} Combined Maximum Output Current vs. Input Voltage



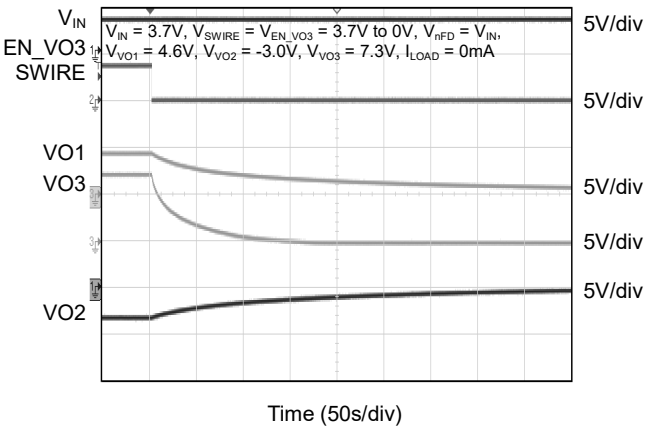
Startup Sequence



Shutdown Sequence Discharge = ON



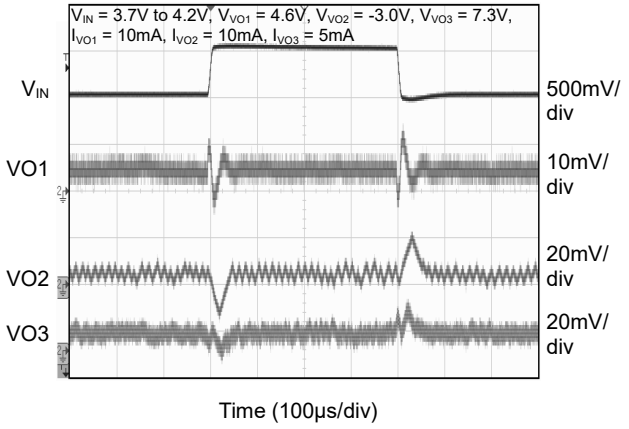
Shutdown Sequence Discharge = OFF



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

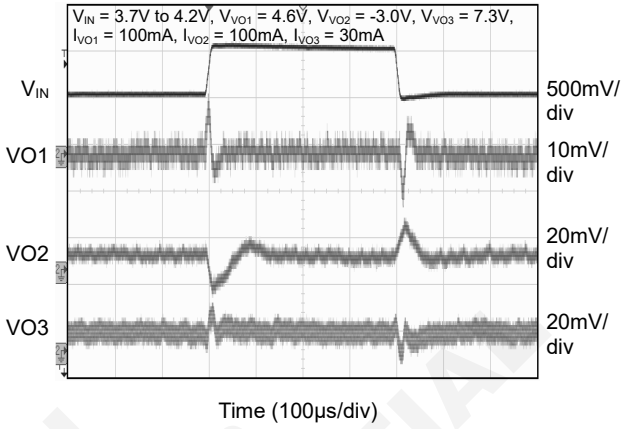
At T_J = +25℃, V_{IN} = 3.7V, unless otherwise noted.

Line Transient at Light Load



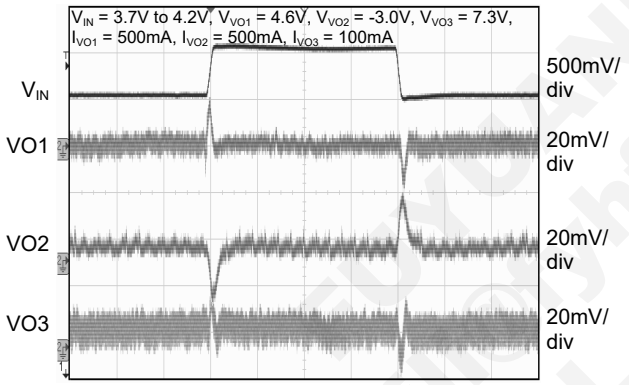
Time (100μs/div)

Line Transient at Moderate Load



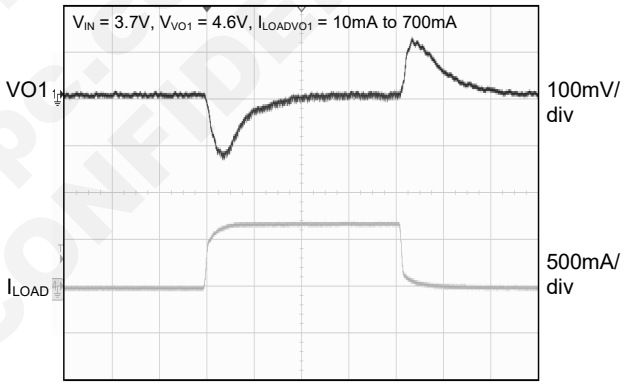
Time (100μs/div)

Line Transient at Heavy Load



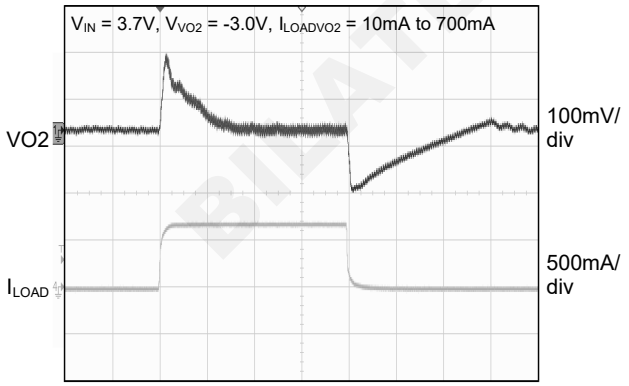
Time (100μs/div)

VO1 Load Transient



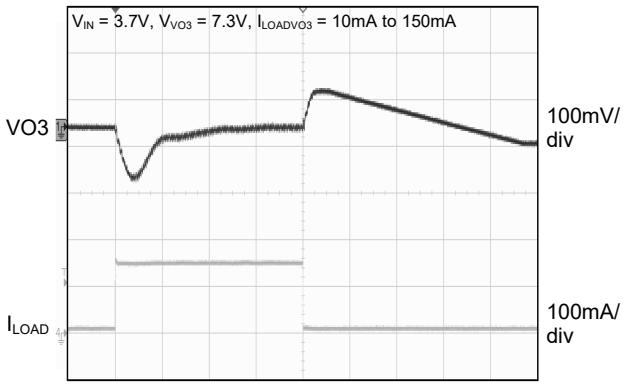
Time (20μs/div)

VO2 Load Transient



Time (50μs/div)

VO3 Load Transient



Time (20μs/div)

FUNCTIONAL BLOCK DIAGRAM

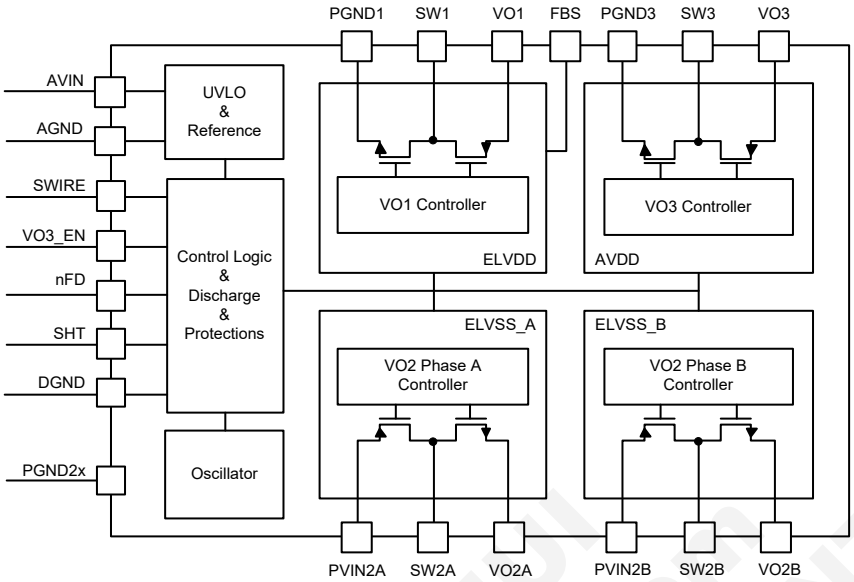


Figure 4. Functional Block Diagram

RECOMMENDED COMPONENT SELECTION

Table 1. Recommended component selection

Converter	Component	Value	Number	Electrical Spec	Part Number	Manufacturer
ELVDD	C_{IN1}	10μF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO1}	22μF	2	X5R, 6.3V, 0603	GRM188R60J226MEA0	Murata
	L_{VO1}	2.2μH	1	4A, 70mΩ, 322512	HMLQ32251B-2R2MS	Cyntec
ELVSS	C_{PVIN2A} C_{PVIN2B}	10μF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO2A} C_{VO2B}	22μF	1	X5R, 10V, 0603	GRM187R61A226ME15	Murata
	L_{VO2A} L_{VO2B}	2.2μH	1	4A, 70mΩ, 322512	HMLQ32251B-2R2MS	Cyntec
AVDD	C_{IN3}	10μF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO3}	10μF	2	X5R, 16V, 0603	GRM188R61C106KAAL	Murata
	L_{VO3}	10μH	1	1.3A, 390mΩ, 252012	SDEM25201B-100MS	Cyntec

DETAILED DESCRIPTION

Under-Voltage Lockout (UVLO)

The device has a built-in under-voltage lockout function which monitors the input voltage and disables the device when the input voltage is too low for operation.

Thermal Shutdown (TSD)

The device has a function of thermal shutdown to prevent damage from overheating and excessive power dissipation. The device shuts down the outputs once the junction temperature exceeds +145℃ (TYP), and restarts the outputs with the same voltages and sequences as programmed before when the temperature decreases to +135℃ (TYP).

VO1 Boost Converter (ELVDD)

The boost converter VO1 uses a valley-current-mode topology with fixed frequency. The output voltage V_{ELVDD} is adjustable between 4.6V and 5.0V (default 4.6V) with 100mV steps (see Table 2).

The output sense pin (FBS) is always connected to the positive pin of output capacitor for the highest output voltage accuracy. The wide hysteresis voltage makes the device suitable for large path loss applications. If not used, the FBS pin can be left floating or connected to ground, or connected to the VO1 pin, then the device senses the output voltage at the VO1 pin.

The output of VO1 is fully isolated (input to output and output to input) in shutdown mode.

VO2 Inverting Buck-Boost Converter (ELVSS)

The inverting buck-boost converter VO2 uses a peak-current-mode topology with dual-phase fixed frequency. The output voltage V_{ELVSS} is adjustable between -6.0V to -0.8V (default -3.0V) with 100mV steps (see Table 2).

When the load current exceeds 260mA, phase A and phase B of the inverting buck-boost converter both work. And only phase A works when the load current decreases to 150mA for reducing the switching loss.

The output of VO2 is fully isolated (input to output and output to input) in shutdown mode.

VO3 Boost Converter (AVDD)

The Boost converter VO3 uses a peak-current-mode topology with fixed frequency. The output voltage V_{AVDD} is adjustable between 5.5V and 7.9V (default 7.3V) with 100mV steps (see Table 2).

The output of VO3 is fully isolated (input to output and output to input) in shutdown mode.

Output Current Capacity

The device is designed to operate with input voltage range of 2.5V to 4.8V. However, due to different input voltage and different output voltage, the output current capacity is quite different. A lower input voltage or a higher output voltage leads to a lower output current capacity.

Input Power Supply

The input power supply voltage is recommended between 2.5V and 4.8V, and it should be stable and free of noise if the device's full performance is to be achieved. If the input supply is placed a few centimeters farther away from the device, additional bulk capacitance is required. The input capacitance shown in the typical application circuit is sufficient for typical applications.

Fault Protection Status (SHT)

The SHT is an interface to indicate a fault protection (SCP, UVLO) status. SHT is internally pulled up to AVIN through a 330kΩ resistor, and it will be pulled down to AGND when fault protection (SCP or UVLO) occurs.

DETAILED DESCRIPTION (continued)

Digital Interface (SWIRE Pin)

The positive output voltages V_{AVDD}, V_{ELVDD} and the negative output voltage V_{ELVSS} is allowed programming through the SWIRE digital interface in discrete steps.

Figure 2 shows an example for SGM3838 programming V_{ELVSS} to -2.4V. The SWIRE pin can be used as a standard enable pin if programming is not required.

The device starts with its default values (green marked values in Table 2) if enabled. The SWIRE interface counts the rising edges and sets the new values as shown in Table 2. The settings are stored in a volatile memory.

Table 2. Programming Table

Rising Edges	VO2 (V_{ELVSS})	Rising Edges	VO2 (V_{ELVSS})	Rising Edges	VO3 (V_{AVDD})	Rising Edges	Outputs Discharge	Rising Edges	VO2 transition time	Rising Edges	VO1 (V_{ELVDD})
0/no pulse	-3.0V	27	-3.4V	0/no pulse	7.3V	0/no pulse	controlled by nFD pin	0/no pulse	12ms	0/no pulse	4.6V
1	-6.0V	28	-3.3V	54	5.5V	79	ON	81	fast	83	4.6V
2	-5.9V	29	-3.2V	55	5.6V	80	OFF	82	12ms	84	4.7V
3	-5.8V	30	-3.1V	56	5.7V					85	4.8V
4	-5.7V	31	-3.0V	57	5.8V					86	4.9V
5	-5.6V	32	-2.9V	58	5.9V					87	5.0V
6	-5.5V	33	-2.8V	59	6.0V						
7	-5.4V	34	-2.7V	60	6.1V						
8	-5.3V	35	-2.6V	61	6.2V						
9	-5.2V	36	-2.5V	62	6.3V						
10	-5.1V	37	-2.4V	63	6.4V						
11	-5.0V	38	-2.3V	64	6.5V						
12	-4.9V	39	-2.2V	65	6.6V						
13	-4.8V	40	-2.1V	66	6.7V						
14	-4.7V	41	-2.0V	67	6.8V						
15	-4.6V	42	-1.9V	68	6.9V						
16	-4.5V	43	-1.8V	69	7.0V						
17	-4.4V	44	-1.7V	70	7.1V						
18	-4.3V	45	-1.6V	71	7.2V						
19	-4.2V	46	-1.5V	72	7.3V						
20	-4.1V	47	-1.4V	73	7.4V						
21	-4.0V	48	-1.3V	74	7.5V						
22	-3.9V	49	-1.2V	75	7.6V						
23	-3.8V	50	-1.1V	76	7.7V						
24	-3.7V	51	-1.0V	77	7.8V						
25	-3.6V	52	-0.9V	78	7.9V						
26	-3.5V	53	-0.8V								

DETAILED DESCRIPTION (continued)

Start-Up Sequence, Soft-Start and Shut-Down

The device has a soft-start function to limit the inrush current. The output discharge function is undefined when V_{IN} is applied until the output discharge is set to follow the nFD setting through the SWIRE interface.

When the converters are disabled, if nFD = low or high impedance if nFD = high, all outputs are discharged.

Pulling VO3_EN high starts the VO3 (AVDD) boost converter. V_{AVDD} follows a linear 1.5ms long voltage ramp until it reaches the default value (7.3V), then the switch current is limited to typical 0.35A.

Pulling SWIRE high starts the VO1 (ELVDD) boost converter. V_{ELVDD} starts with a reduced switch current limit of 0.2A until it reaches the default voltage (4.6V), then the full current limit is released.

5ms after SWIRE is pulled high the VO2 (ELVSS) inverting buck-boost converter starts. V_{ELVSS} starts with a reduced switch current limit of 0.7A until it reaches the default voltage (-3V), then the full current limit is released.

Short Circuit and Overload Protection

The device is protected from damage of V_{AVDD}, V_{ELVDD} and V_{ELVSS} shorting to ground. The device is also protected when V_{ELVDD} and V_{ELVSS} are shorted together.

A short at any converter or the V_{AVDD} overload protection can shut down the whole device, then the shutdown state is latched, and the input is fully disconnected with all outputs.

In order to reset the whole device, V_{IN} has to cycle below UVLO or VO3_EN and SWIRE have to be low at the same time for minimum t_{OFF}.

The device detects a short or an overload when one of the below conditions is fulfilled:

- V_{ELVDD} is not in regulation 1.6ms after V_{ELVDD} is enabled (SWIRE = high for longer than 1.6ms) then all converters shut down.
- V_{ELVSS} is not in regulation 5ms after V_{ELVSS} is enabled (SWIRE = high for longer than 10ms) then all converters shut down.
- V_{AVDD} protection is enabled when the soft-start is completed.
- V_{ELVDD} falls below 81% of the programmed output voltage longer than 0.6ms then all converters shut down.
- V_{ELVSS} rises above 82% of the programmed output voltage longer than 0.6ms then all converters shut down.
- V_{AVDD} falls below 88% of the programmed output voltage longer than 0.6ms then all converters shut down.

Device Reset

- A power cycle resets all settings to default values.
- Short-circuit and overload protection reset all settings.
- Pulling SWIRE high to enable the V_{ELVDD} converter resets the output discharge then output discharge is controlled by nFD pin.
- Pulling SWIRE low for t_{OFF} then V_{ELVDD}, V_{ELVSS} and V_{AVDD} is reset to default values of 4.6V, -3.0V and 7.3V.
- Pulling SWIRE low for t_{OFF} then V_{ELVSS} transition time is reset to default value of 12ms.
- Pulling VO3_EN and SWIRE low at the same time for t_{OFF} then Short circuit protection is reset.

Layout Guideline

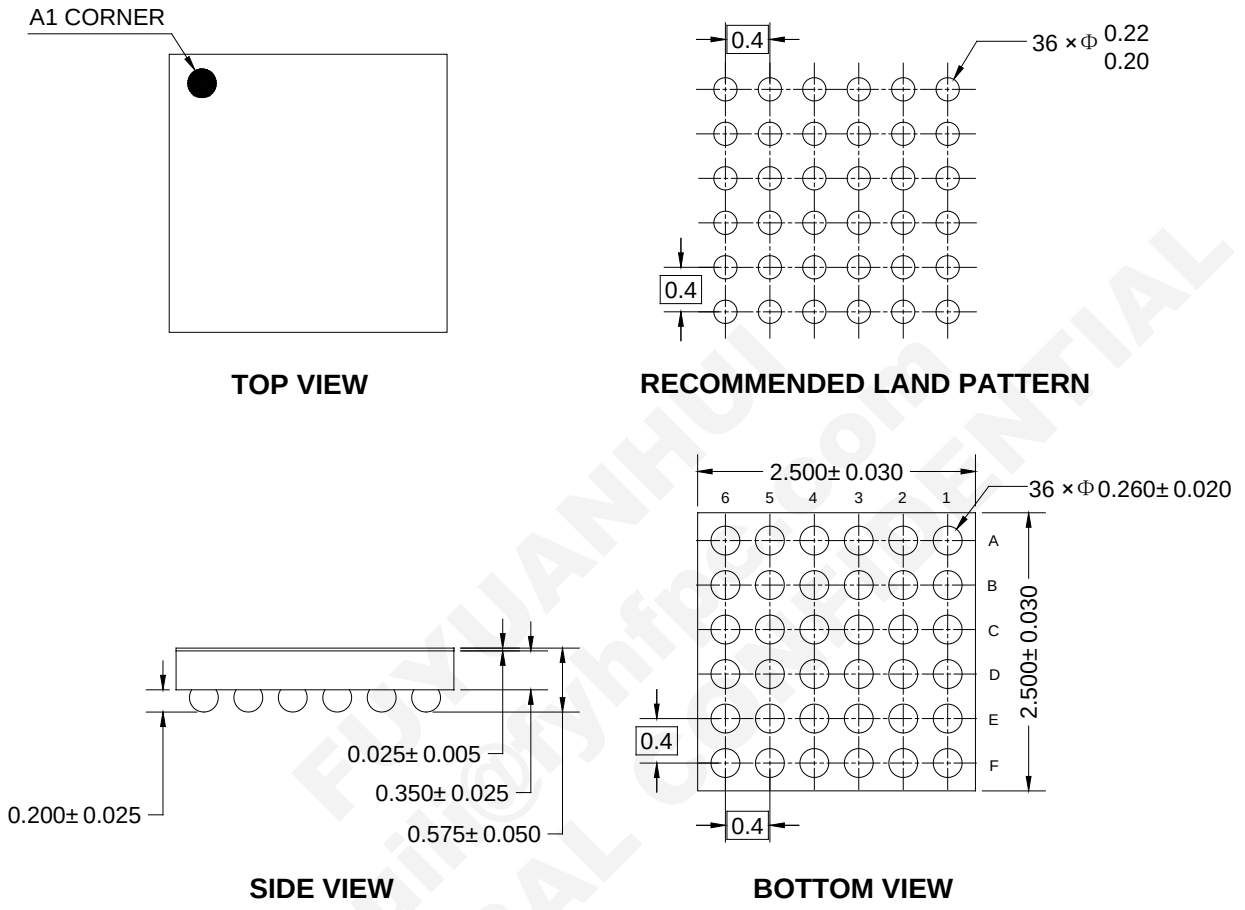
The PCB layout is quite important in the power supply design. An incorrect layout could cause many problems, such as instability, load and line transient regulation problems, output voltage noise, and EMI issues. Good grounding becomes important especially with heavy load current.

The following PCB layout guide should be applied:

• A common ground plane between analog ground (GND) and power ground (PGND) for minimize ground shifts is recommended.
• Traces of switching nodes (SW1, SW2A, SW2B and SW3) should be short and wide.
• Place input capacitors on PVIN (PVIN2A and PVIN2B) and output capacitors on VO2 (VO2A and VO2B) as close as possible to the device.
• Use short and wide traces to connect the input capacitors on PVIN and the output capacitors on VO2.
• Place the output capacitors on VO1 and VO3 as close as possible to the device.
• Connect AGND, DGND and PGNDx with the exposed thermal pad.

PACKAGE OUTLINE DIMENSIONS

WLCSP-2.5×2.5-36B



TOP VIEW

RECOMMENDED LAND PATTERN

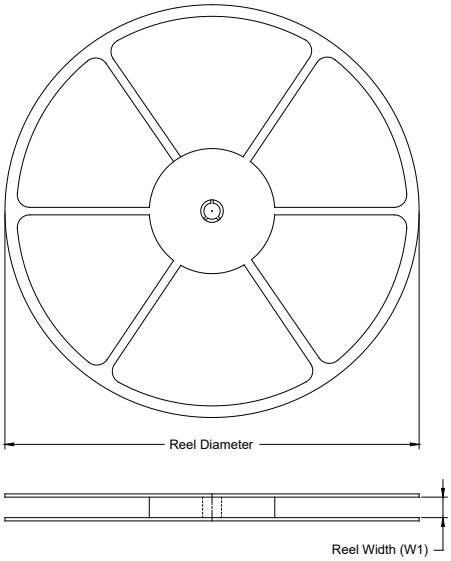
SIDE VIEW

BOTTOM VIEW

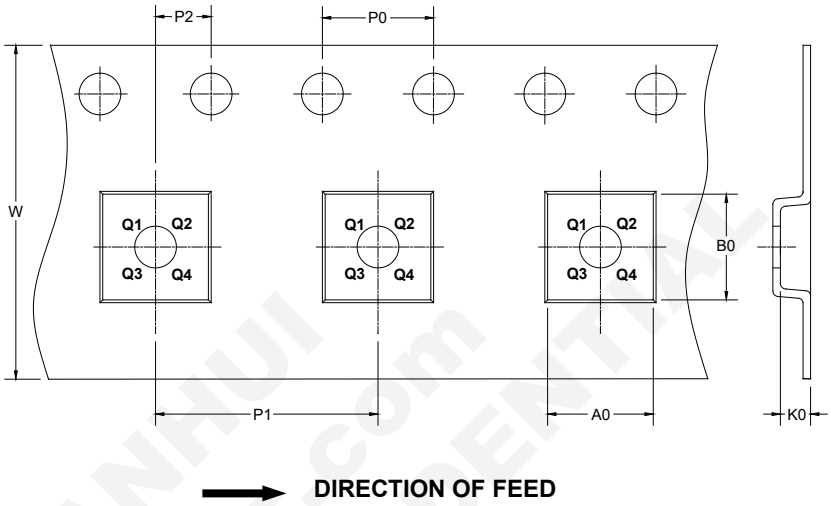
NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

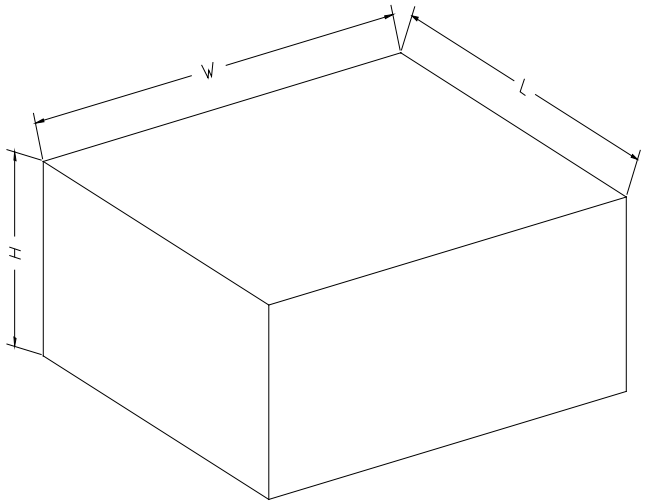
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.5×2.5-36B	13″	12.4	2.66	2.69	0.77	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002