SGM8910
4Vrms High Performance Audio Line and Headset Driver with Click-Pop Noise Cancelling

GENERAL DESCRIPTION

The SGM8910 is a high performance 4Vrms stereo audio line driver with click-pop noise cancelling in the applications where single power supply, PCB size and no click-pop noise are critical, it reduces external component count and board space. SGM8910 can drive 32Ω impedance headset directly, so it can be used as the high performance driver of line out and headset in different applications.

SGM8910 integrates a charge pump and negative low drop output voltage regulator to generate a low noise negative supply rail that supports it to provide a clean, pop-free and ground-biased output. The SGM8910 is capable of driving 4Vrms into a 600Ω load when V_{DD} is 10V or 10mW into 32Ω headset when V_{DD} is 3.3V. Capless output structure allows the removal of the costly output DC-blocking capacitors. For some special applications where AC coupling output is necessary, SGM8910 provides MUTEOUT driver to drive external click-pop noise cancelling circuit during power on and power off.

SGM8910 will be in mute status during power-on blanking time, external mute control signal can take over the mute status before power-on blanking time is over, SGM8910 can cancel power up click-pop noise perfectly. Using under-voltage protection (UVP), SGM8910 will cancel the turn off click-pop noise perfectly.

The SGM8910 is available in Green TSSOP-20 and TQFN-4×4-20L packages. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Capless Structure to Eliminate Pop-Clicks and Output DC-Blocking Capacitors**
- **2.8V to 12V Supply Voltage**
- **Low Noise, Low THD and Low Crosstalk:**
  Typical V_n < 6.5μV_{RMS} from 20Hz to 20kHz at Gain = -1
  THD+N < 0.002% for 10kΩ Load and Gain = -1 at 1kHz
  Crosstalk is -89dB at 1kHz
- **4Vrms Output Voltage into 600Ω Load for 10V V_{DD}**
- **1Vrms Output Voltage into 600Ω Load for 3.3V V_{DD}**
- **Supports to Drive 32Ω to 600 Ω Headset:**
  10mW for 32Ω Headset at V_{DD} = 3.3V
- **Single-Ended Output**
- **Differential or Single-Ended Input**
- **UVP Function to Cancel Turn Off Click-Pop Noise**
- **Adjustable Power-On Blanking Time to Eliminate Turn on Click-Pop Noise**
- **Short-Circuit and Thermal Protection for Audio Driver**
- **Negative LDO has Output Auto-Discharge Function in Disable Status**
- **1.8V Logical Control for EN and $\overline{\text{MUTE}}$**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in the Green TSSOP-20 and TQFN-4×4-20L Packages**

APPLICATIONS

PDP/LCD TV
DVD Players
Mini/Micro Combo Systems
Soundcards

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8910	TSSOP-20	-40℃ to +85℃	SGM8910YTS20G/TR	SGM8910YTS20 XXXXX	Tape and Reel 4000
	TQFN-4×4-20L	-40℃ to +85℃	SGM8910YTQI20G/TR	SGM8910 YTQI20 XXXXX	Tape and Reel 3000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range ..... -0.3V to 13.2V
Input Voltage Range ..... V_{SS} - 0.3V to V_{DD} + 0.3V
$\overline{MUTE}$, EN to GND ..... -0.3V to 5V + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.8V to 12V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

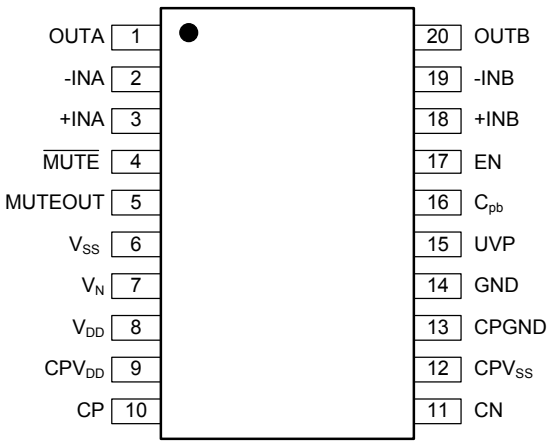
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

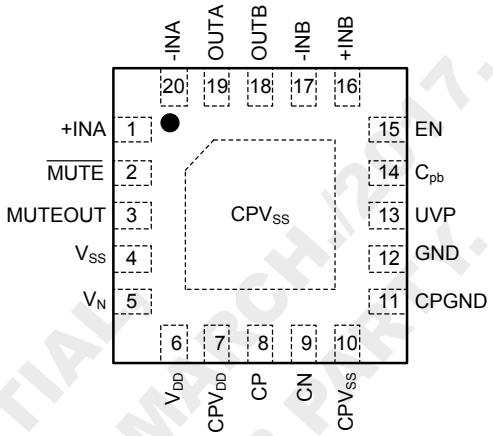
PIN CONFIGURATIONS

(TOP VIEW)



TSSOP-20

(TOP VIEW)



TQFN-4×4-20L

PIN DESCRIPTION

PIN		NAME	FUNCTION
TSSOP-20	TQFN-4×4-20L		
1	19	OUTA	Output of driver A.
2	20	-INA	Negative polarity input of driver A.
3	1	+INA	Positive polarity input of driver A.
4	2	$\overline{MUTE}$	Mute control input, active low. When $\overline{MUTE}$ = "Low", chip enters into mute status; when $\overline{MUTE}$ = "High", chip works normally. There is a 5MΩ pull-low resistor at $\overline{MUTE}$ pin.
5	3	MUTEOUT	Open drain output of mute. When SGM8910 is in mute status, MUTEOUT will be in high-impedance state; when SGM8910 is not in mute status, MUTEOUT will be in low logical output to drive external mute circuit.
6	4	V_{SS}	Negative power supply of drivers.
7	5	V_N	Output of negative low drop output regulator.
8	6	V_{DD}	Positive supply voltage of drivers. When V_{DD} under-voltage event happens, chip will enter into mute status.
9	7	CPV_{DD}	Power supply of negative charge pump DC/DC.
10	8	CP	Charge pump flying capacitor positive connection.
11	9	CN	Charge pump flying capacitor negative connection.
12	10	CPV_{SS}	Output of negative charge pump DC/DC.
13	11	CPGND	Ground of charge pump DC/DC.
14	12	GND	Ground.
15	13	UVP	Under-voltage protection input. When UVP event happens, chip will be in mute status.
16	14	C_{pb}	Power-on blanking time adjusting, connect a capacitor from C_{pb} pin to GND to program the power-on blanking time. Chip is in mute status during power-on blanking time.
17	15	EN	Enable control input of chip. EN = "High" to enable chip, SGM8910 is in active status; EN = "Low" to disable chip, SGM8910 is in shutdown status.
18	16	+INB	Positive polarity input of driver B.
19	17	-INB	Negative polarity input of driver B.
20	18	OUTB	Output of driver B.
–	Thermal Pad	CPV_{SS}	Output of negative charge pump DC/DC.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage (V_{DD})		2.8		12	V
R_L		32			Ω
$\overline{MUTE}$, EN Low-Level Input Voltage (V_{IL})				0.4	V
$\overline{MUTE}$, EN High-Level Input Voltage (V_{IH})		1.8			V
ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V, R_{LOAD} = 5kΩ, C_{FLY} = 1μF)					
Output Offset Voltage ($\|V_{OS}\|$)	V_{DD} = 3.3V, input AC-coupled		100		μV
Power Supply Rejection Ratio (PSRR)			0.1		μV/V
High-Level Output Voltage (V_{OH})	V_{DD} = 3.3V		3.2		V
Low-Level Output Voltage (V_{OL})	V_{DD} = 3.3V		-1.6		V
External Under-Voltage Detection (V_{UVP})			1.2		V
Charge Pump Switching Frequency (f_{CP})			580		kHz
High-Level Input Current, $\overline{MUTE}$ ($\|I_{IH}\|$)	V_{DD} = 3.3V, V_{IH} = V_{DD}		700		nA
Low-Level Input Current, $\overline{MUTE}$ ($\|I_{IL}\|$)	V_{DD} = 3.3V, V_{IL} = 0V		1		nA
Supply Current (I_{VDD})	V_{DD} = 3.3V, $\overline{MUTE}$ = 3.3V, no load		16.2		mA
Thermal Shutdown (t_{SD})			155		℃
Thermal Shutdown Hysteresis			20		℃
OPERATING CHARACTERISTICS (V_{DD} = 3.3V, R_{LOAD} = 10kΩ, C_{FLY} = 1μF, -1 × Gain select)					
Output Voltage, Outputs in Phase (V_O)	1% THD+N, f = 1kHz, 10kΩ load		1.2		Vrms
Total Harmonic Distortion Plus Noise (THD+N)	f = 1kHz, BW = 20Hz to 20kHz, 10kΩ load, V_O = 1Vrms		0.0009		%
Output Power to 32Ω Headset	f = 1kHz, 32Ω load, V_{DD} = 3.3V, THD+N = 0.008%		10		mW
Signal-to-Noise Ratio (SNR)	f = 1kHz, BW = 20Hz to 20kHz, 10kΩ load, V_O = 1Vrms		104		dB
	f = 1kHz, BW = 20Hz to 20kHz, 32Ω load, P_O = 10mW		98		
Dynamic Range (DNR)	A-weighted, AES17 filter, 1Vrms ref		120		dB
Noise Voltage (V_n)	A-weighted, AES17 filter, 1Vrms ref, BW = 20Hz to 20kHz		6.5		$μV_{RMS}$
Output Impedance when Muted (Z_O)			150		Ω
Input-to-Output Attenuation when Muted	$\overline{MUTE}$ = GND		45		dB
Slew Rate	1Vrms, 1kHz input		16		V/μs
Crosstalk-Line L-R and R-L	f = 1kHz, 10kΩ load, V_O = 1Vrms		-120		dB
	f = 1kHz, 32Ω load, V_O = 10mW		-89		
Current Limit (I_{LIM})	V_{DD} = 3.3V		60		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, R_{LOAD} = 5kΩ, C_{FLY} = 1μF)					
Output Offset Voltage ($\|V_{OS}\|$)	V_{DD} = 5V, input AC-coupled		100		μV
Power Supply Rejection Ratio (PSRR)			0.1		μV/V
High-Level Output Voltage (V_{OH})	V_{DD} = 5V		4.9		V
Low-Level Output Voltage (V_{OL})	V_{DD} = 5V		-3.3		V
Charge Pump Switching Frequency (f_{CP})			580		kHz
High-Level Input Current, $\overline{MUTE}$ ($\|I_{IH}\|$)	V_{DD} = 5V, V_{IH} = V_{DD}		1000		nA
Low-Level Input Current, $\overline{MUTE}$ ($\|I_{IL}\|$)	V_{DD} = 5V, V_{IL} = 0V		1		nA
Supply Current (I_{VDD})	V_{DD} = 5V, $\overline{MUTE}$ = 5V, no load		16.8		mA
Thermal Shutdown (t_{SD})			155		℃
Thermal Shutdown Hysteresis			20		℃
OPERATING CHARACTERISTICS (V_{DD} = 5V, R_{LOAD} = 10kΩ, C_{FLY} = 1μF, -1 × Gain select)					
Output Voltage, Outputs in Phase (V_O)	1% THD+N, f = 1kHz, 10kΩ load		2.5		Vrms
Total Harmonic Distortion Plus Noise (THD+N)	f = 1kHz, BW = 20Hz to 20kHz, 10kΩ load, V_O = 2Vrms		0.0006		%
Output Power to 32Ω Headset	f = 1kHz, 32Ω load, V_{DD} = 5V, THD+N = 0.008%		20		mW
Signal-to-Noise Ratio (SNR)	f = 1kHz, BW = 20Hz to 20kHz, 10kΩ load, V_O = 2Vrms		110		dB
	f = 1kHz, BW = 20Hz to 20kHz, 32Ω load, P_O = 20mW		102		
Dynamic Range (DNR)	A-weighted, AES17 filter, 2Vrms ref		120		dB
Noise Voltage (V_n)	A-weighted, AES17 filter, 2Vrms ref, BW = 20Hz to 20kHz		6.5		$μV_{RMS}$
Output Impedance when Muted (Z_O)			150		Ω
Input-to-Output Attenuation when Muted	$\overline{MUTE}$ = GND		45		dB
Slew Rate	1Vrms, 1kHz input		12		V/μs
Crosstalk-Line L-R and R-L	f = 1kHz, 10kΩ load, V_O = 2Vrms		-120		dB
	f = 1kHz, 32Ω load, P_O = 20mW		-89		
Current Limit (I_{LIM})	V_{DD} = 5V		70		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 12V, T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ELECTRICAL CHARACTERISTICS (V_{DD} = 12V, R_{LOAD} = 5kΩ, C_{FLY} = 1μF)					
Output Offset Voltage ($\|V_{OS}\|$)	V_{DD} = 12V, input AC-coupled		100		μV
Power Supply Rejection Ratio (PSRR)			0.1		μV/V
High-Level Output Voltage (V_{OH})	V_{DD} = 12V		11.9		V
Low-Level Output Voltage (V_{OL})	V_{DD} = 12V		-10.3		V
Charge Pump Switching Frequency (f_{CP})			580		kHz
Supply Current (I_{VDD})	V_{DD} = 12V, $\overline{MUTE}$ = 5V, no load		17.6		mA
Thermal Shutdown (t_{SD})			155		℃
Thermal Shutdown Hysteresis			20		℃
OPERATING CHARACTERISTICS (V_{DD} = 12V, R_{LOAD} = 10kΩ, C_{FLY} = 1μF, -1 × Gain select)					
Output Voltage, Outputs in Phase (V_O)	1% THD+N, f = 1kHz, 10kΩ load		7.5		Vrms
Total Harmonic Distortion Plus Noise (THD+N)	f = 1kHz, BW = 20Hz to 20kHz, 10kΩ load, V_O = 4Vrms		0.002		%
Output Power to 32Ω Headset	f = 1kHz, 32Ω load, V_{DD} = 12V, THD+N = 0.005%		30		mW
Signal-to-Noise Ratio (SNR)	f = 1kHz, BW = 20Hz to 20kHz, 10kΩ load, V_O = 4Vrms		115		dB
	f = 1kHz, BW = 20Hz to 20kHz, 32Ω load, P_O = 30mW		103		
Noise Voltage (V_n)	A-weighted, AES17 filter, 2Vrms ref, BW = 20Hz to 20kHz		6.5		$μV_{RMS}$
Output Impedance when Muted (Z_O)			150		Ω
Input-to-Output Attenuation when Muted	$\overline{MUTE}$ = GND		34		dB
Slew Rate	1Vrms, 1kHz input, 10kΩ load		17		V/μs
	1Vrms, 1kHz input, 32Ω load		10		
Crosstalk-Line L-R and R-L	f = 1kHz, 10kΩ load, V_O = 2Vrms		-131		dB
	f = 1kHz, 32Ω load, P_O = 20mW		-89		

TYPICAL APPLICATION

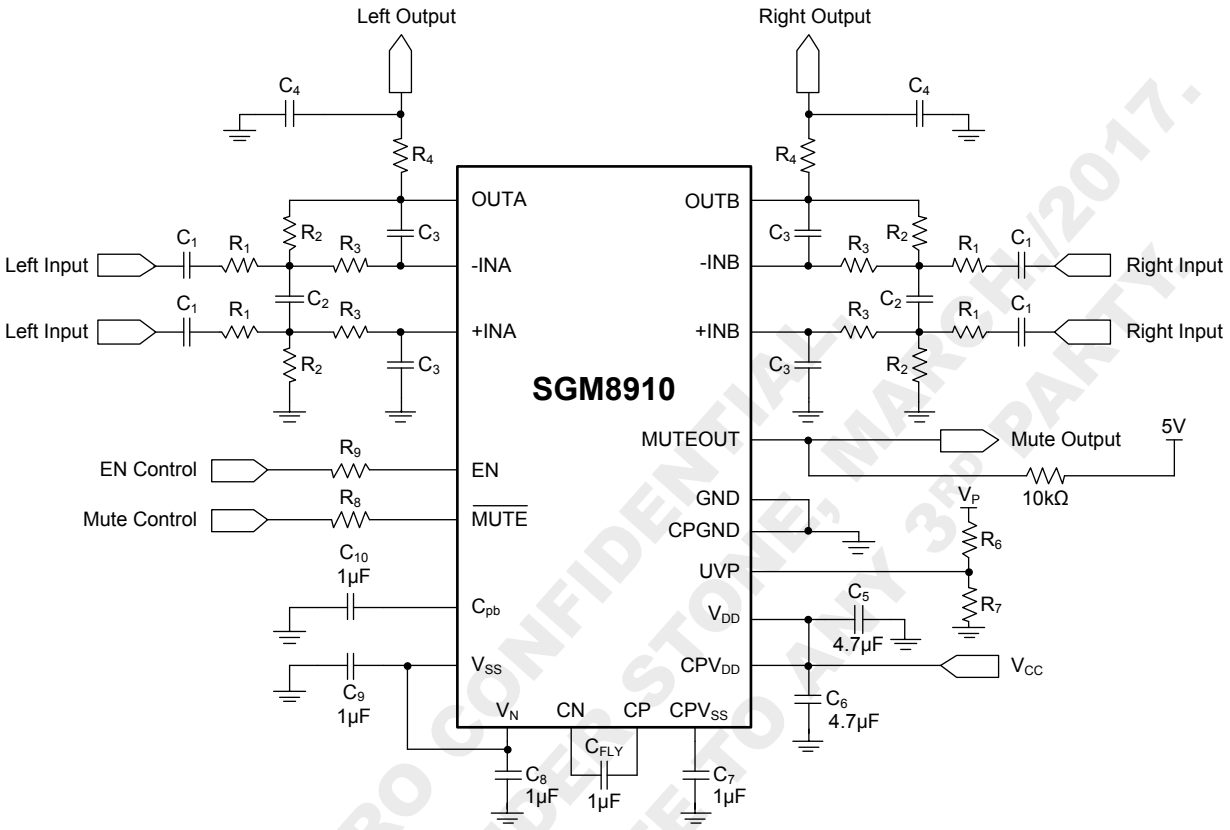


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

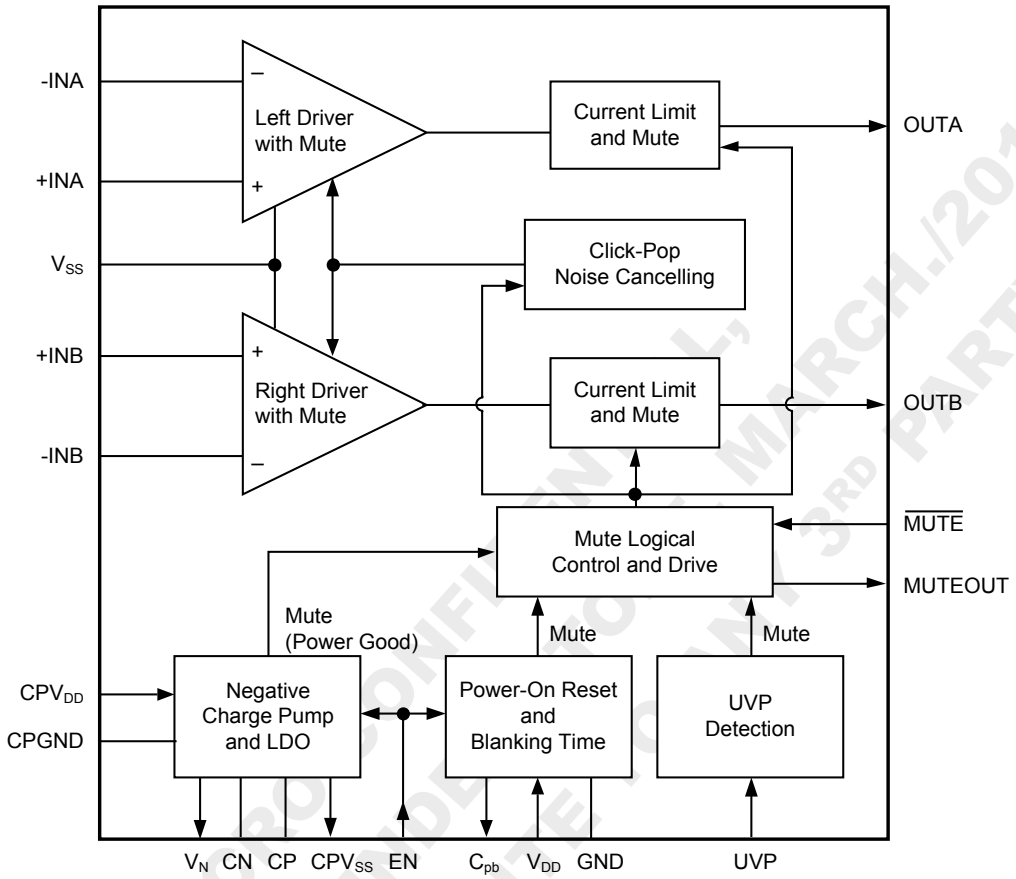


Figure 2. Block Diagram

APPLICATION INFORMATION

Line Driver Amplifiers

Single power supply line-driver amplifiers typically require DC-blocking capacitors. The top drawing in Figure 3 illustrates the conventional line-driver amplifier connection to the load and output signal.

DC-blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click and pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

The capless amplifier architecture operates from a single supply but makes use of an internal negative charge pump to provide a negative voltage rail. Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click- and pop-reduction circuit, the capless amplifier requires no output DC-blocking capacitors. The bottom block diagram and waveform of Figure 3 illustrate the ground-referenced line-driver architecture. This is the architecture of the SGM8910.

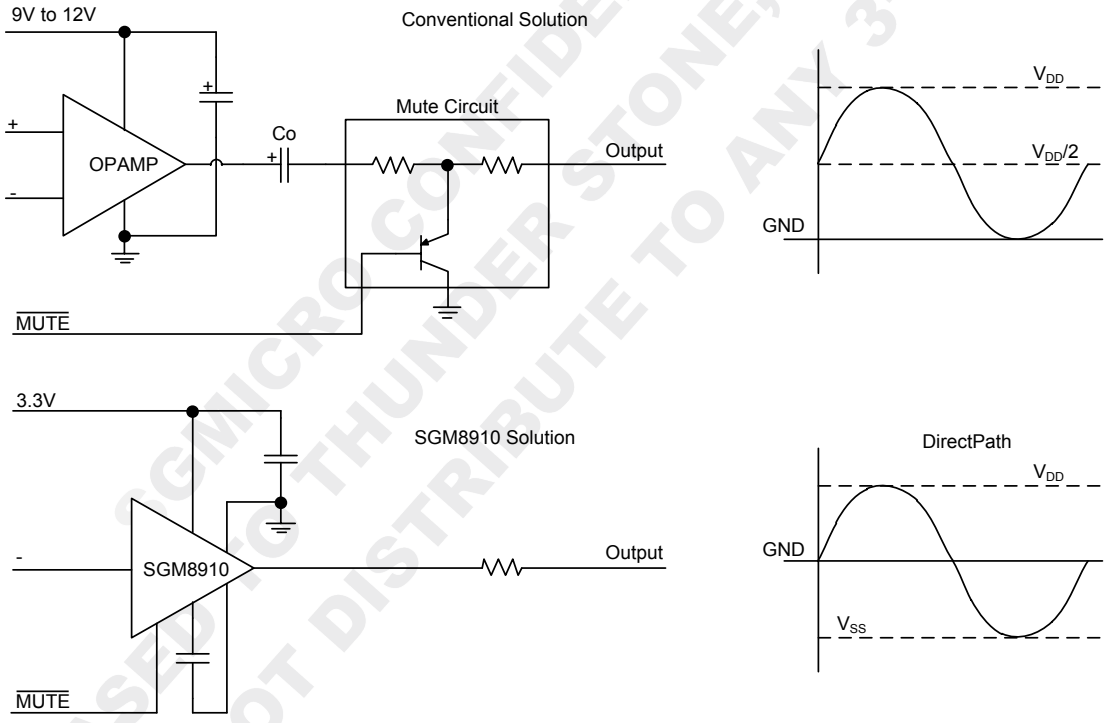


Figure 3. Conventional and Capless Line Driver

APPLICATION INFORMATION (continued)

Charge Pump Flying Capacitor and CPV_{SS} Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The CPV_{SS} capacitor must be at least equal to the charge pump capacitor C_{FLY} in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and the typical value is 1μF.

Decoupling Capacitors

The SGM8910 is a capless line-driver amplifier that requires adequate power-supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. Dual good low equivalent-series-resistance (ESR) ceramic capacitors, typically 4.7μF, placed as close as possible to the device V_{DD} and CPV_{DD} leads work best. Placing these decoupling capacitors close to the SGM8910 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier also helps, but it is not required in most applications because of the high PSRR of this device.

Internal Under-Voltage Detection

In Figure 4, the SGM8910 contains an internal precision band-gap reference voltage and a comparator used to monitor the V_{DD} power supply voltage. The internal V_{DD} monitor is set at 2.6V with 150mV hysteresis. When UV event happens on V_{DD}, SGM8910 will enter into mute status at once.

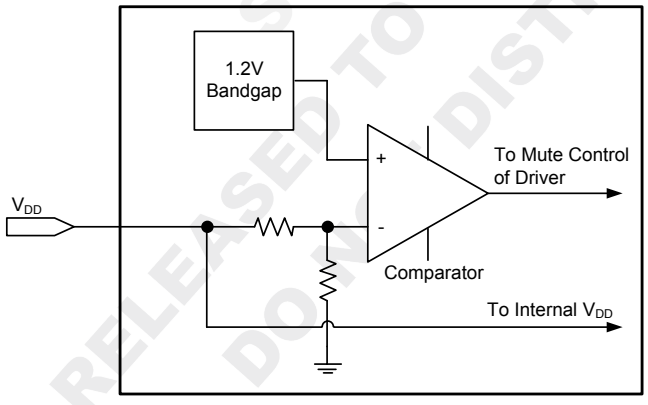


Figure 4. V_{DD} UV Event Detection

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the SGM8910. These capacitors block the DC portion of the audio source and allow the SGM8910 inputs to be properly biased to provide maximum performance.

The input-blocking capacitor forms a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1. The frequency and/or capacitance can be determined when one of the two values is given:

$$f_{C_{IN}} = \frac{1}{2\pi R_{IN} C_{IN}} \text{ or } C_{IN} = \frac{1}{2\pi f_{C_{IN}} R_{IN}} \quad (1)$$

Pop-Free Power Up

In Figure 5, pop-free power up is ensured by keeping the $\overline{MUTE}$ pin low before power-on blanking time is over. The chip should be kept in mute status until the input AC-coupling capacitors are fully charged, this way proper pre-charge of the AC-coupling is performed and pop-free power up is achieved. Figure 5 illustrates the internal circuit and preferred power up sequence.

The power-on blanking time is adjustable. Adjust this time (t_{pb}) by connecting a capacitor (C_{pb}) between C_{pb} pin and ground. Calculate the external capacitor as follows:

$$C_{pb} = (t_{pb})/(4 \times 10^6) \quad (2)$$

where t_{pb} is in seconds and C_{pb} is in farads.

Capacitive Load

The SGM8910 has the ability to drive a high capacitive load up to 220pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47Ω or larger for the line driver output.

MUTEOUT Driver

MUTEOUT is the indication signal that informs audio processing processor what audio driver's status is. MUTEOUT also can be used to drive external mute circuit to get better click-pop noise cancelling performance in some special applications.

APPLICATION INFORMATION (continued)

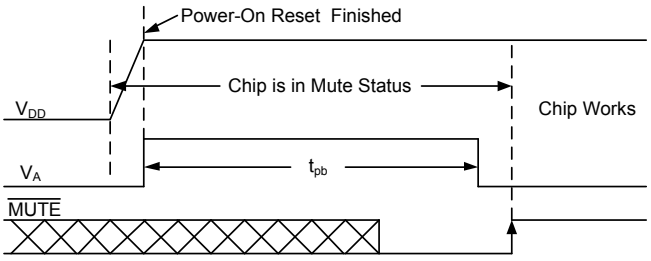


Figure 5. Power up Sequence

External Under-Voltage Detection

In Figure 6, external under-voltage detection can be used to mute the SGM8910 and cancel the click-pop noise generated during power off.

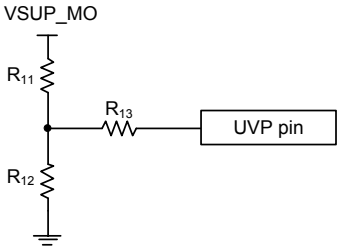


Figure 6. External UVP Circuit

The threshold seen at the UVP pin is 1.2V. A hysteresis is introduced with a resistive divider, where thresholds for startup and shutdown are determined respectively as follows:

Startup Threshold: $V_{UDPR} = 1.2V \times (R_{11} + R_{12})/R_{12}$
Shutdown Threshold: $V_{UDPF} = 1.2V \times (R_{11}+R_{12})/R_{12} - 4.6\mu A \times (R_{13} + R_{11} \,||\, R_{12}) \times (R_{11} + R_{12})/R_{12}$
Hysteresis: $4.6\mu A \times (R_{13} + R_{11} \,||\, R_{12}) \times (R_{11} + R_{12})/R_{12}$

The R_{13} is optional, if the R_{13} is not used, the UVP pin is connected to the resistor divider center tap directly.

EN and $\overline{\text{MUTE}}$ Control

EN and $\overline{\text{MUTE}}$ control are independent. When EN = "Low", chips enters into low power status, negative charge pump, negative LDO and audio driver are disabled, C_{pb} and negative LDO output are in auto-discharge status. When EN = "High", chip enters into power on stage, negative charge pump, negative LDO and audio driver will work, but audio driver output stage is controlled by internal mute signal.

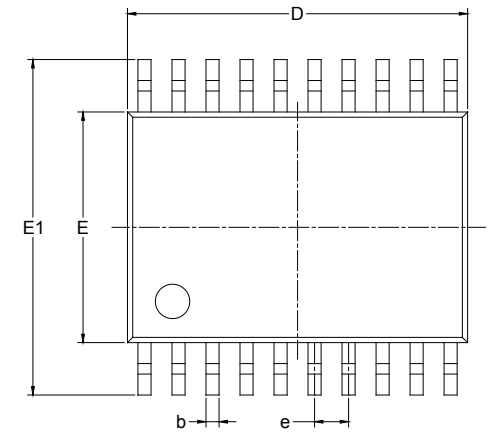
External $\overline{\text{MUTE}}$, power-on blanking time, power-on reset, V_{DD} UV, external UVP signals will be combined as the inputs signal of internal mute logical circuit, it generates mute signal to mute or enable the output stage of audio driver.

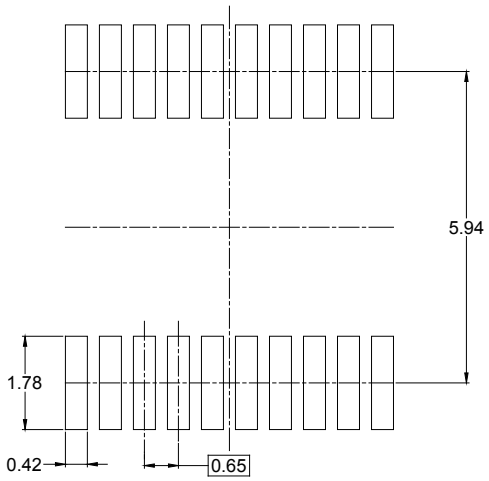
Layout Recommendations

Ground traces are recommended to be routed as a star ground to minimize hum interference. V_{DD}, CPV_{DD}, CPV_{SS}, V_N, V_{SS} decoupling capacitors and the charge pump capacitor C_{FLY} should be connected with short traces.

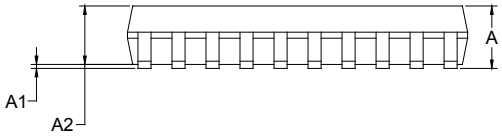
PACKAGE OUTLINE DIMENSIONS

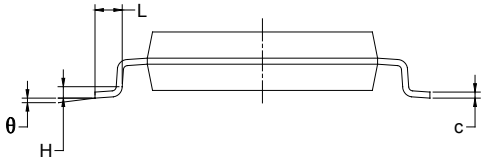
TSSOP-20





RECOMMENDED LAND PATTERN (Unit: mm)

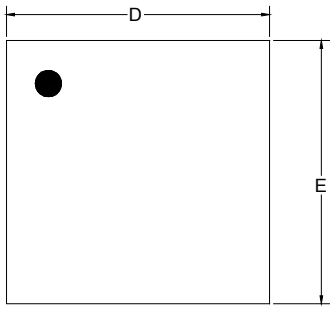




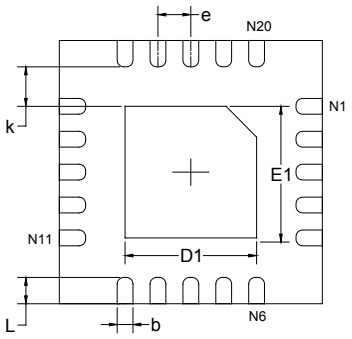
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

PACKAGE OUTLINE DIMENSIONS

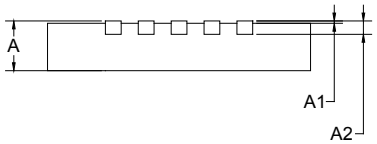
TQFN-4×4-20L



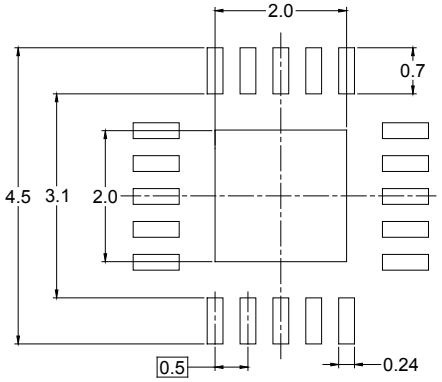
TOP VIEW



BOTTOM VIEW



SIDE VIEW

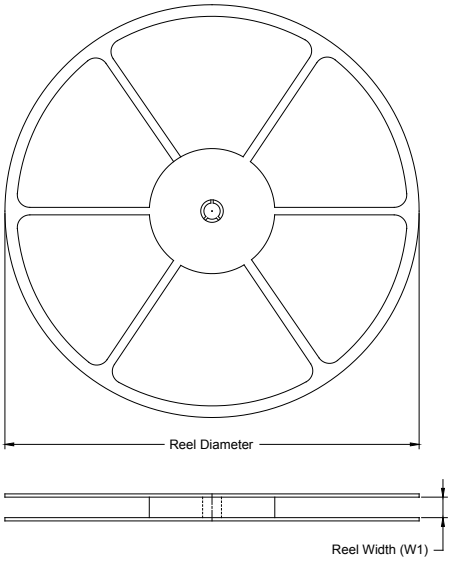


RECOMMENDED LAND PATTERN (Unit: mm)

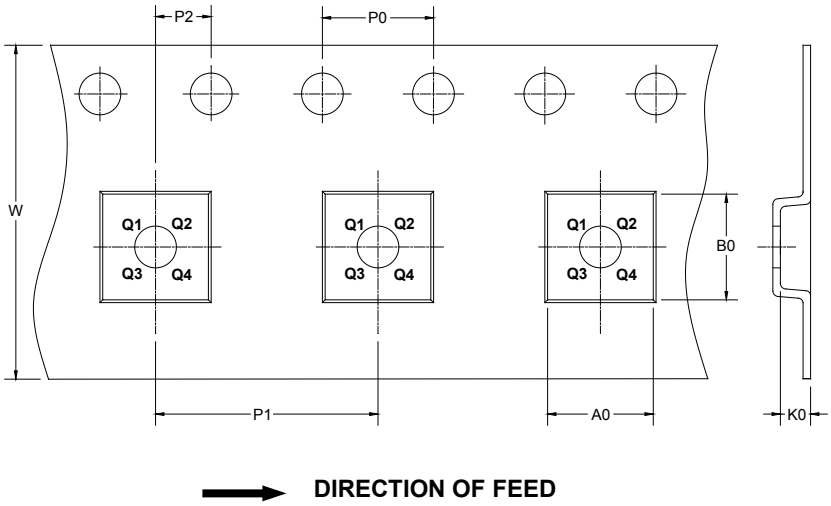
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
D1	1.900	2.100	0.075	0.083
E	3.900	4.100	0.154	0.161
E1	1.900	2.100	0.075	0.083
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



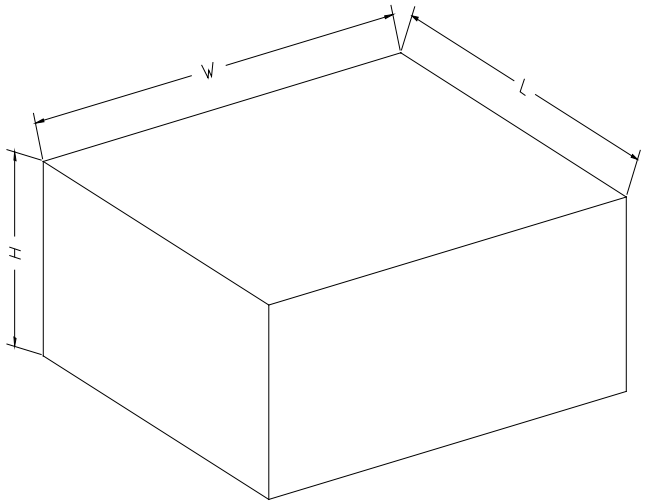
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-20	13″	12.4	6.80	6.85	1.70	4.0	8.0	2.0	12.0	Q1
TQFN-4×4-20L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002