SGM89111
Capless 3Vrms Line Driver with 8MHz 5th-Order Video Driver

GENERAL DESCRIPTION

The SGM89111 is a 3Vrms pop/click-free stereo line driver designed to allow the removal of the output DC-blocking capacitors for reduced component count and cost. The SGM89111 also has a single rail-to-rail 5th-order video filter with a -3dB bandwidth of 8MHz and a slew rate of 35V/µs. It operates from 3.0V to 5.5V power supply. The device is ideal for single supply electronics where size and cost are critical design parameters.

The SGM89111 is capable of driving 3Vrms into a 2.5kΩ load with 5V supply voltage. The device has differential inputs and uses external gain setting resistors that supports a gain range of ±1V/V to ±10V/V. The use of external gain resistors also allows the implementation of a 2nd-order low pass filter to compliment DAC's and SOC converters. The SGM89111 has build-in shutdown control for pop/click-free on/off control. The SGM89111's video driver employs an internal level shift circuit that avoids sync-pulse clipping and allows DC-coupled output.

Using the SGM89111 in audio products can reduce component count compared to traditional methods of generating a 3Vrms output. The SGM89111 doesn't require a power supply greater than 5V to generate an 8.5V_{PP} output, nor does the device require a split rail power supply. The SGM89111 integrates a charge pump to generate a negative supply rail that provides a clean, pop/click-free ground-biased 3Vrms output.

The SGM89111 is available in Green TSSOP-20 package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Capless Audio Driver Structure**
  - **Eliminates Pop/Clicks**
  - **Eliminates Output DC-Blocking Capacitors**
  - **Provides Flat Frequency Response from DC to 20kHz**
- **Low Noise and THD**
  - **Typical SNR = 107dB**
  - **Typical V_N = 9µVrms**
  - **Typical THD+N = 0.001% (f = 1kHz)**
- **3Vrms Output Voltage into 2.5kΩ Load with 5V Supply Voltage**
- **Support Differential Audio Signal Input**
- **Excellent SD Video Performance**
- **5th-Order Video Filter**
- **6dB Gain Video Driver**
- **Video Driver can Drive Two Video Loads**
- **Input Voltage Range Includes Ground**
- **Operates from 3.0V to 5.5V Single Power Supply**
- **Available in Green TSSOP-20 Package**

APPLICATIONS

Set-Top Box
Communication Devices
LCD TV
Blu-Ray DVD-Players
Home Theater in a Box

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM89111	TSSOP-20	SGM89111YTS20G/TR	SGM89111YTS20 XXXXX	Tape and Reel, 3000

NOTE: **XXXXX** = Date Code and Vendor Code.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage..-0.3V to 6V
Input Voltage (Audio)........................PV_{SS} - 0.3V to PV_{DD} + 0.3V
Input Voltage (Video)...........................GND - 0.3V to V_{CC} + 0.3V
Minimum Load Impedance (Audio R_L).............................> 600Ω
EN to GND...-0.3V to V_{DD} + 0.3V
Operating Temperature Range...........................-40℃ to +85℃
Junction Temperature..150℃
Storage Temperature Range............................ -65℃ to +150℃
Lead Temperature (Soldering, 10s)...……...……………… 260℃
ESD Susceptibility
HBM………………………………………………………......2500V
MM 250V

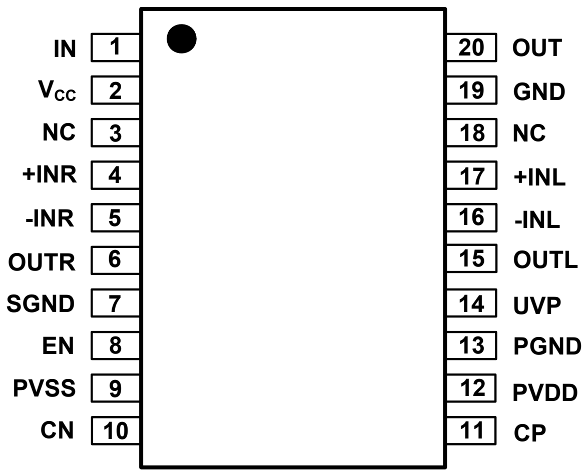
NOTE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

PIN CONFIGURATION (TOP VIEW)

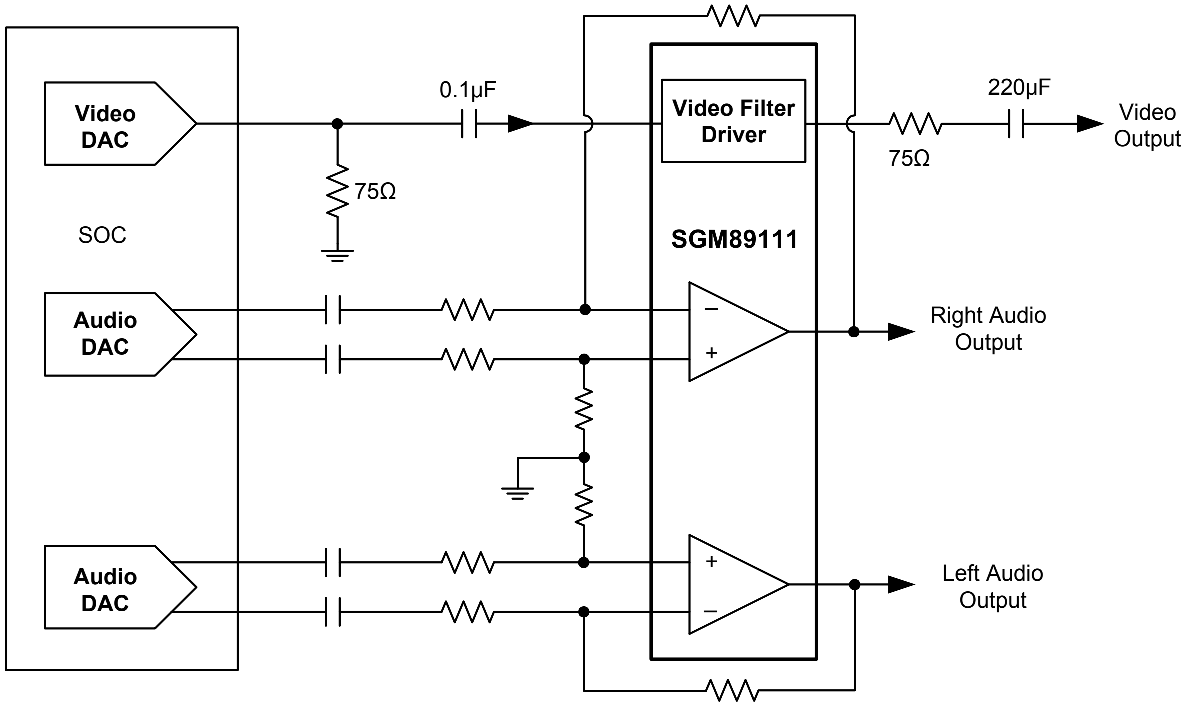


TSSOP-20

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IN	SD Video Signal Input.
2	V_{CC}	Power Supply of Video Driver.
3, 18	NC	No Connection.
4	+INR	Right Channel OPAMP Positive Input.
5	-INR	Right Channel OPAMP Negative Input.
6	OUTR	Right Channel OPAMP Output.
7	SGND	Audio Signal Ground.
8	EN	Enable Input for Audio Channel. Active High.
9	PVSS	Negative Supply Voltage Output.
10	CN	Charge Pump Flying Capacitor Negative Terminal.
11	CP	Charge Pump Flying Capacitor Positive Terminal.
12	PVDD	Positive Supply of Audio Driver.
13	PGND	Power Ground of Audio Driver.
14	UVP	Undervoltage Protection Input of Audio Channel.
15	OUTL	Left Channel OPAMP Output.
16	-INL	Left Channel OPAMP Negative Input.
17	+INL	Left Channel OPAMP Positive Input.
19	GND	Ground of Video Signal.
20	OUT	SD Driver Video Signal Output.

TYPICAL OPERATION CIRCUIT



ELECTRICAL CHARACTERISTICS OF STEREO LINE DRIVER

(T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ELECTRICAL CHARACTERISTICS					
Output Offset Voltage ($\lvert V_{OS} \rvert$)	V_{DD} = 3V to 5V		1.2	6	mV
Power Supply Rejection Ratio (PSRR)	V_{DD} = 3V to 5V		100		dB
High-Level Output Voltage (V_{OH})	V_{DD} = 3.3V, R_L = 2.5kΩ	3.18			V
Low-Level Output Voltage (V_{OL})	V_{DD} = 3.3V, R_L = 2.5kΩ			-3.05	V
High-Level Input Current (EN) ($\lvert I_{IH} \rvert$)	V_{DD} = 5V, V_I = V_{DD}			1	μA
Low-Level Input Current (EN) ($\lvert I_{IL} \rvert$)	V_{DD} = 5V, V_I = 0V			1	μA
Supply Current (I_{DD})	V_{DD} = 3.3V, no load, EN = V_{DD}		10.5	16	mA
	V_{DD} = 5V, no load, EN = V_{DD}		10.6	16.4	
	Shutdown mode, V_{DD} = 3V to 5V		0.1	0.18	
OPERATING CHARACTERISTICS (V_{DD} = 3.3V, R_L = 2.5kΩ, C_{PUMP} = 1μF, C_{PVSS} = 1μF, C_{IN2} = 10μF, R_{IN} = 10kΩ, R_{FB} = 20kΩ.) [1]					
Output Voltage (Outputs In Phase) (V_O)	THD = 1%, V_{DD} = 3.3V, f = 1kHz	2.05			Vrms
	THD = 1%, V_{DD} = 5V, f = 1kHz	3.05			
	THD = 1%, V_{DD} = 5V, f = 1kHz, R_L = 100kΩ	3.1			
Total Harmonic Distortion Plus Noise (THD+N)	V_O = 2Vrms, f = 1kHz		0.001		%
Crosstalk	V_O = 2Vrms, f = 1kHz		115		dB
Output Current Limit (I_O)	V_{DD} = 3.3V		20		mA
Input Resistor Range (R_{IN})			10		kΩ
Feedback Resistor Range (R_{FB})			20		kΩ
Slew Rate			9		V/μs
Maximum Capacitive Load			220		pF
Noise Output Voltage (V_N)	A-weighted, BW = 22kHz		9		μVrms
Signal to Noise Ratio (SNR)	A-weighted, V_O = 3Vrms, THD+N = 0.1%, BW = 22kHz		107		dB
Unity Gain Bandwidth (G_{BW})			6.6		MHz
Open-Loop Voltage Gain (A_{VO})			120		dB
Charge Pump Frequency (F_{CP})		290	410	550	kHz
External Undervoltage Detection (V_{UVP})		1.03	1.13	1.23	V
External Undervoltage Detection Hysteresis Current (I_{Hys})			4.3		μA
SHUTDOWN PIN					
Input High Voltage (V_{INH})		1.2			V
Input Low Voltage (V_{INL})				0.6	V
RECOMMENDED OPERATING CONDITIONS					
DC Supply Voltage (V_{DD})		3		5.5	V

NOTE:

1. For C_{PUMP}, C_{PVSS}, C_{IN2}, R_{IN}, R_{FB} and etc, please refer to the APPLICATION CIRCUIT on page 11.

ELECTRICAL CHARACTERISTICS OF VIDEO DRIVER

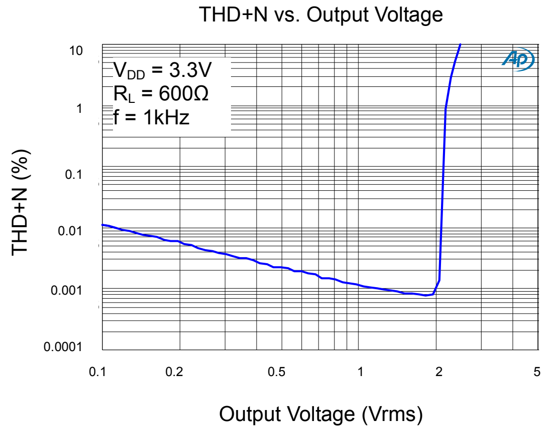
(V_{CC} = 5.0V, at R_L = 150Ω connected to GND, V_{IN} = 1V_{PP}, and C_{IN1} = 0.1μF [(2)], all outputs AC-coupled with 220μF, referenced to 400kHz, T_A = +25℃, unless otherwise noted.)

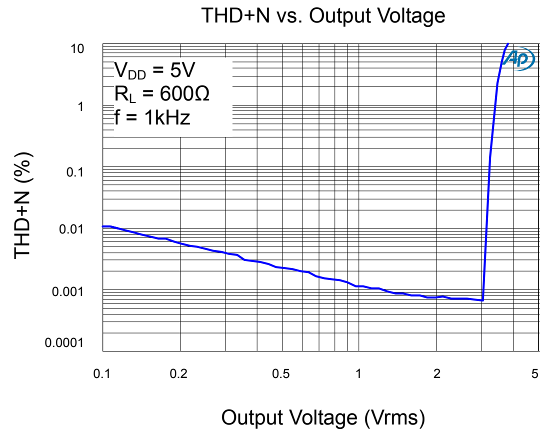
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Output Level Shift Voltage (V_{OLS})	V_{IN} = 0V, no load		360	520	mV
Voltage Gain (A_V)	R_L = 150Ω	5.6	6	6.4	dB
OUTPUT CHARACTERISTICS					
Output Voltage High Swing	V_{IN} = 3.0V, R_L = 150Ω to GND		4.82		V
Output Short-Circuit Current (I_{SC})	V_{IN} = 0.4V, OUT shorted to GND through 10Ω		115		mA
	V_{IN} = 1.7V, OUT shorted to V_{CC} through 10Ω		-120		
POWER SUPPLY					
Operating Voltage Range (V_{CC})		3.0		5.5	V
Power Supply Rejection Ratio (PSRR)	V_{CC} = 3.5V to 5.0V		50		dB
Quiescent Current (I_Q)	V_{IN} = 0.5V		7	9.6	mA
DYNAMIC PERFORMANCE					
-0.1dB Bandwidth			5.6		MHz
-1dB Bandwidth			6.6		MHz
-3dB Bandwidth			7.6		MHz
Filter Response (Normalized Gain)	f_{IN} = 27MHz		42		dB
Slew Rate	2V output step, 80% to 20%		35		V/μs
Group Delay Variation (D/DT)	Difference between 400kHz and 6.5MHz		30		ns
Fall Time	2V output step, 80% to 20%		34		ns
Rise Time	2V output step, 80% to 20%		33		ns

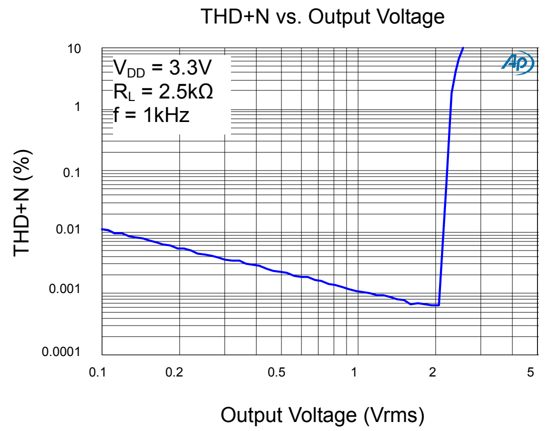
NOTE:
2. For C_{IN1} and etc, please refer to the APPLICATION CIRCUIT on page 11.

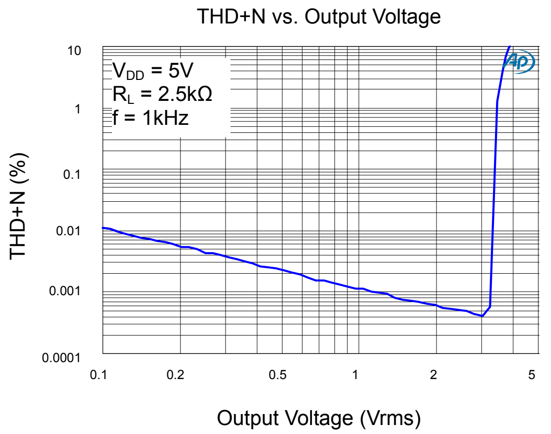
TYPICAL PERFORMANCE CHARACTERISTICS OF STEREO LINE DRIVER

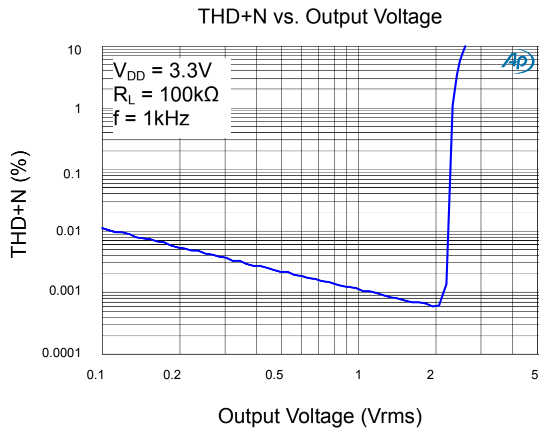
T_A = +25℃, C_{PUMP} = 1μF, C_{PVSS} = 1μF, C_{IN2} = 10μF, R_{IN} = 10kΩ, R_{FB} = 20kΩ, unless otherwise noted.

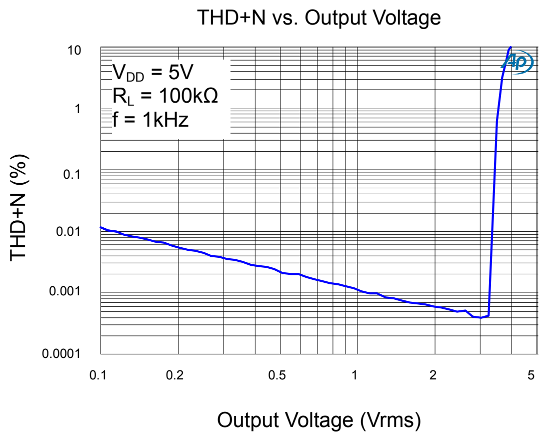








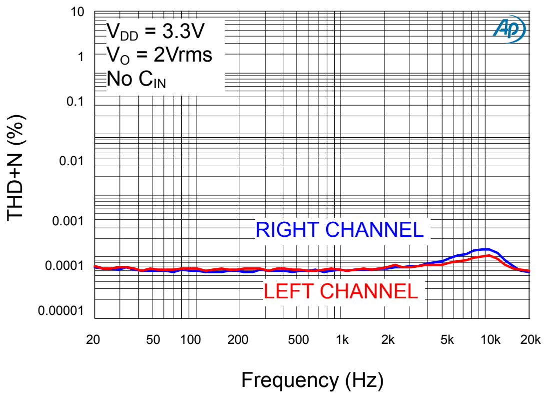




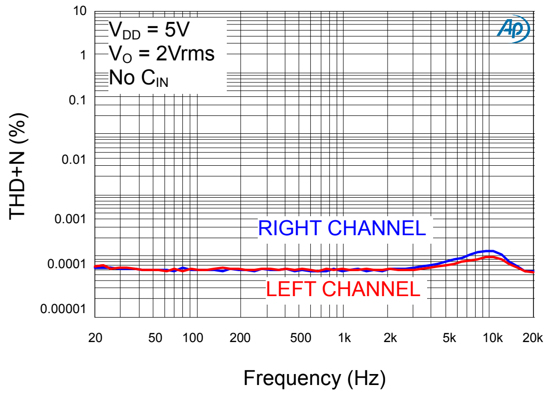
TYPICAL PERFORMANCE CHARACTERISTICS OF STEREO LINE DRIVER

T_A = +25°C, R_L = 2.5kΩ, C_{PUMP} = 1µF, C_{PVSS} = 1µF, C_{IN2} = 10µF, R_{IN} = 10kΩ, R_{FB} = 20kΩ, unless otherwise noted.

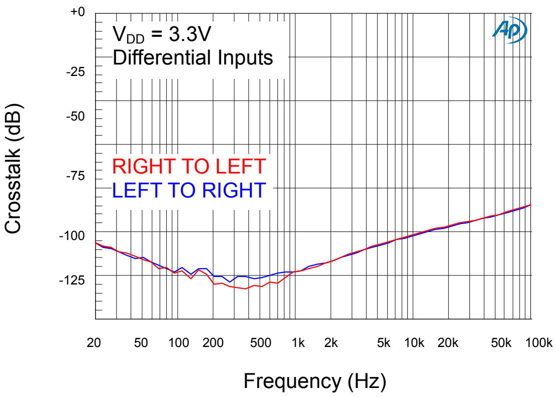
THD+N vs. Frequency



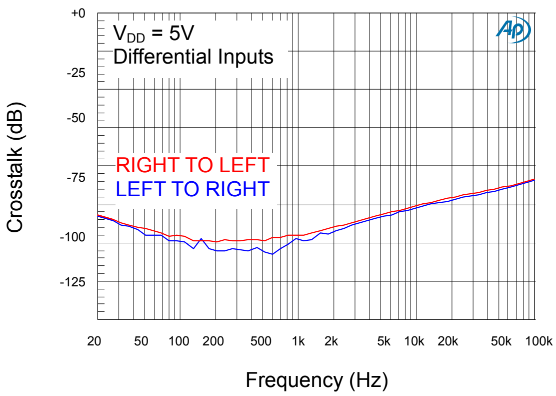
THD+N vs. Frequency



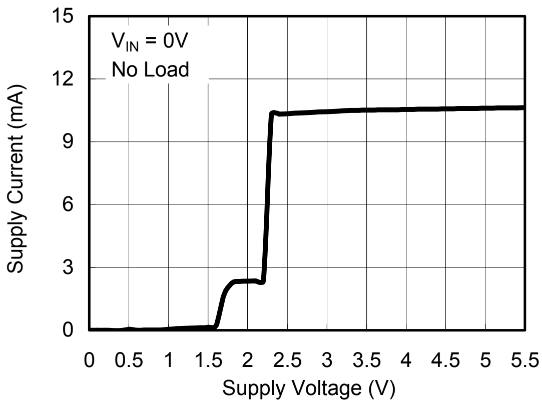
Crosstalk vs. Frequency



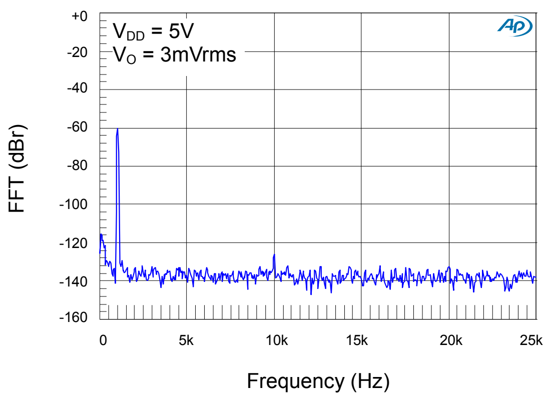
Crosstalk vs. Frequency



Supply Current vs. Supply Voltage

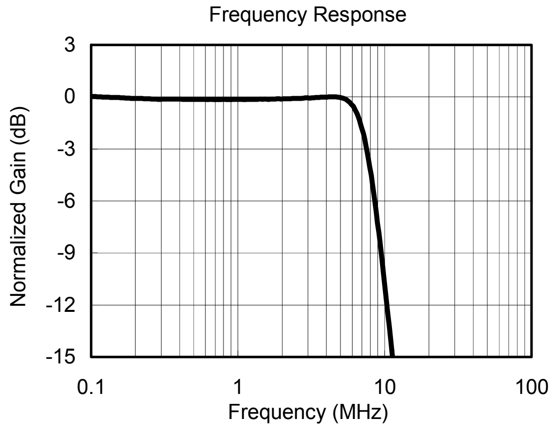


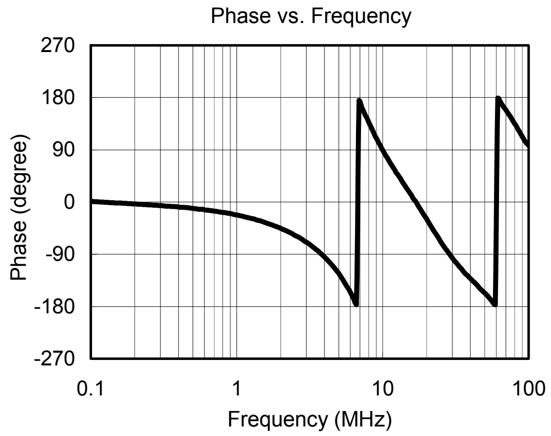
FFT vs. Frequency

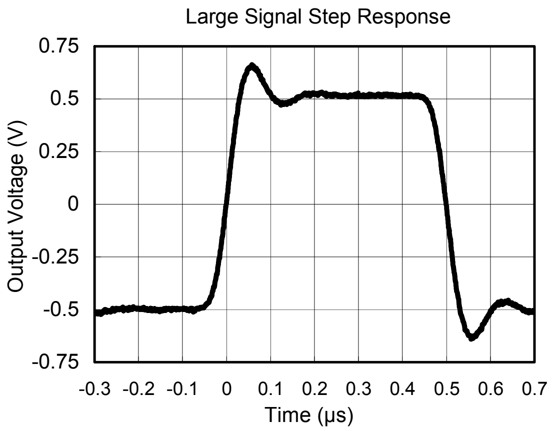


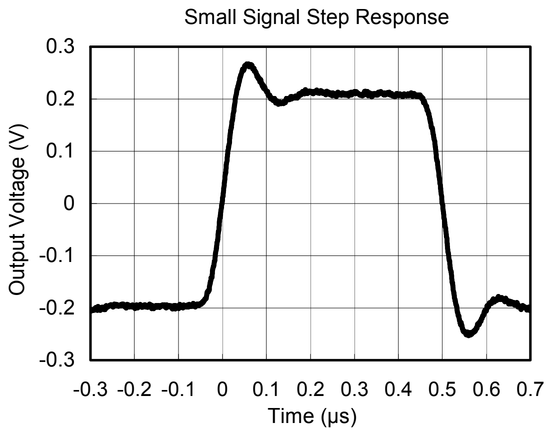
TYPICAL PERFORMANCE CHARACTERISTICS OF VIDEO DRIVER

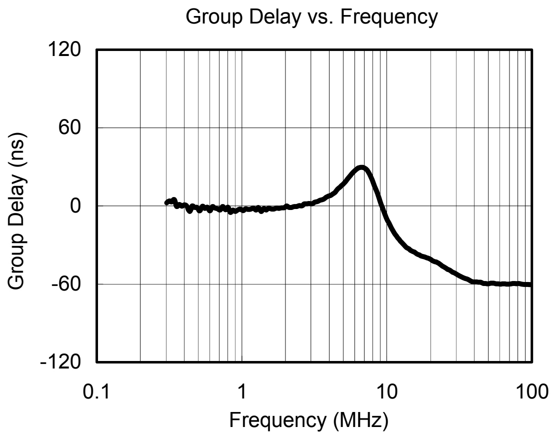
At V_{CC} = 5V, T_A = +25℃, R_L = 150Ω, all outputs AC-coupled with 220μF, unless otherwise noted.

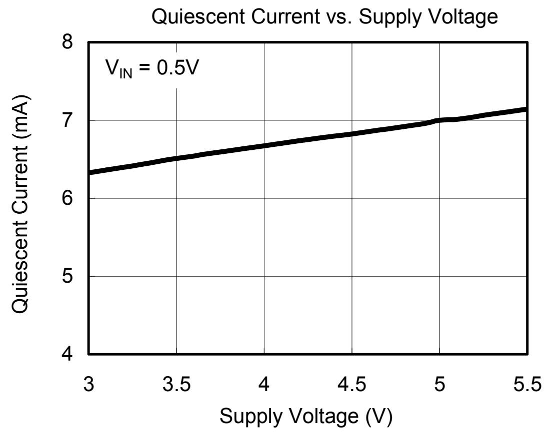






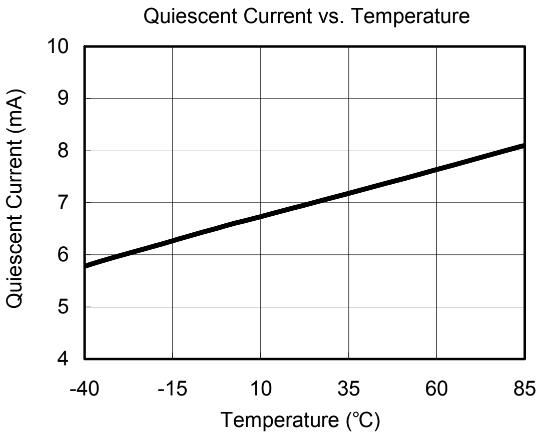


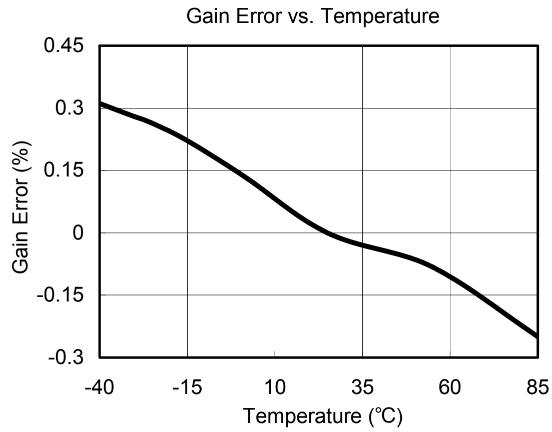


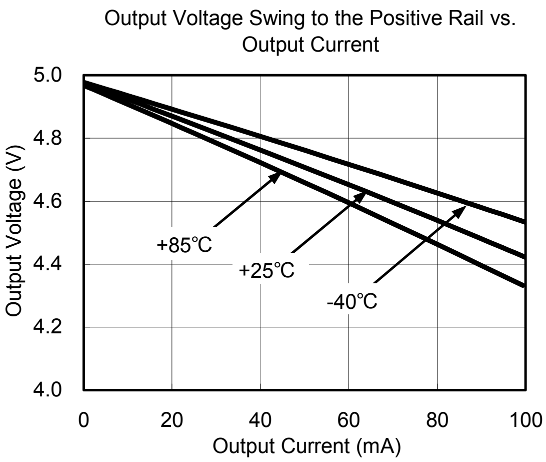


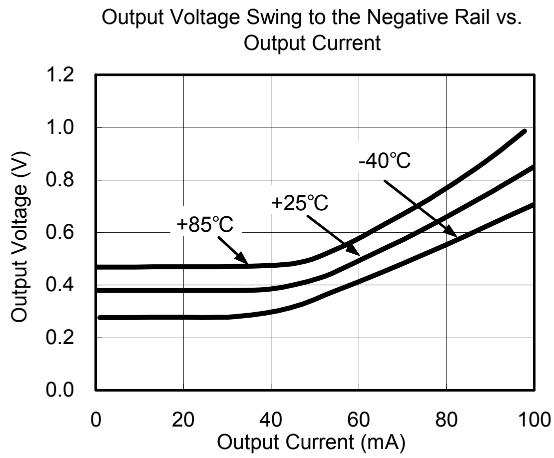
TYPICAL PERFORMANCE CHARACTERISTICS OF VIDEO DRIVER

At V_{CC} = 5V, T_A = +25℃, R_L = 150Ω, all outputs AC-coupled with 220μF, unless otherwise noted.

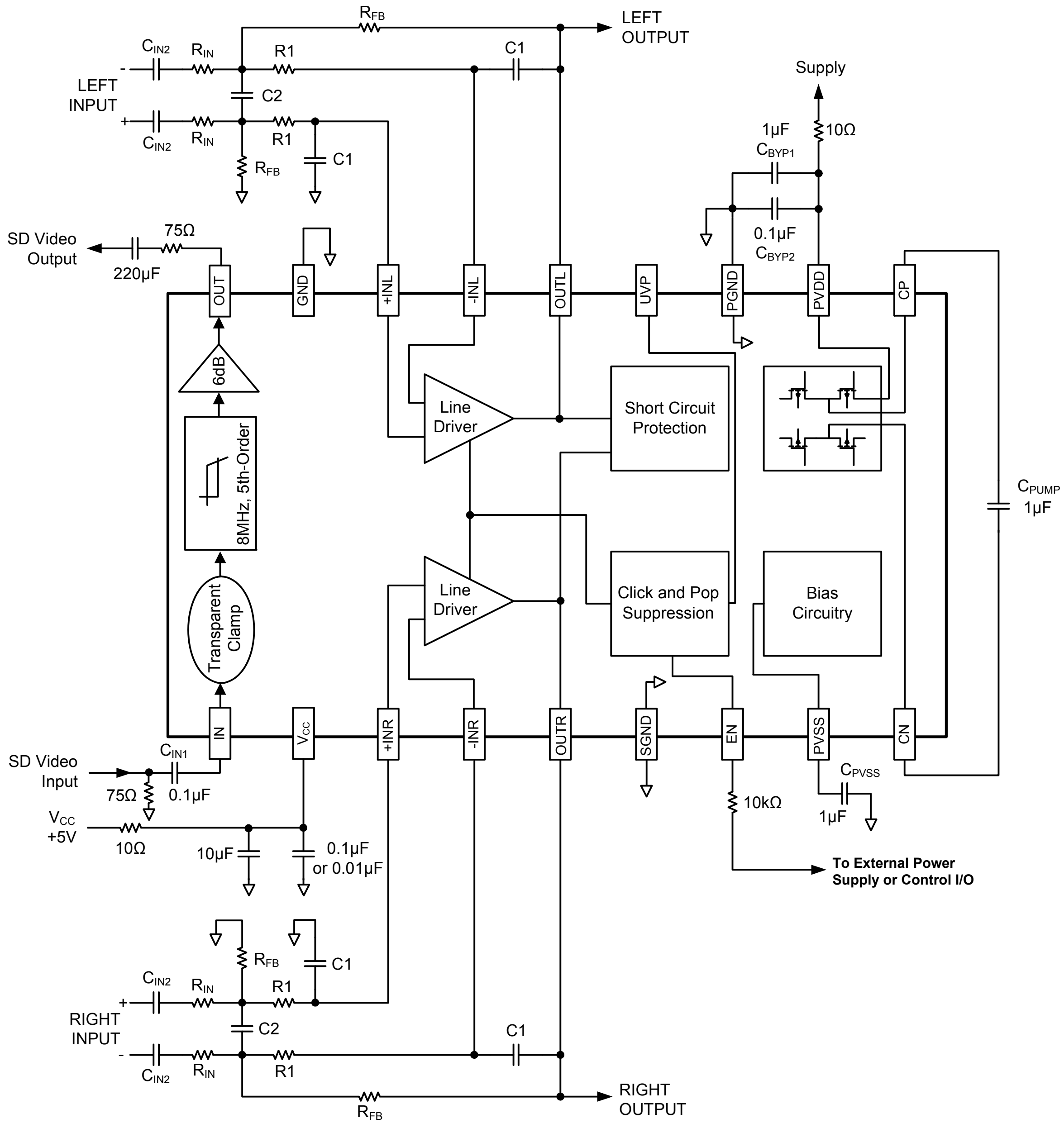








APPLICATION CIRCUIT



NOTES:

1. In order to get good performance, it's important to select the right C_{PUMP}, C_{PVSS}, C_{BYP1} and C_{BYP2} in application. All tests are performed with circuit set up with X5R and X7R capacitors. Capacitors having high dissipative loss, such as Y5V capacitor, may cause performance degradation and unexpected system behavior.
2. A 10kΩ resistor must be serially connected to EN pin.
3. Power supply V_{CC} must be sequenced on first before input video signals.
4. Two serial 10Ω resistors are recommended to be used.

APPLICATION INFORMATION OF SD VIDEO FILTER AND DRIVER

Functional Description

SGM89111 operates from a single 3.0V to 5.5V supply. In application, SGM89111 is a fully integrated solution for filtering and buffering SDTV signals in front of video decoder or behind video encoder. For example, SGM89111 can replace a passive LC filter and an amplifier driver at CVBS side in set-top box and DVD player. This solution can help reduce PCB size and production cost, and it also improves video signal performance comparing with traditional design using discrete components. SGM89111 features a DC-coupled input buffer, a 5-pole low-pass filter to eliminate out-of-band noise of video encoder, and a gain of 6dB in the output amplifier to drive 75Ω load. The AC- or DC-coupled input buffer eliminates sync crush, droop, and field tilt. The output of SGM89111 also can be DC-coupled or AC-coupled.

Input Considerations

Besides AC coupling, the SGM89111 inputs also can be DC-coupled. In DC coupling application, no input coupling capacitors are needed because the amplitude of input video signal from DAC includes ground and extends up to 1.4V, and SGM89111 can be directly connected to the output of a single-supply, current-output DAC without any external bias network. In applications where DAC's output level exceeds the range from 0V to 1.4V, or SGM89111 is driven by an unknown external source or a SCART switch which has its own clamping circuit, AC coupling is needed.

Output Considerations

The SGM89111 outputs can be DC-coupled or AC-coupled. When input is 0V, the SGM89111 output voltage is 360mV typically. In DC coupling design, one 75Ω resistor is used to connect SGM89111's output pin with external load directly, and this serial back-termination resistor is used to match the impedance of the transmission line between SGM89111 and external load to cancel the signal reflection. The SGM89111 outputs can sink and source current allowing the device to be AC-coupled with external load. In AC coupling, at least 220μF capacitor will be used in order to eliminate field tilt.

SGM89111 is designed to drive two video lines simultaneously - essentially a 75Ω load, while keeping the output dynamic range as wide as possible.

Power-Supply Bypassing and Layout

Correct power supply bypassing is very important for optimizing video performance in design. One 0.1μF and one 10μF capacitors are always used to bypass V_{CC} pin of SGM89111. Place these two capacitors as close to the SGM89111 supply pin as possible. A large ground plane is also needed to ensure optimum performance. The input and output termination resistors should be placed as close to the related pins of SGM89111 as possible to avoid performance degradation. The PCB traces at the output side should have 75Ω characteristic impedance in order to match the 75Ω characteristic impedance of the cable connecting external load. In design, keep the board trace at the inputs and outputs of the SGM89111 as short as possible to minimize the parasitic stray capacitance and noise pickup.

APPLICATION INFORMATION OF AUDIO DRIVER

Decoupling Capacitors

The SGM89111 is a capless line driver amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device V_{DD} lead, works best. Placing this decoupling capacitor close to the SGM89111 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10μF or larger capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Gain Setting Resistors Ranges

The gain setting resistors, R_{IN} and R_{FB}, must be chosen so that noise, stability and input capacitor size of the SGM89111 are kept within acceptable limits. Voltage gain is defined as R_{FB} divided by R_{IN}.

Selecting values that are too low demands a large input AC coupling capacitor, C_{IN2}. Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different gain settings.

Table 1. Recommended Resistor Values

INPUT RESISTOR VALUE, R_{IN}	FEEDBACK RESISTOR VALUE, R_{FB}	DIFFERENTIAL INPUT GAIN	INVERTING INPUT GAIN	NON INVERTING INPUT GAIN
22kΩ	22kΩ	1.0V/V	-1.0V/V	2.0V/V
20kΩ	30kΩ	1.5V/V	-1.5V/V	2.5V/V
33kΩ	68kΩ	2.1V/V	-2.1V/V	3.1V/V
10kΩ	100kΩ	10.0V/V	-10.0V/V	11.0V/V

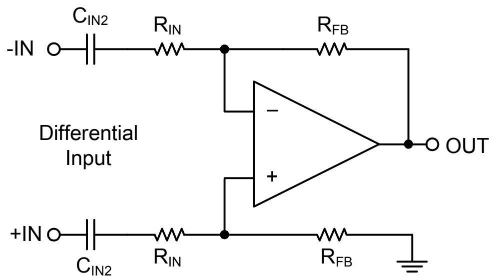


Figure 1. Differential Input

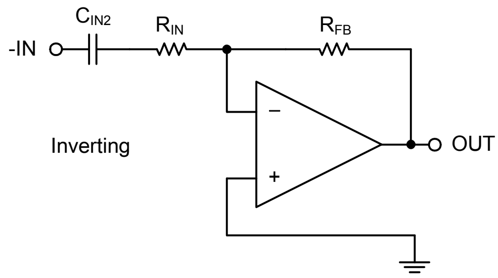


Figure 2. Inverting

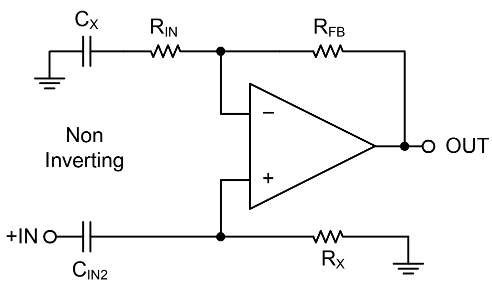


Figure 3. Non-Inverting

APPLICATION INFORMATION OF AUDIO DRIVER

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the SGM89111. These capacitors block the DC portion of the audio source and allow the SGM89111 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC-gain to one, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1, then the frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN2}} \quad \text{or} \quad C_{IN2} = \frac{1}{2\pi fc_{IN} R_{IN}} \qquad (1)$$

Using the SGM89111 as 2nd-Order Filter

Several audio DACs used today require an external low-pass filter to remove out of band noise. This is possible with the SGM89111 as it can be used like a standard OPAMP.

Several filter topologies can be implemented both single-endedly and differentially. In Figure 4, a Multi Feedback (MFB), with differential input and single-ended input is shown.

An AC coupling capacitor to remove DC-content from the source is shown. It serves to block any DC-content from the source and lowers the DC-gain to one, helping reducing the output DC-offset to minimum.

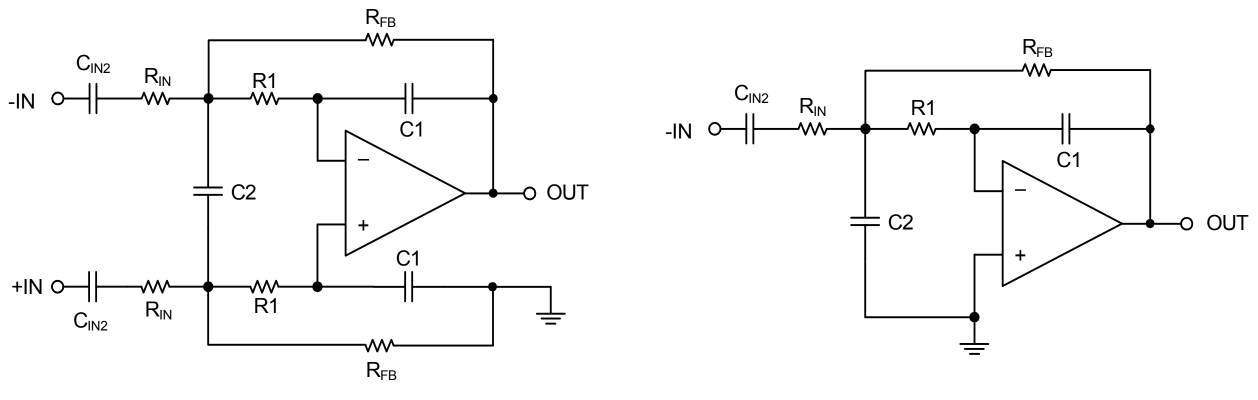


Figure 4. 2nd-Order Active Low Pass Filter

The resistor values should be kept low to obtain low noise, but should also be high enough value to get a small size AC coupling cap. Using 5.6kΩ for the resistors, C1 = 220pF, and C2 = 470pF, an SNR of 107dB can be achieved with a 10μF input AC coupling capacitor.

APPLICATION INFORMATION OF AUDIO DRIVER

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{SD}$ (EN) (shutdown pin) low during power supply ramp up and down. The EN pin should be kept low until the input AC coupling capacitors are fully charged before asserting the EN pin high. This way proper precharge of the AC coupling is performed, and pop-free power-up is achieved. Figure 5 illustrates the preferred sequence.

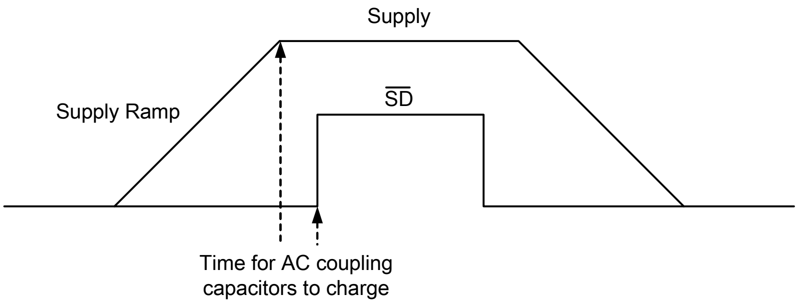


Figure 5. Power-Up Sequence

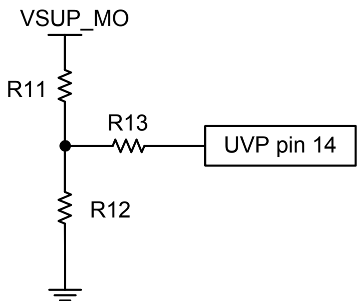
External Undervoltage Detection

External undervoltage detection can be used to mute/shut down the SGM89111 before an input device can generate a pop.

The threshold seen at the UVP pin is 1.13V. A hysteresis is introduced with a resistive divider, where thresholds for startup and shutdown are determined respectively as follows:

Startup Threshold: V_{UDPR} = 1.13V × (R11 + R12) / R12
Shutdown Threshold: V_{UDPF} = 1.13V × (R11+R12) / R12 - 4.6μA × (R13 + R11 || R12) × (R11 + R12) / R12
Hysteresis: 4.3μA × (R13 + R11 || R12) × (R11 + R12) / R12

The R13 is optional. If the R13 is not used, the UVP pin connects to the divider center tap directly.



Capacitive Load

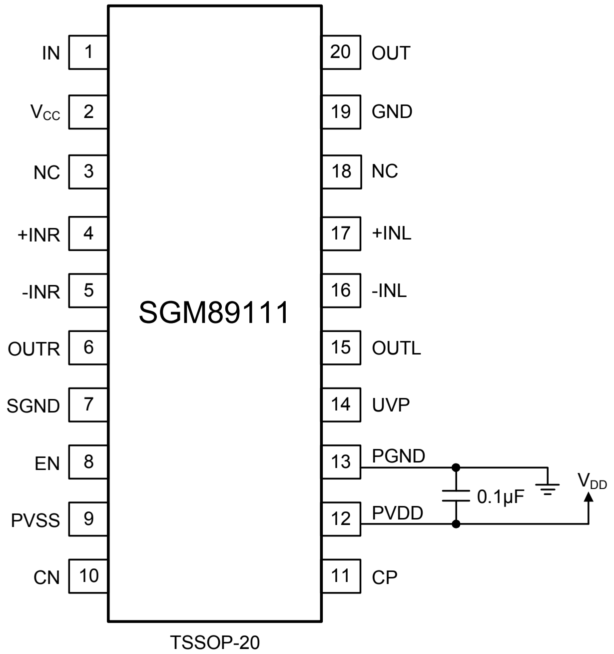
The SGM89111 has the ability to drive large capacitive load up to 220pF directly, and larger capacitive loads can be accepted by adding a series resistor of 47Ω or larger.

Gain-Setting Resistors

The gain setting resistors, R_{IN} and R_{FB}, must be placed close to the input pins to minimize the capacitive loading on these pins and to ensure maximum stability of the SGM89111.

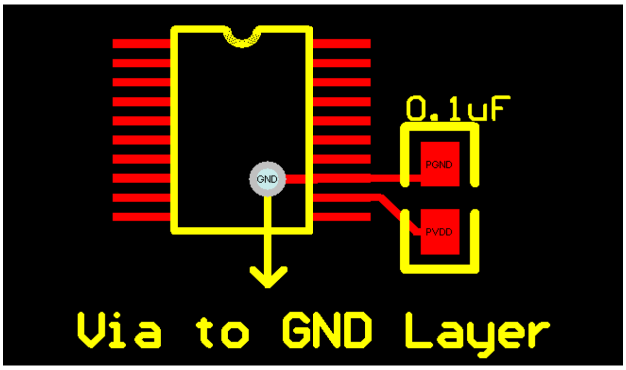
APPLICATION INFORMATION OF AUDIO DRIVER

PCB Layout Guide

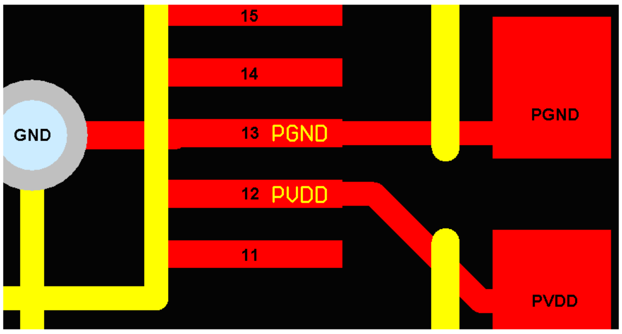


NOTE: 0.1μF decoupling capacitor must be close to PGND and PVDD pins; capacitor can be connected between PVDD and PGND pins directly and then connect PGND pin to GND layer.

The reference PCB layout is shown in below:

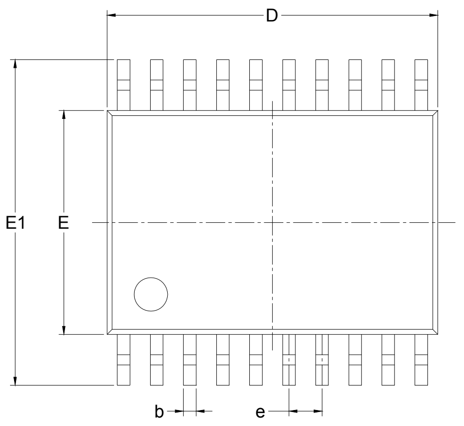


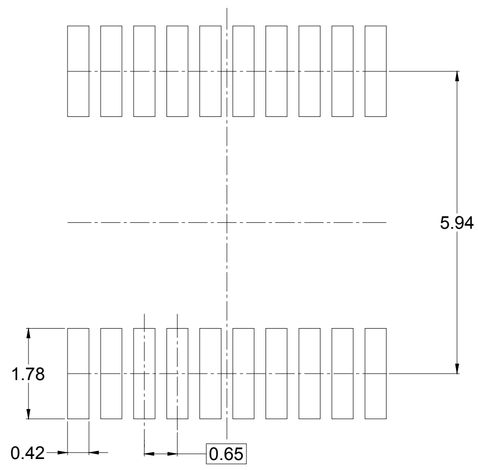
Zoomed in:



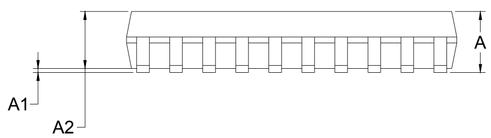
PACKAGE OUTLINE DIMENSIONS

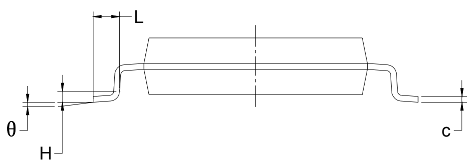
TSSOP-20





RECOMMENDED LAND PATTERN (Unit: mm)

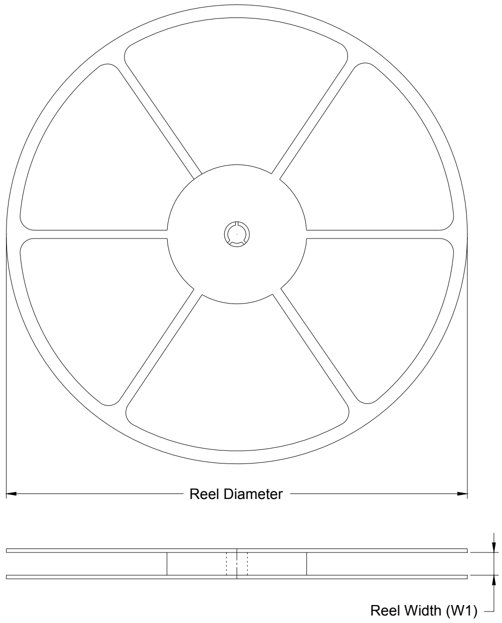




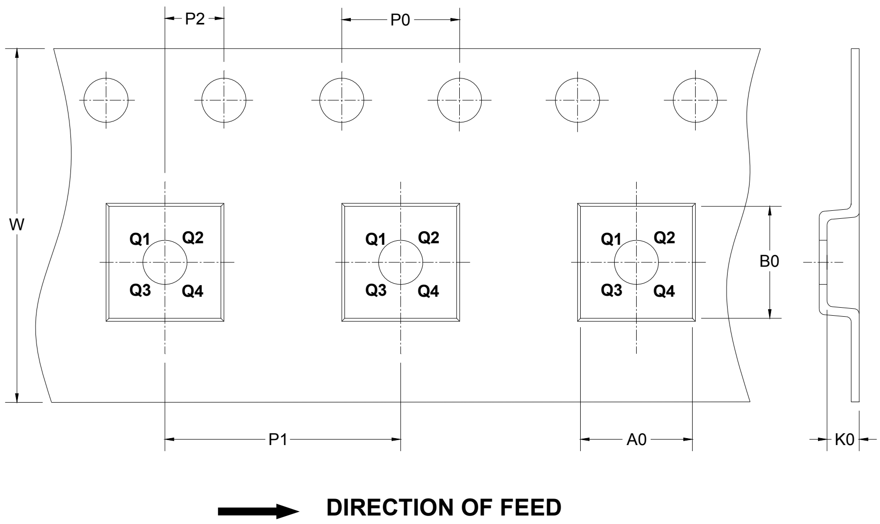
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

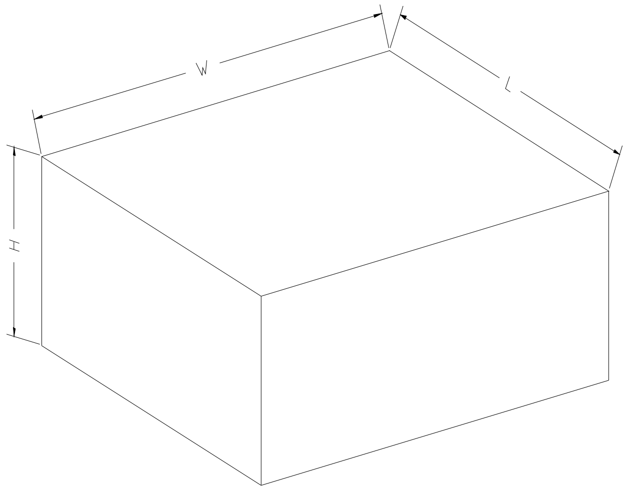


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-20	13″	12.4	6.8	6.85	1.7	4.0	8.0	2.0	12.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5