SGM5347-12
8 Channels, 12-Bit Digital-to-Analog Converter with Output Operational Amplifier

GENERAL DESCRIPTION

The SGM5347-12 features 8 channels of 12-bit digital-to-analog converter (DAC) with output amplifiers. The output amplifier provides high current drive capability. The digital data is input via a serial link bus. Only three control lines are required, and cascaded connections can be used.

The SGM5347-12 is suitable for electronic volume control and replacement for potentiometers for adjustment, in addition to normal DAC applications.

The SGM5347-12 is available in Green SOIC-16 and TSSOP-16 packages. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Low Power Consumption (0.5mW/CH)**
- **Integrating 8 Channels of 12-Bit DAC**
- **Simultaneous 8 Channels Output Updating**
- **Build-in Analog Output Amplifier with Sink/Source Current Capability and Short Current Control**
- **The Range of D/A Conversion can be Independently Set by Separating the Power Supply for MCU Interface and Operational Amplifier and the Power Supply for DAC**
- **Capable of being Controlled Directly by a 3V MCU**
- **Individual Channel Power-Down Capability**
  - **0.6μA (TYP) I_{CC} for Power-Down Mode**
- **Power-On Reset: Output Reset to GND**
- **Daisy-Chain Capability**
- **Serial Data Input: Up to 2.5MHz Operation**
- **Wide Power Supply Range: 2.8V to 5.5V**
- **Available in Green SOIC-16 and TSSOP-16 Packages**

TYPICAL APPLICATION

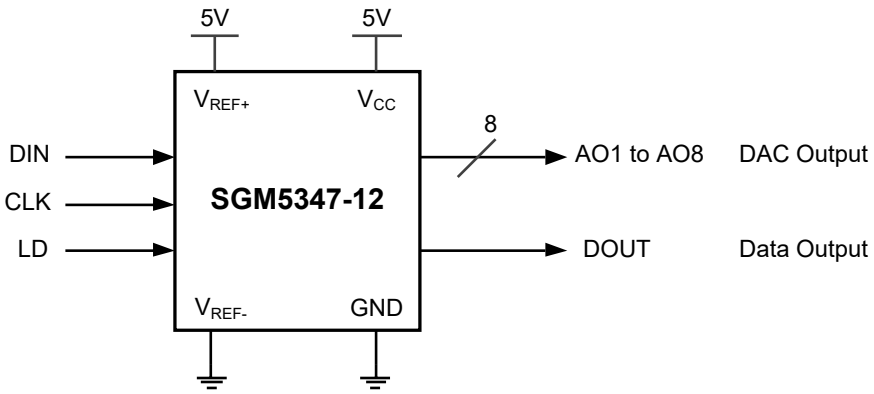


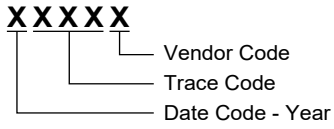
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5347-12	SOIC-16	-40℃ to +125℃	SGM5347-12XS16G/TR	SGMMP0XS16 XXXXX	Tape and Reel, 2500
	TSSOP-16	-40℃ to +125℃	SGM5347-12XTS16G/TR	SGMMP1 XTS16 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range (1)

V_{CC} ..... -0.3V to 6.5V

V_{REF+} ..... -0.3V to 6.5V

V_{REF-} ..... GND ± 0.3V

Input Voltage Range, V_{IN} .....-0.3V to V_{CC} + 0.3V

Output Voltage Range, V_{OUT} .....-0.3V to V_{CC} + 0.3V

Package Thermal Resistance

SOIC-16..... 90℃/W

TSSOP-16 ..... 120℃/W

Junction Temperature.....+150℃

Storage Temperature Range .....-65℃ to +150℃

Lead Temperature (Soldering, 10s).....+260℃

ESD Susceptibility

HBM.....4000V

CDM 1000V

NOTE: 1. $V_{CC} \geq V_{REF+}$.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range.....-40℃ to +125℃

Power Supply Voltage 1

V_{CC} .....2.8V to 5.5V

GND.....0V

Power Supply Voltage 2 (V_{REF+} - V_{REF-} ≥ 0.5V)

V_{REF+} ..... 0.5V to V_{CC}

V_{REF-} ..... GND

Oscillation Limited Output Capacitance, C_{OL} .....2nF (TYP)

Digital Data Setting Range.....#000 to #FFF

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

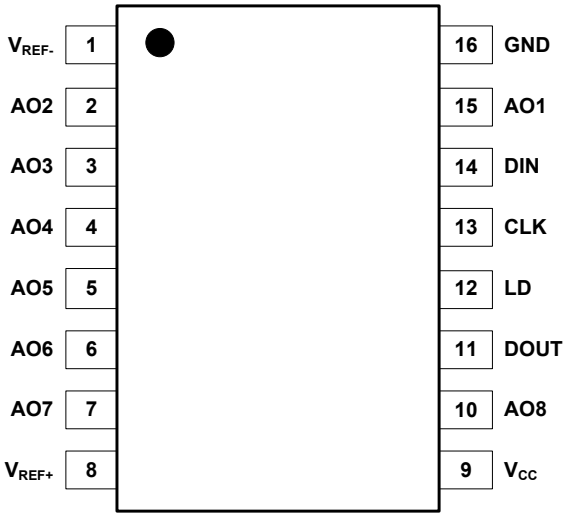
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

(TOP VIEW)



SOIC-16/TSSOP-16

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	V_{REF-}	-	Negative Reference Voltage Input. Always connect this pin to ground in application.
8	V_{REF+}	-	Positive Reference Voltage Input.
9	V_{CC}	-	Power Supply Pin. Power supply pin of MCU interface and operational amplifier.
16	GND	-	Ground Pin. Ground pin of MCU interface and operational amplifier.
15, 2, 3, 4, 5, 6, 7, 10	AO1-AO8	O	DAC Output Pins. These pins are 12-bit DAC outputs with operational amplifiers.
11	DOUT	O	Data Output Pin. This pin outputs MSB of the 16-bit shift register.
12	LD	I	Load Signal Input Pin. If LD pin is brought from low to high, the data of shift register is loaded to the decoder and the register for DAC output.
13	CLK	I	Shift Clock Input Pin. The input signal from the DIN pin is input to a 16-bit shift register on the rising edge of the shift clock.
14	DIN	I	Serial Data Input Pin. This pin inputs 16-bit length serial data.

NOTE: DIN, CLK, and LD pins should remain "L" level at non-data transfer.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.8V to 5.5V, T_A = -40℃ to +125℃, V_{REF+} = V_{CC}, V_{REF-} = GND, C_L = 200pF to GND, input code range from 48 to 4047. Typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Analog DC Performance					
Resolution		12			Bit
INL (1)			3	11	LSB
DNL (2)	Monotonicity guaranteed by design	-0.7		0.85	LSB
Offset			3	15	mV
Gain Error			0.1	0.45	%FSR
Offset Drift			10	60	μV/℃
Gain Drift			2	15	ppmFS/℃
Zero Code Error	0μA current load		3	15	mV
	200μA current load		5		
	1mA current load		8		
Full Scale Error	0μA current load		3	25	mV
	200μA current load		6		
	1mA current load		20		
Zero Code Drift			5		μV/℃
Full Scale Error Drift			5		μV/℃
Analog AC Performance					
Output Settling Time	To 1LSB		7		μs
Slew Rate	C_{LOAD} = 200pF		0.9		V/μs
Noise Density	Code = 0x800, f = 1kHz		30		nV/$\sqrt{Hz}$
Noise	30kHz LPF		17		μV_{RMS}
Multiplying Bandwidth			300		kHz
Wake-Up Time	C_{LOAD} = 200pF		8		μs
Output Characteristics					
Output Resistance			0.3		Ω
Short Current	Sink		37		mA
	Source		37		
Continuous Current (3)	V_{CC} = 2.8V		5		mA
	V_{CC} = 5.5V		10		
Maximum Capacitance Load			2		nF
Reference Characteristics					
V_{REF+}		0.5		V_{CC}	V
Input Impedance			25		kΩ
Digital Input Characteristics					
Input Current			0.1	1	μA
Input Low Voltage	V_{CC} = 2.8V to 3.6V			0.6	V
	V_{CC} = 4.5V to 5.5V			0.8	
Input High Voltage	V_{CC} = 2.8V to 3.6V	2.3			V
	V_{CC} = 4.5V to 5.5V	3.5			
Input Hysteresis			0.2		V

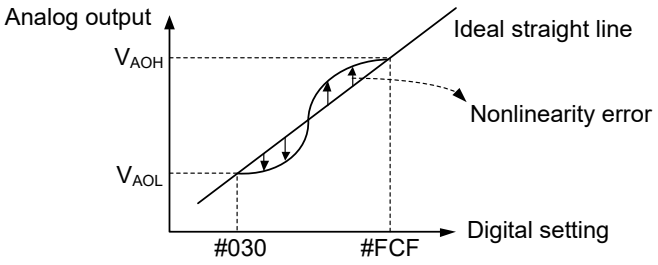
ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 5.5V, T_A = -40℃ to +125℃, V_{REF+} = V_{CC}, V_{REF-} = GND, C_L = 200pF to GND, input code range from 48 to 4047. Typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Power-On Reset						
Reset Level		MIN for minimum entry level, MAX for maximum release level	2.45	2.6	2.78	V
Hysteresis		Difference between reset release level and entry level		40		mV
Power Consumption						
Normal Operation Mode	I_{CC}	V_{CC} = 5V		0.5	0.8	mA
	I_{REF+}	V_{REF+} = 5V		0.2	0.4	
Power-Down Mode		V_{CC} = 5V		0.6	3	μA
		V_{REF+} = 5V		0.01	1	

NOTES:

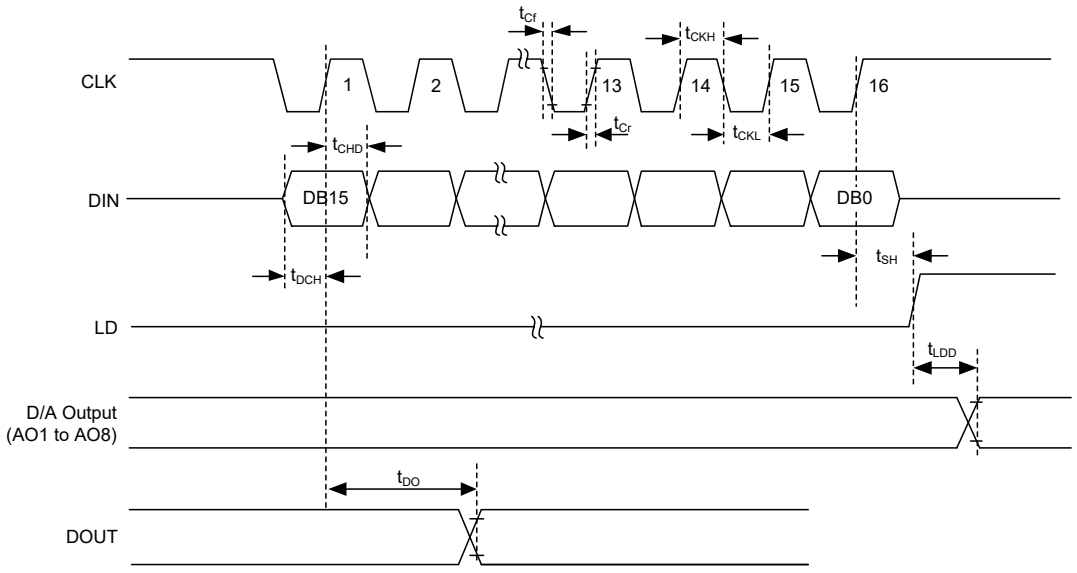
1. Nonlinearity error: The error of the I/O curve deviated from the ideal straight line between output voltages at "#030" and "#FCF".
2. Differential nonlinearity error: The error deviated from the ideal increment given when the digital value is incremented by one bit.
3. At +125℃, please limit the output current of each channel to 5mA for maximum operating life time.



TIMING CHARACTERISTICS

(V_{CC} = 2.8V to 5.5V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
"L" Level Clock Pulse Width	t_{CKL}		200			ns
"H" Level Clock Pulse Width	t_{CKH}		200			ns
Clock Rising Time	t_{Cr}				200	ns
Clock Falling Time	t_{Cf}					
Data Setup Time	t_{DCH}		30			ns
Data Hold Time	t_{CHD}		60			ns
Load Setup Time	t_{CHL}		200			ns
Load Hold Time	t_{LDC}		100			ns
"H" Level Load Pulse Width	t_{LDH}		100			ns
Data Output Delay Time	t_{DO}		70		350	ns
D/A Output Settling Time	t_{LDD}				100	μs
LD Hold Time after the 16th Rising Edge of CLK	t_{SH}		60			ns



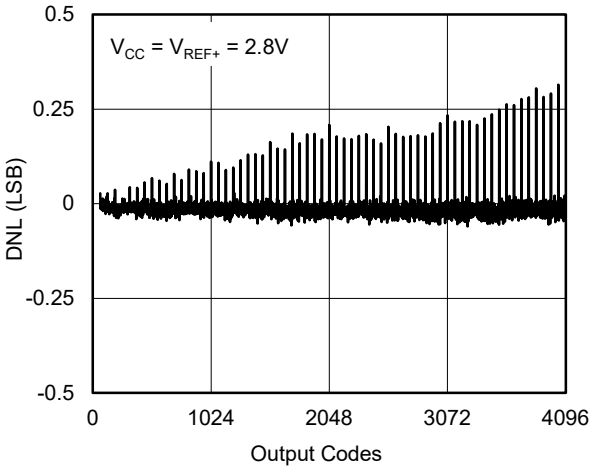
NOTES:
1. The D/A output evaluation levels are 90% and 10% of V_{CC}. The other evaluation levels are 80% and 20% of V_{CC}.
2. Please ensure of the 16 bits of data are sent before the rising edge of LD.

Figure 2. Input/Output Timing

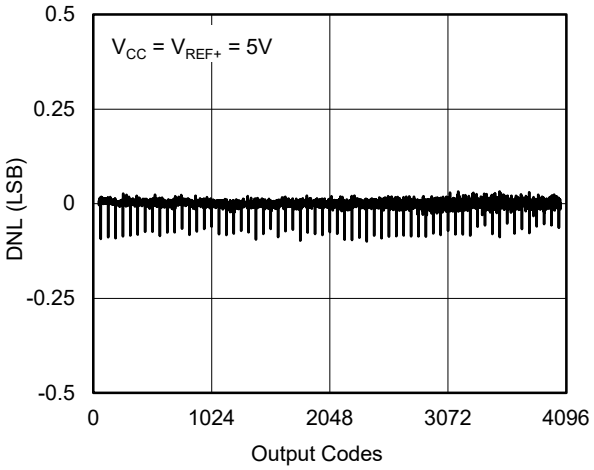
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

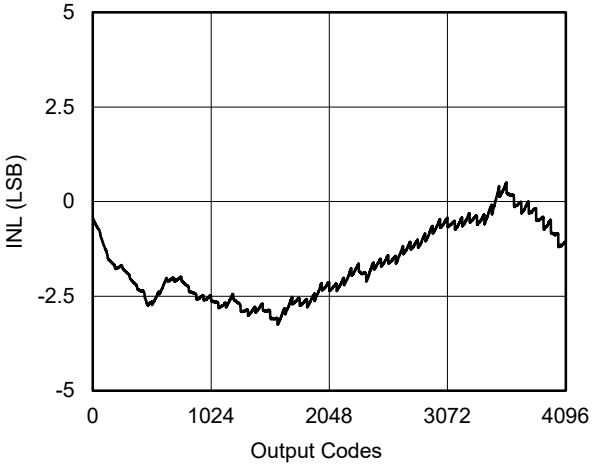
DNL vs. Output Codes



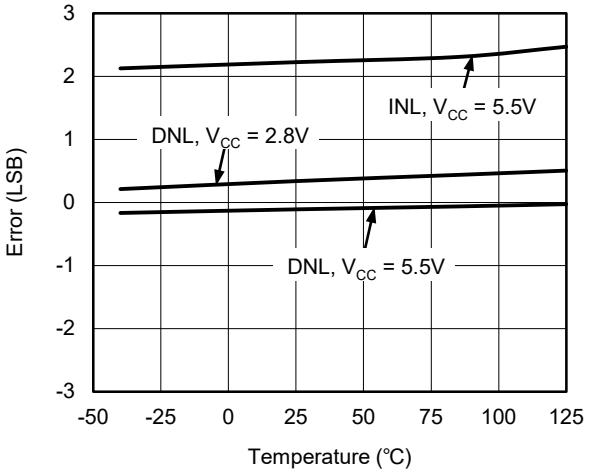
DNL vs. Output Codes



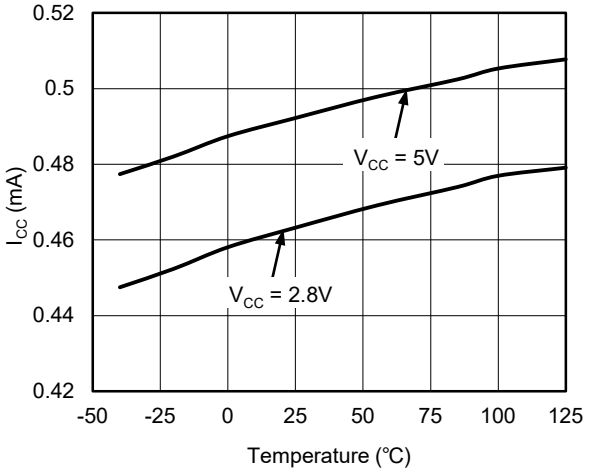
INL vs. Output Codes



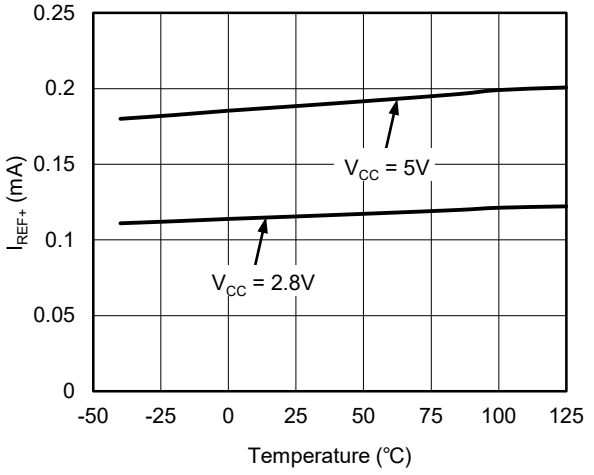
INL and DNL vs. Temperature



I_{CC} vs. Temperature



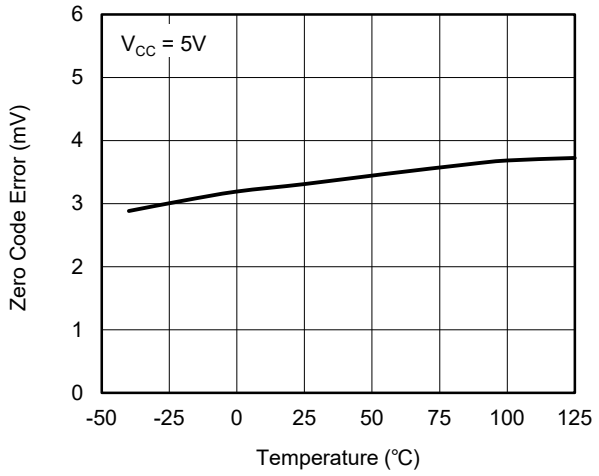
I_{REF+} vs. Temperature



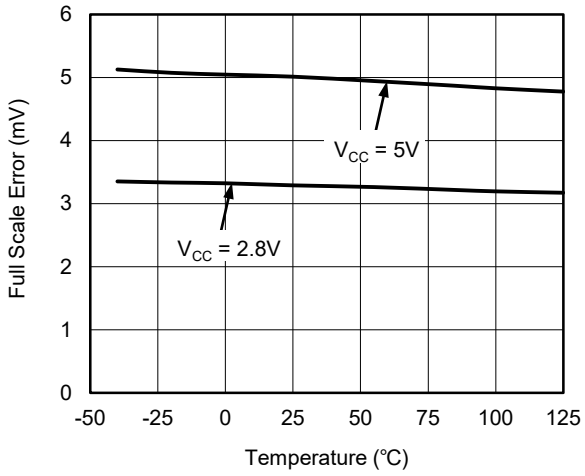
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

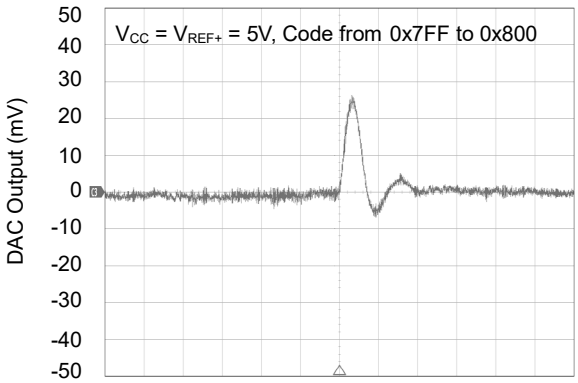
Zero Code Error vs. Temperature



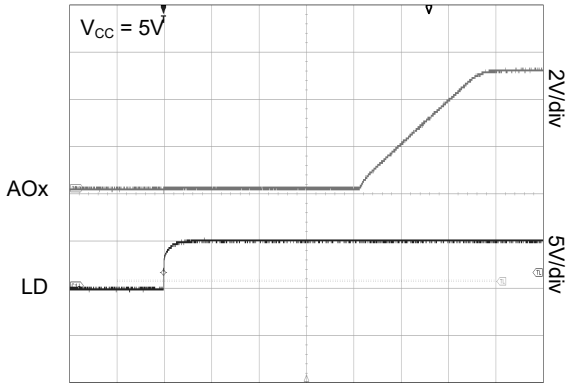
Full Scale Error vs. Temperature



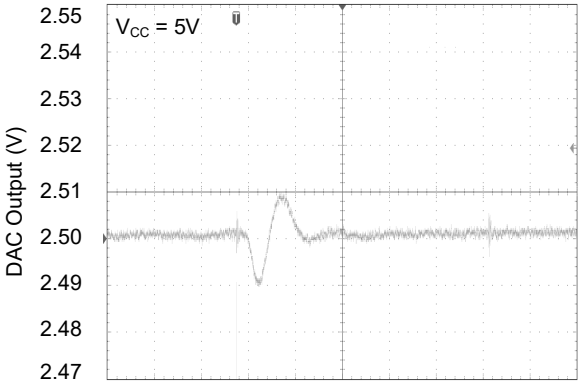
Glitch Response



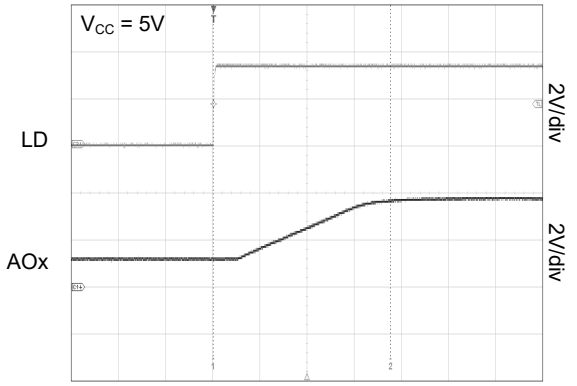
Wake-Up Time



DAC-to-DAC Crosstalk



Settling Time



FUNCTIONAL BLOCK DIAGRAM

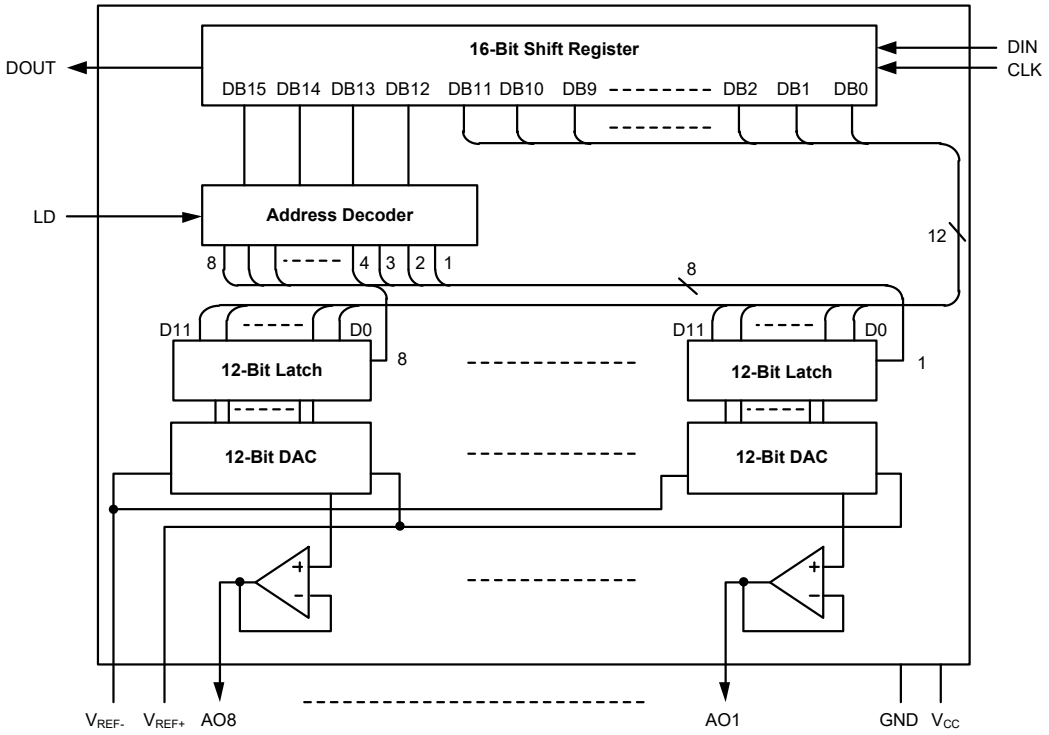


Figure 3. Block Diagram

TIMING CHART AT DATA SETTING

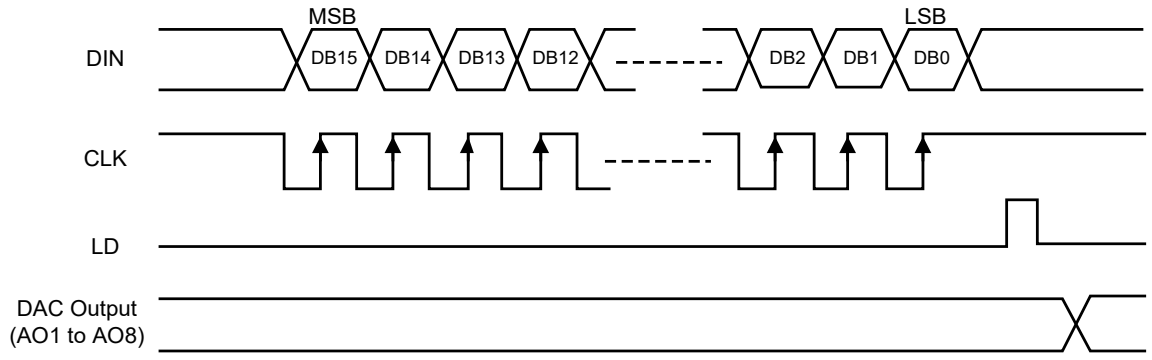


Figure 4. Timing Chart at Data Setting

DETAILED DESCRIPTION

DAC Architecture

The SGM5347-12 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings followed by an output buffer. The reference voltage is externally applied at V_{REF+} for DAC channels 1 through 8.

For simplicity, a single resistor string is shown in Figure 5. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage of:

$$V_{AOx} = D \times V_{LB} + V_{REF-} \quad (1)$$

$$V_{LB} = (V_{REF+} - V_{REF-})/4096 \quad (2)$$

where

D is the decimal equivalent of the binary code that is loaded into the DAC register.

D can take on any value between 0 and 4095. This configuration ensures that the DAC is monotonic.

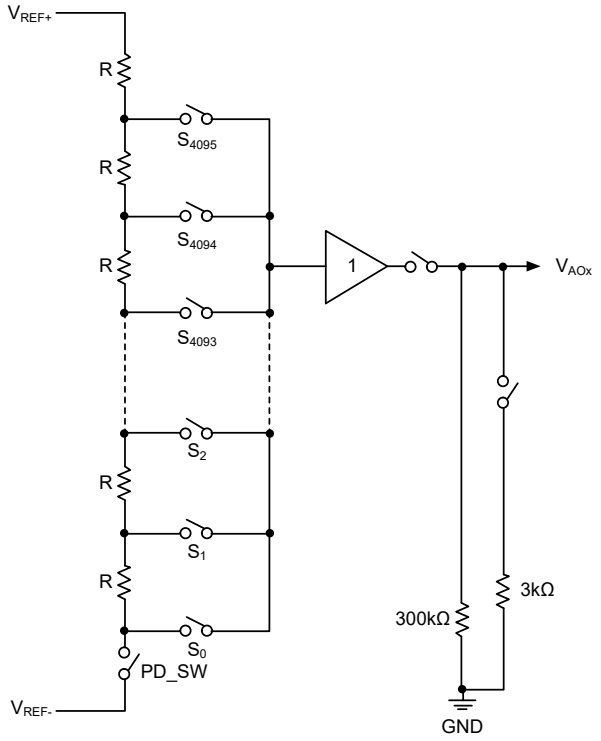


Figure 5. DAC Resistor String

Because all 8 DAC channels of the SGM5347-12 can be controlled independently, each channel consists of a DAC register and a 12-bit DAC. Figure 6 is a simple block diagram of an individual channel in the SGM5347-12. Depending on the mode of operation, data written into a DAC register causes the 12-bit DAC output to be updated, or an additional command is required to update the DAC output. Further description of the mode of operation can be found in CONTROL Register section.

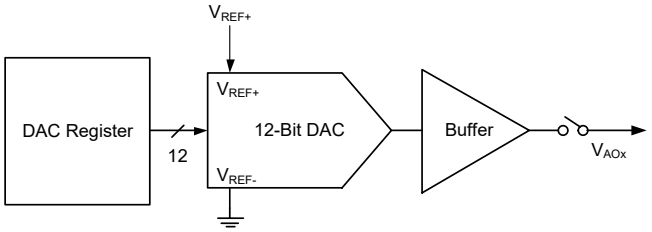


Figure 6. Single-Channel Block Diagram

DETAILED DESCRIPTION (continued)

Data for Shift Register

- SGM5347-12 has a 16-bit shift register for chip control.
- It is necessary to set the data as following configuration to a 16-bit shift register.
- The data consists of 16 bits: a 4-bit address selection and a 12-bit DAC control signal.

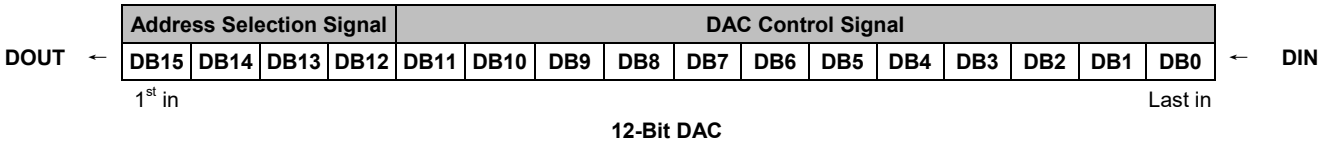


Figure 7. Serial Data

Address Selection Signal

Input Data Signal				Address Selected
DB15	DB14	DB13	DB12	
0	0	0	0	Don't care.
1	0	0	0	AO1 selected.
0	1	0	0	AO2 selected.
1	1	0	0	AO3 selected.
0	0	1	0	AO4 selected.
1	0	1	0	AO5 selected.
0	1	1	0	AO6 selected.
1	1	1	0	AO7 selected.
0	0	0	1	AO8 selected.
1	0	0	1	PWR_DWN.
0	1	0	1	CONTROL.
1	1	0	1	Don't care.
0	0	1	1	Don't care.
1	0	1	1	Don't care.
0	1	1	1	Don't care.
1	1	1	1	Don't care.

DAC Control Signal

Input Data Signal												DAC Output Voltage
DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	0	0	0	0	0	= V_{REF-}
0	0	0	0	0	0	0	0	0	0	0	1	= V_{LB} + V_{REF-}
0	0	0	0	0	0	0	0	0	0	1	0	= 2 × V_{LB} + V_{REF-}
~	~	~	~	~	~	~	~	~	~	~	~	~
1	1	1	1	1	1	1	1	1	1	1	0	= 4094 × V_{LB} + V_{REF-}
1	1	1	1	1	1	1	1	1	1	1	1	= 4095 × V_{LB} + V_{REF-}

NOTE: V_{LB} = (V_{REF+} - V_{REF-})/4096.

DETAILED DESCRIPTION (continued)

PWR_DWN Register

BIT	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Definition	PD_AO8	PD_AO7	PD_AO6	PD_AO5	PD_AO4	PD_AO3	PD_AO2	PD_AO1	N/A	N/A	N/A	N/A
Default	0	0	0	0	0	0	0	0	Don't care			

PWR_DWN register is not readable. Setting the bit to 1 powers down the corresponding DAC channel. Clearing the bit brings it up. If all the channels are powered down then the bias circuit will be powered down as well.

CONTROL Register

BIT	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Definition	N/A	N/A	N/A	N/A	RST	UPDATE	SYNC	3K_PULL	N/A	N/A	N/A	N/A
Default	X	X	X	X	X	0	0	0	Don't care			

RST = 1 Reset internal circuit other than the shift register. Will be automatically cleared to 0 after writing a 1. Since the reset doesn't hold, the next frame can be used for command. For example, at the first frame, the RST bit is written so that all DAC outputs reset to 0 at rising edge of the LD signal. The second frame can be a data writing command, but the DAC outputs won't be changed from 0 until writing of the data takes effect by the LD signal of the second frame.

3K_PULL = 1 Enable the 3kΩ pull-down resistors for all the 8 channels. The pull-down resistors are only enabled in power-down mode.

3K_PULL = 0 The pull-down resistance is around 300kΩ.

SYNC = 1 The rising edge of LD signal only loads the data in shift register to DIN register indicated by ADDR but does not update the data register. LD will update all 8 channels when writing to channel 8.

SYNC = 0 The rising edge of LD signal loads the data in shift register to DIN and DATA.

UPDATE = 1 The rising edge of LD signal updates data in DIN register of all 8 channels to the corresponding data registers. The bit is then automatically cleared to 0.

Example one of a simultaneous update:

1. Write 0x020 to CONTROL register.
2. Write data to channel 1, to channel 2 … to channel 7.
3. Writing data to channel 8 causes all the 8 channels to update at the same time. Then the following writings are still simultaneously updated.
4. Write 0x000 to CONTROL register to exit simultaneous update mode.

Example two of a simultaneous update:

1. Write 0x020 to CONTROL register.
2. Write data to channel 1, to channel 2 … to channel 7.
3. Write 0x060 to CONTROL register to update all the 8 channels. Then the following writings are still simultaneously updated.
4. Write 0x000 to CONTROL register to exit simultaneous update mode.

CHARACTERIZATION OF V_{AO} - I_{AO}

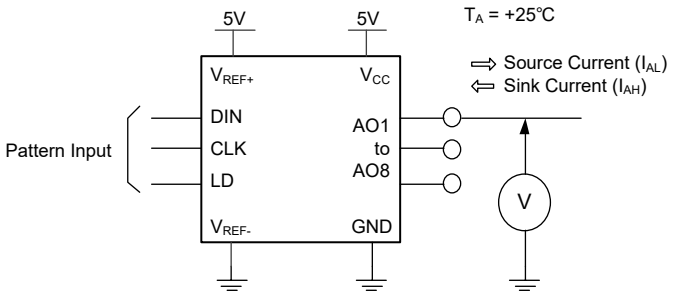


Figure 8. V_{AO} - I_{AO}

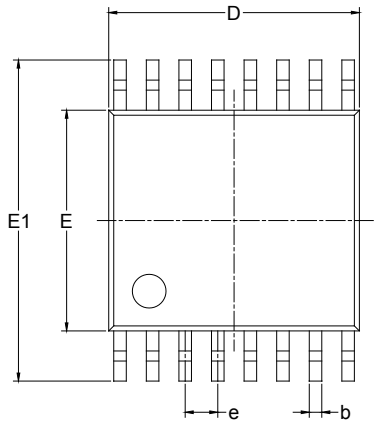
REVISION HISTORY

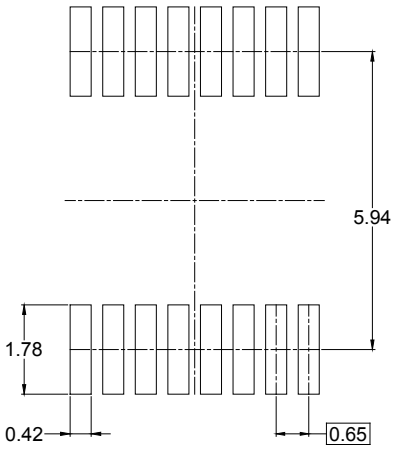
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2019) to REV.A	**Page**
Changed from product preview to production data	All

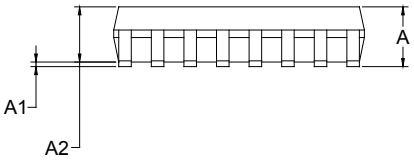
PACKAGE OUTLINE DIMENSIONS

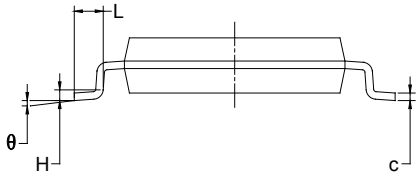
TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

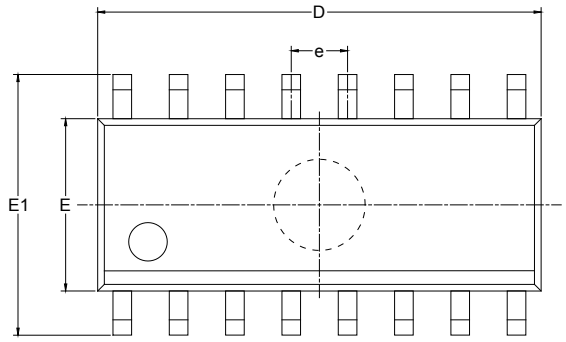


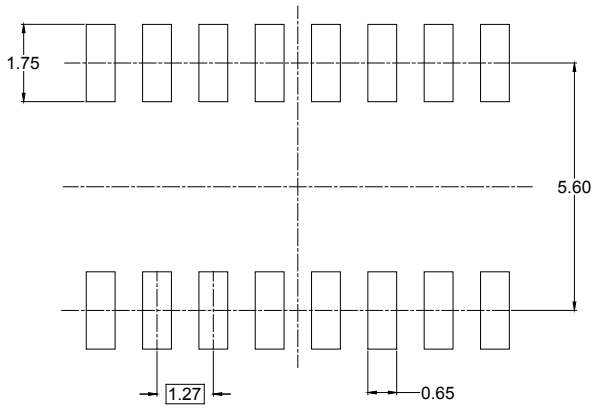


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

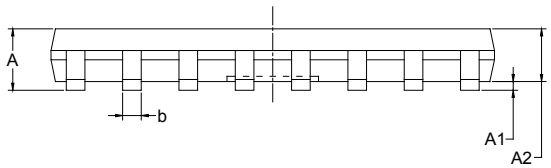
PACKAGE OUTLINE DIMENSIONS

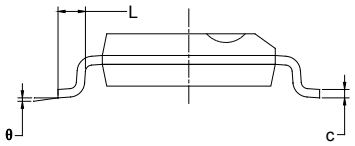
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)

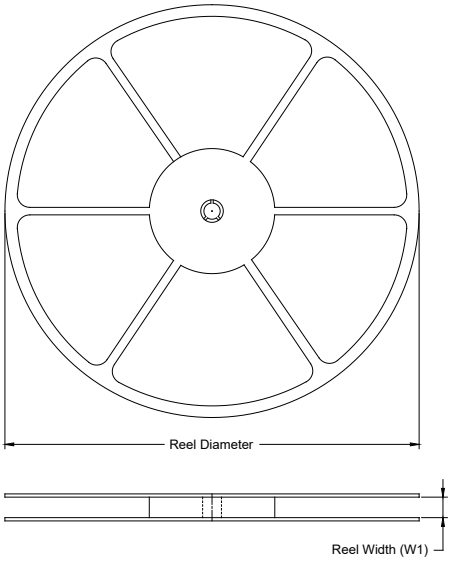




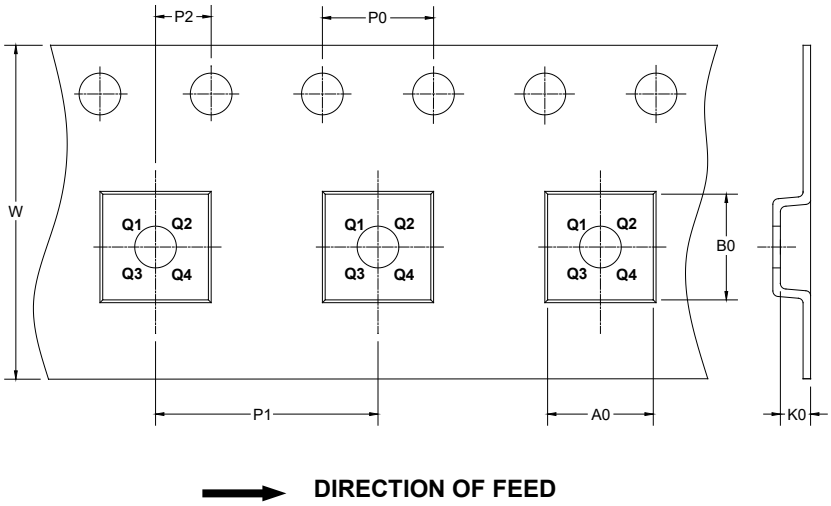
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



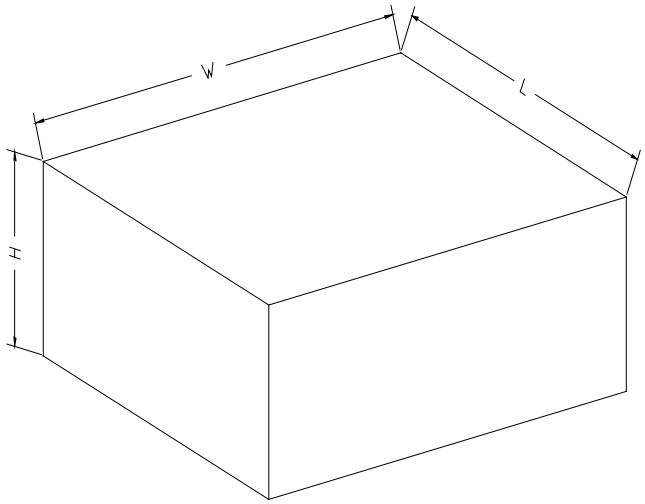
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1
SOIC-16	13″	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002