



# SGM48520

## 5V, 6A, 4A, Low-Side GaN and MOSFET Driver with 1ns Pulse Width

### GENERAL DESCRIPTION

The high-speed, single-channel low-side driver SGM48520 is designed to drive GaN FETs and logic level MOSFETs. Application areas include LiDAR, time of flight, facial recognition, and power converters using low-side drivers. The SGM48520 with TDFN package provides 6A source and 4A sink output current capability. Moreover, the output current capability of WLCSP package is better. Split output configuration allows individual turn-on and turn-off time optimization depending on FET. Package and pinout with minimum parasitic inductances reduce the rise and fall time and limit the ringing. Additionally, the 2ns propagation delay with minimized tolerances and variations allows efficient operation at high frequencies.

The driver has internal under-voltage lockout and over-temperature protection against overload and fault events.

The SGM48520 is available in Green WLCSP-0.88×1.28-6B and TDFN-2×2-6AL packages.

### FEATURES

- 5V Supply Voltage
- 6A Peak Source and 4A Peak Sink Currents
- Ultra-Fast, Low-side Gate Driver for GaN and Si FETs
- Minimum Input Pulse Width: 1ns
- Up to 60MHz Operation
- Propagation Delay: 2ns (TYP)
- Rise Time: 570ps (TYP)
- Fall Time: 610ps (TYP)
- Protection Features:
  - ◆ Under-Voltage Lockout (UVLO)
  - ◆ Over-Temperature Protection (OTP)
- Available in Green WLCSP-0.88×1.28-6B and TDFN-2×2-6AL Packages

### APPLICATIONS

Laser Distance Measuring System  
 5G RF Communication System  
 Wireless Charging System  
 GaN DC/DC Conversion System

### TYPICAL APPLICATION

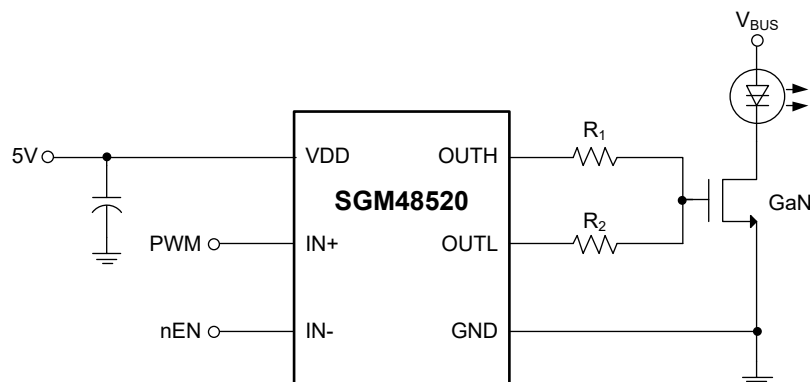


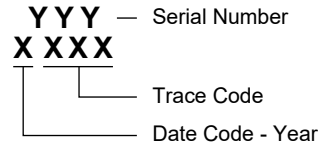
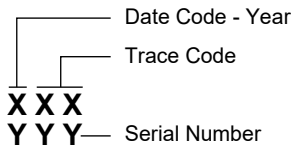
Figure 1. Typical Application Circuit

**PACKAGE/ORDERING INFORMATION**

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48520	WLCSP-0.88x1.28-6B	-40°C to +125°C	SGM48520XG/TR	XXX MBy	Tape and Reel, 3000
	TDFN-2x2-6AL	-40°C to +125°C	SGM48520XTDI6G/TR	G3M XXXX	Tape and Reel, 3000

**MARKING INFORMATION**

NOTE: XXX = Date Code and Trace Code. XXXX = Date Code and Trace Code.  
 WLCSP-0.88x1.28-6B TDFN-2x2-6AL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

**ABSOLUTE MAXIMUM RATINGS**

- Supply Voltage, V<sub>DD</sub>..... 5.75V
- IN+, IN- Pin Voltage, V<sub>INx</sub>..... -0.3V to 5.75V
- OUTH Pin Voltage, V<sub>OUTH</sub>..... -0.3V to V<sub>DD</sub> + 0.3V
- OUTL Pin Voltage, V<sub>OUTL</sub>..... -0.3V to 5.75V
- Junction Temperature..... +150°C
- Storage Temperature Range..... -65°C to +150°C
- Lead Temperature (Soldering, 10s)..... +260°C

**RECOMMENDED OPERATING CONDITIONS**

- Supply Voltage, V<sub>DD</sub>..... 4.75V to 5.25V
- IN+, IN- Pin Voltage, V<sub>INx</sub>..... 0V to 5.25V
- Operating Junction Temperature Range..... -40°C to +125°C

**OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

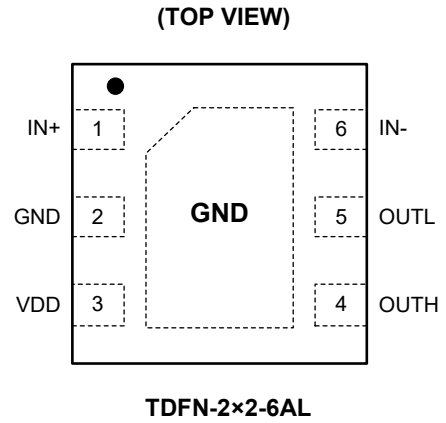
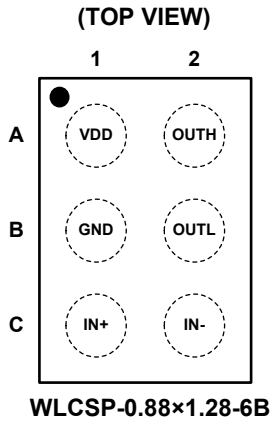
**ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

**DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
WLCSP-0.88x1.28-6B	TDFN-2x2-6AL			
A1	3	VDD	I	Input Voltage Supply. Bypass to GND with a low inductance ceramic capacitor.
A2	4	OUTH	O	Pull-Up Gate Drive Output. Connect it to the gate of the target transistor with an optional resistor.
B1	2	GND	—	Ground.
B2	5	OUTL	O	Pull-Down Gate Drive Output. Connect it to the gate of the target transistor with an optional resistor.
C1	1	IN+	I	Non-Inverting Logic Input.
C2	6	IN-	I	Inverting Logic Input.
—	Exposed Pad	GND	—	Exposed Pad. It is internally connected to GND through substrate. Connect this pad to large copper area, generally a ground plane.

NOTE: I: input, O: output.

FUNCTION TABLE

IN- Pin	IN+ Pin	OUTH Pin	OUTL Pin
L	L	Open	L
L	H	H	Open
H	L	Open	L
H	H	Open	L

**ELECTRICAL CHARACTERISTICS**(V<sub>DD</sub> = 5V, typical values are at T<sub>J</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC Characteristics</b>						
VDD Quiescent Current	I <sub>VDDQ</sub>	V <sub>IN+</sub> = V <sub>IN-</sub> = 0V		55		μA
VDD Operating Current	I <sub>VDD_OP</sub>	f <sub>SW</sub> = 30MHz, no load		34		mA
		f <sub>SW</sub> = 30MHz, 100pF load		47		
Under-Voltage Lockout	V <sub>DD_UVLO</sub>	VDD rising		4.15		V
UVLO Hysteresis	ΔV <sub>DD_UVLO</sub>			75		mV
Over-Temperature Shutdown, Rising Edge Threshold	T <sub>OTP</sub>			175		°C
Over-Temperature Hysteresis	ΔT <sub>OTP</sub>			26		°C
<b>Input DC Characteristics</b>						
IN+, IN- High Threshold	V <sub>IH</sub>			2.1		V
IN+, IN- Low Threshold	V <sub>IL</sub>			1.4		V
IN+, IN- Hysteresis	V <sub>HYS</sub>			0.7		V
Positive Input Pull-Down Resistance	R <sub>IN+</sub>	To GND		200		kΩ
Negative Input Pull-Up Resistance	R <sub>IN-</sub>	To VDD		200		kΩ
Input Pin Capacitance	C <sub>IN</sub>	To GND		5		pF
<b>Output DC Characteristics</b>						
OUTL Voltage	V <sub>OL</sub>	I <sub>OUTL</sub> = 100mA, V <sub>IN+</sub> = V <sub>IN-</sub> = 0V		28		mV
OUTH Voltage	V <sub>DD</sub> - V <sub>OH</sub>	I <sub>OUTH</sub> = 100mA, V <sub>IN+</sub> = 5V, V <sub>IN-</sub> = 0V		27		mV
Peak Source Current <sup>(1)</sup>	I <sub>OH</sub>	V <sub>OUTH</sub> = 0V, V <sub>IN+</sub> = 5V, V <sub>IN-</sub> = 0V		6		A
Peak Sink Current <sup>(1)</sup>	I <sub>OL</sub>	V <sub>OUTL</sub> = 5V, V <sub>IN+</sub> = V <sub>IN-</sub> = 0V		4		A

NOTE:

1. The output current is only for TDFN package. The performance of WLCSP package is better and the data will be supplemented after completing the test.

**SWITCHING CHARACTERISTICS**(V<sub>DD</sub> = 5V, typical values are at T<sub>J</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Startup Time, V <sub>DD</sub> Rising above UVLO	t <sub>START</sub>	IN- = GND, IN+ = VDD, V <sub>DD</sub> rising to 4.4V to OUTH rising		50		μs
ULVO Falling	t <sub>SHUTOFF</sub>	IN- = GND, IN+ = VDD, V <sub>DD</sub> falling below 3.9V to OUTH falling		2.5		μs
Turn-on Propagation Delay	t <sub>PDR</sub>	V <sub>IN-</sub> = 0V, IN+ to OUTH, 100pF load		1.9		ns
Turn-off Propagation Delay	t <sub>PDF</sub>	V <sub>IN-</sub> = 0V, IN+ to OUTL, 100pF load		2.2		ns
Pulse Positive Distortion (t <sub>PDF</sub> - t <sub>PDR</sub> )	Δt <sub>PD</sub>			300		ps
Output Rise Time	t <sub>RISE</sub>	0Ω series 100pF load <sup>(2)</sup>		570		ps
Output Fall Time	t <sub>FALL</sub>	0Ω series 100pF load <sup>(2)</sup>		610		ps
Minimum Input Pulse Width	t <sub>MIN</sub>	0Ω series 100pF load <sup>(2)</sup>		1		ns

NOTE:

2. Rise and fall are calculated as a 20% to 80%.

FUNCTIONAL BLOCK DIAGRAM

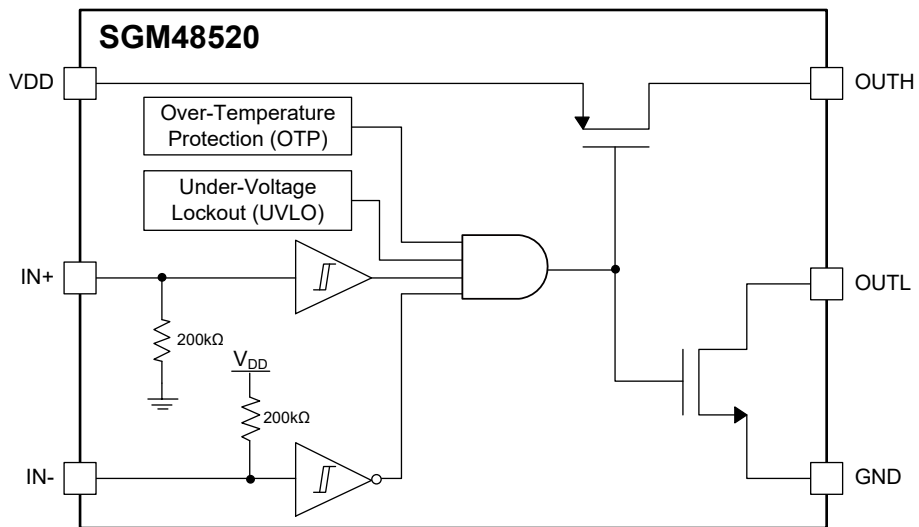


Figure 2. Functional Block Diagram

## DETAILED DESCRIPTION

The high-speed, single-channel low-side driver SGM48520 is designed to drive GaN FETs and logic level MOSFETs. Application areas include LiDAR, time of flight, facial recognition, and power converters using low-side drivers.

SGM48520 provides the lowest propagation delay of 2ns from the driver to the power transistor. SGM48520 adopts small WLCSP package with very small parasitic inductance. This package reduces ringing and increases current drive capability in high frequency applications when driving power transistors.

### Input Stage

There are two Schmitt triggers at the input pins IN+ and IN- to improve noise immunity. In order to prevent the output from accidentally turning on when the input is in the floating state, IN+ is internally connected to a pull-down resistor, and IN- is internally connected to a pull-up resistor. The output signal depends on the logic voltage levels on the IN+ and IN- pins (which are not a differential input pair).

### Output Stage

SGM48520 provides 6A peak source and 4A sink currents, and the outputs are separated to allow custom pull-up and pull-down drive strength to suit the application. OUTH and OUTL pins can each be connected to transistor gates using separate drive resistors, adjusting the driving speed of turning on and off to control the slew rate and EMI of the driving signal and the ringing on the gate signal. Controlling ringing

as much as possible reduces the stress on the driver and switch device, which is very important for high-performance applications and reliability of GaN FETs. In order to prevent the device  $C_{ISS}$  from turning the FET on by mistake, the OUTL pin will be pulled low in under-voltage conditions.

### VDD and Under-Voltage Lockout

The rated working voltage of SGM48520 is  $5V \pm 0.25V$ , and the maximum power supply voltage of the part is 5.75V. In the application, the error of the power supply of the driver chip needs to be ensured within 0.25V, and the transient overshoot voltage of the power supply cannot exceed the maximum voltage of the part. In the VDD Overshoot Solution section, there are more detailed design details.

SGM48520 provides under-voltage lockout (UVLO) function to protect the circuit in the event of a fault condition. The UVLO trigger point is set at 4.15V, and the hysteresis voltage is 76mV. This UVLO level ensures that the GaN FET operates in the low  $R_{DS(ON)}$  region. When UVLO is triggered, the output is low.

### Over-Temperature Protection (OTP)

The SGM48520 provides an over-temperature protection (OTP) function with a trigger point of  $+175^{\circ}C$ . The hysteresis temperature is  $26^{\circ}C$ . If the OTP is triggered, switching action is stopped with OUTL held low. Then when the junction temperature of the device falls below  $+149^{\circ}C$ , normal operation resumes.

## APPLICATION INFORMATION

Since the output of the PWM controller often cannot provide the voltage required by the gate of the power device, a high-performance gate driver is usually required between the PWM output of the controller and the gate of the GaN transistor, so that the GaN transistor can operate at correct gate voltages. In addition, the gate driver can reduce switching losses and maximize the performance of GaN transistors in high-frequency applications. Especially in the field of digital power control, it is common for the PWM signal of the digital controller to be a 3.3V logic signal, and GaN transistors cannot work optimally with this gate voltage. The gate driver boosts the 3.3V signal to the preferred gate drive voltage of 5V, which fully turns on the power device and minimizes conduction losses.

The good noise immunity of the SGM48520 gate driver also minimizes the effects of high frequency switching noise when the driver is placed near the power switch. Adding a gate driver also transfers the gate charge power loss from the controller to the driver, effectively reducing the power consumption and thermal stress in the controller.

SGM48520 is a low-side high-speed gate driver with a maximum operating frequency of 60MHz and an operating voltage of 5V. It is optimized to drive GaN FETs. The output has an independent configuration architecture, which can flexibly adjust the turn-on and turn-off speed, while providing a strong current sinking and sourcing capabilities.

The SGM48520 is primarily used to drive GaN transistors, which are used in various power converters, LiDAR, wireless chargers, and synchronous rectifiers. The SGM48520 can be used as a driver for high-speed pulsed laser diodes.

### Typical Application

A typical application circuit for the SGM48520 is shown in Figure 1, a single-channel, 5V drive voltage, specifically designed to drive GaN transistors or logic-level Si FETs. The output has a separated structure, so that the turn-on and turn-off speeds can be controlled separately by driving resistors. If it is not

necessary to adjust the turn-on and turn-off speeds separately, OUTH and OUTL may be connected directly together (with a single gate drive resistor added if necessary).

In order to avoid voltage overstress caused by the parasitic inductance of the drive circuit, SGMICRO recommends the use of at least 2Ω resistors at OUTH and OUTL.

For applications requiring a smaller resistance value, please contact SGMICRO E2E for guidance.

### Design Requirements

There are some key factors to consider when designing with the SGM48520 gate driver and GaN power FETs, especially for high MHz frequency (or nanosecond pulse) applications. These factors include circuit layout, PCB trace design, passive component selection, and maximum operating frequency.

### Detailed Design Procedure

#### Handling Ground Bounce

Place the ground pin of the SGM48520 as close as possible to the source of the low-side FET to get the smallest gate current loop, the smallest parasitic inductance, and maximize the switching performance. However, this can cause ground bounce on the SGM48520, resulting in incorrect switching logic at the input and wrong level at the output.

In order to eliminate this effect, SGM48520 has built-in Schmitt triggers on the input terminals to increase the input hysteresis. Equation 1 shows the relationship between the input hysteresis and the maximum allowable di/dt:

$$\frac{di}{dt} = \frac{V_{HYS}}{L_p} \quad (1)$$

where

$L_p$ : Parasitic inductance between source and Ground.

$V_{HYS}$ : Hysteresis voltage of the input port.

$di/dt$ : Current slew rate.

APPLICATION INFORMATION (continued)

Assuming that the parasitic inductance is 0.7nH and the hysteresis voltage is 0.7V, the maximum allowable current slew rate is 1A/ns by calculation. If the current slew rate generated in the application is higher than 1A/ns, this exceeds the hysteresis voltage range and causes the output signal to be unstable. Using the inverting input to accept the PWM signal and connecting the non-inverting input to VDD reduce the possibility of false pulses or oscillations and improve stability. High di/dt produces high transient voltage spikes that affect the input of the SGM48520. In order to protect the device from a large current spike at IN-, a 100Ω current limiting resistor can be placed before the IN- input.

If the current slew rate is not too high, and the pulse width is not very short (for example, 1ns range), the extra delay can be accepted. The parasitic capacitance of the SGM48520 input can be used to good advantage to create an RC filter to reduce high-frequency noise by adding a resistor in series with the input pin. The SGM48520 has stable input capacitance of about 5pF at the input pins, which is convenient for this purpose.

If the environment is more severe, using a common mode choke coil can increase the stability of the system.

In applications that use current sensing resistors, the ground bounce phenomenon is particularly serious. In

the application circuit with current sense resistor shown in Figure 3, the ground of the SGM48520 is connected to the source of the GaN FET, and one side of the current sense resistor is connected to the controller ground. In the case of high-speed switching and large current, the potential rebound due to the parasitic inductance of the current detection resistor will cause the circuit to turn on/off by mistake, and in severe cases may cause damage to the device. Figure 5 shows the solution for this situation: Use a common mode choke between the controller output and the SGM48520 input. When the pulse width is not extremely narrow, a resistor can also be added to the signal output line before SGM48520 to form an RC filter as a supplement. Although the circuit of Figure 4 improves the ground bounce problem by connecting the GND of the driver to the signal ground after the current sense resistor, this circuit is not recommended. The drawback of this circuit is that the voltage drop across the current sense resistor and its parasitic inductance reduce the transient and DC gate drive voltage to the FET, reducing efficiency. In severe cases, the voltage ringing caused by the inductance of the sense resistor path can even cause the FET to spuriously turn on and off. For these reasons, the circuit of Figure 5 is the preferred solution to ground bounce problems.

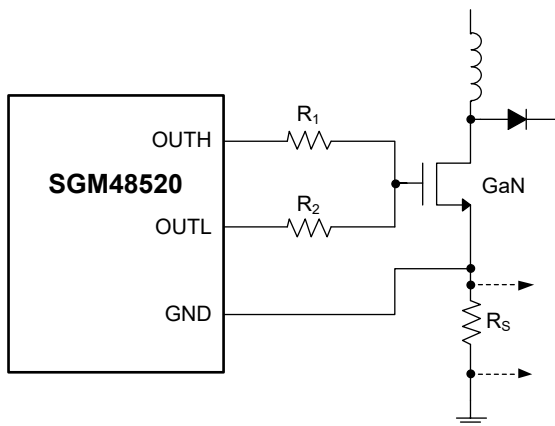


Figure 3. Rs Current Sense A Configuration

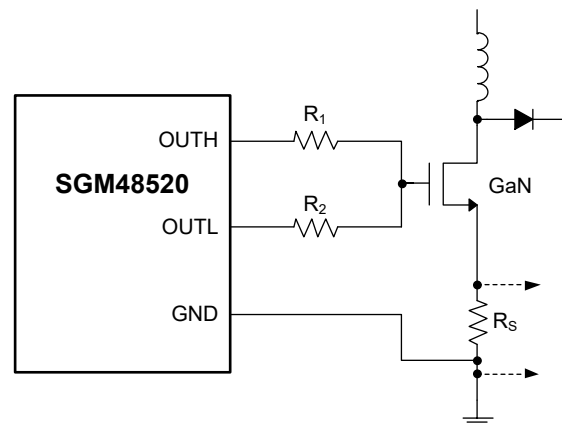


Figure 4. Rs Current Sense B Configuration



APPLICATION INFORMATION (continued)

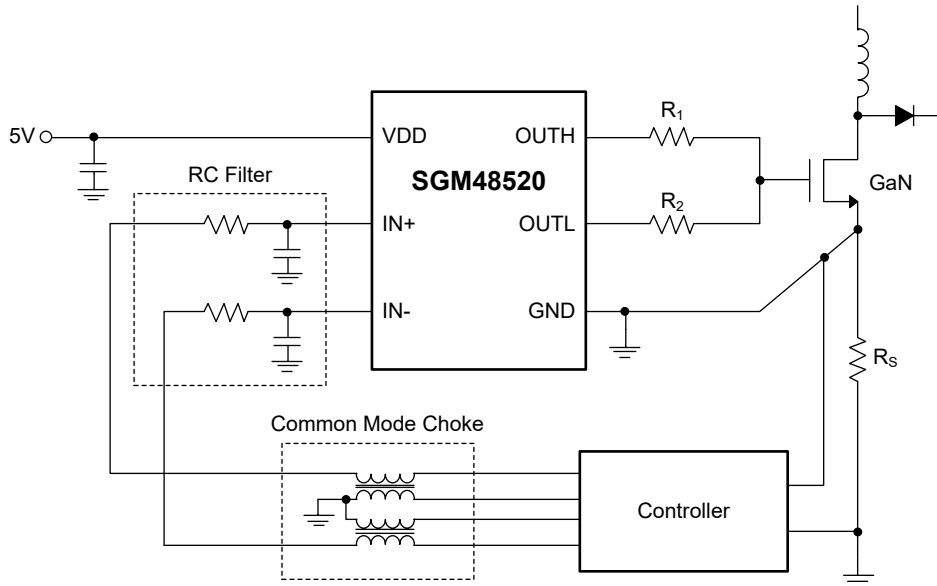


Figure 5. Filtering For Ground Bounce Noise Handling with SGM48520

Creating Nanosecond Pulse with SGM48520

SGM48520 can provide a minimum 1ns pulse width output to capacitive load. However, outputting such a small equivalent pulse width requires a very powerful digital driver and also needs to consider the influence of parasitic parameters from the digital output to the SGM48520 input. Using the two inputs of SGM48520 and the AND gate can get a method of generating short pulses at the output. As shown in Figure 6, connect one digital signal to IN+, and the other delayed digital signal

to IN-, so that a narrow pulse will appear at the output, the width of which is equal to the delay time of the two digital signals. The digital controller only needs to control the delay time in the range of nanoseconds, which reduces the requirement for the SGM48520 input signal. If the digital signal has only one output, an RC low-pass filter can be used to generate a signal with an adjustable delay time, which is related to the RC time constant.

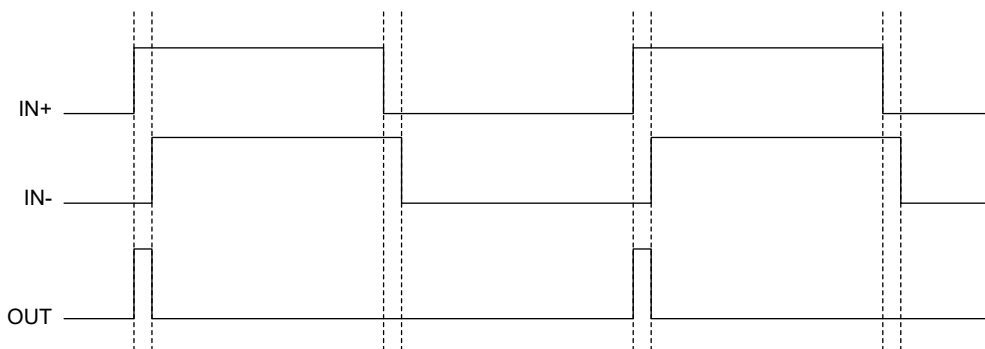


Figure 6. Timing Diagram of Creating Short Pulses

## APPLICATION INFORMATION (continued)

### VDD Overshoot Solution

Due to the existence of PCB parasitic inductance, inductance ringing and transient overshoot voltage are prone to occur under high current switching conditions. In the PCB design process, it is necessary to evaluate and control the overshoot caused by the ringing, so as not to exceed the stress of the device. The strength of the overshoot voltage and the percentage of the overshoot duration to the switching time are parameters that affect the stress. Keeping the overshoot below maximum allowable pin voltage is the best solution. The parasitic inductance can be decreased by optimizing PCB layout. To limit the voltage overshoot, low ESL components and series resistance can be helpful as well. If the overshoot is too large, the accuracy of the power supply needs to be considered. For example, if the overshoot voltage is 0.5V, the maximum error voltage of the power supply cannot exceed 5.25V (5% accuracy). Therefore, if the overshoot voltage is large, a power supply with higher accuracy is necessary.

### Applications at High Frequencies

SGM48520 has a rise/fall time of 570ps/610ps, and provides a minimum output capability of 1ns pulse width and a maximum operating frequency of 60MHz. According to the capacitive load, different output modes and frequencies can be selected. Under the working condition of high-frequency pulse, in order to prevent the device from overheating, a high-frequency pulse train with a certain interval time can be used. This can increase the transient frequency and keep the effective value of the output current unchanged. At this time, a larger decoupling capacitor is needed to charge the capacitive load at a high frequency.

### Power Supply Recommendations

In order to provide high peak current when the FET is turned on and improve the stability of the VDD pin supply voltage, a low ESR/ESL ceramic capacitor needs to be used as a bypass capacitor placed as close as possible to the IC's VDD and GND pins. To avoid ringing at the IC pins as much as possible, the decoupling capacitors need to be placed on the same side as the IC, and vias cannot be used.

In order to achieve the best transient performance, SGMICRO recommends choosing a three-terminal capacitor and a capacitor with a larger capacitance in parallel. The three-terminal capacitor needs to be placed close to the VDD and GND pins of the IC, and the other capacitor is placed close to the three-terminal capacitor. The three-terminal capacitor has the lowest ESL, and the larger capacitor provides enough drive peak current. Under normal circumstances, it is recommended to use 0.1 $\mu$ F 0402 or through-core capacitors in parallel with 1 $\mu$ F 0603 capacitors.

### Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. SGM48520 provides WLCSP ball grid array package, which can reduce the parasitic inductance in the connection line with BGA type GaN FET.

In order to achieve the best performance, a PCB with at least four routing layers is recommended to minimize the parasitic inductance. Using resistors and capacitors in a smaller package (0201) can also minimize inductance and PCB space. It is necessary to calculate the resistor power of a small package to meet the requirements of gate drive power loss.

### Drive Loop Inductance and Grounding

SGM48520 should be placed as close to the GaN FET as possible, and the trace of the gate drive circuit should be as wide as possible to reduce parasitic inductance.

To achieve minimum drive loop inductance, it is recommended to use the second layer of the PCB as the source loop of the GaN FET, near the bottom of the device (top layer). Both the vias connected to the GND pin and the source of the FET are connected to this layer with minimal impedance. Please note that only when the GND plane is connected to the source power plane at the FET will the coupling of the ground plane be decreased.

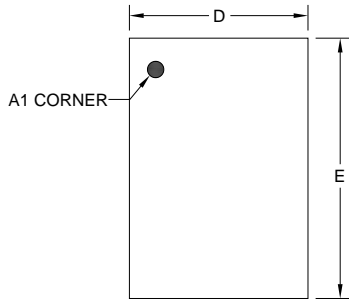
**APPLICATION INFORMATION (continued)****Bypass Capacitor**

The VDD pin requires a bypass capacitor connected to GND, placed as close to the pins of the SGM48520 as physically possible. The capacitor should be connected to VDD and GND power planes, which should be large and as close to the top layer of the PCB as possible. Due to the high operating frequency of the IC, the inductance of the bypass capacitor is critical, so the value of the bypass capacitor should be between 0.1 $\mu$ F

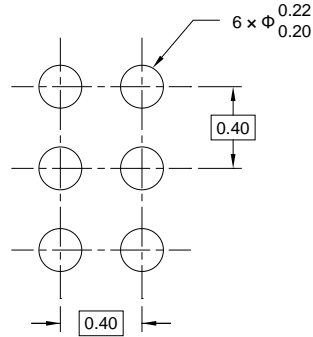
and 1 $\mu$ F, and the material should be X7R or better. The best capacitors for the application are low inductance chip capacitors (LICC), interdigital capacitors (IDC), feedthrough and LGA capacitors. Finally, in order to meet the demand of driving peak current, an extra 1 $\mu$ F capacitor between VDD and GND should be added in parallel close to the IC.

PACKAGE OUTLINE DIMENSIONS

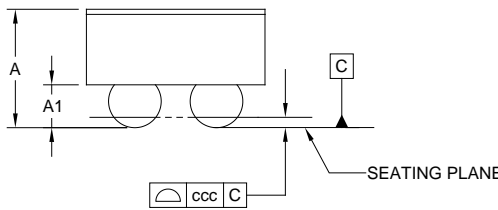
WLCSP-0.88x1.28-6B



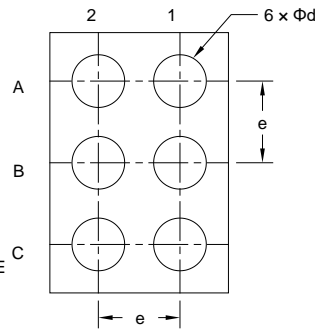
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



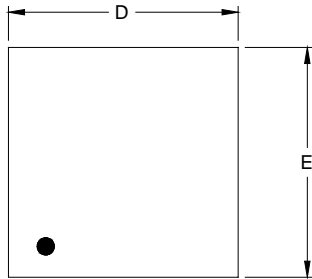
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.535	0.580	0.625
A1	0.190	0.210	0.230
D	0.845	0.875	0.905
E	1.245	1.275	1.305
d	0.238	0.258	0.278
e	0.400 BSC		
ccc	0.050		

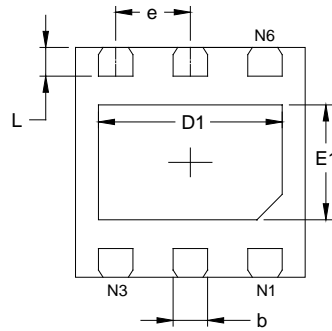
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

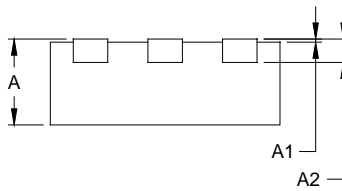
TDFN-2x2-6AL



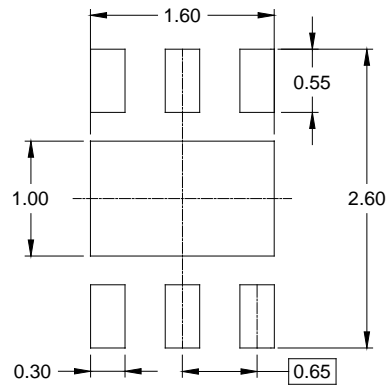
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

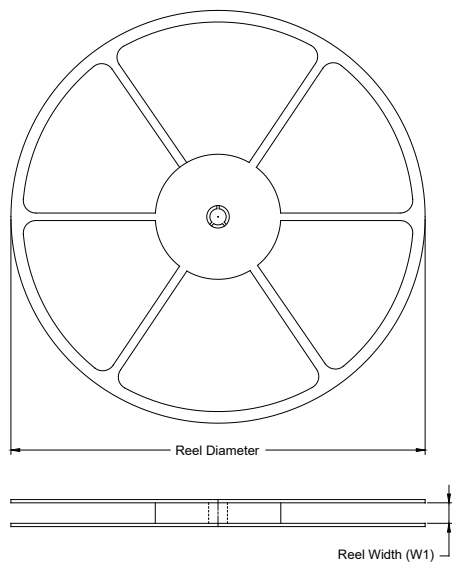
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.500	1.700	0.059	0.067
E	1.900	2.100	0.075	0.083
E1	0.900	1.100	0.035	0.043
b	0.250	0.350	0.010	0.014
e	0.650 BSC		0.026 BSC	
L	0.174	0.326	0.007	0.013

NOTE: This drawing is subject to change without notice.

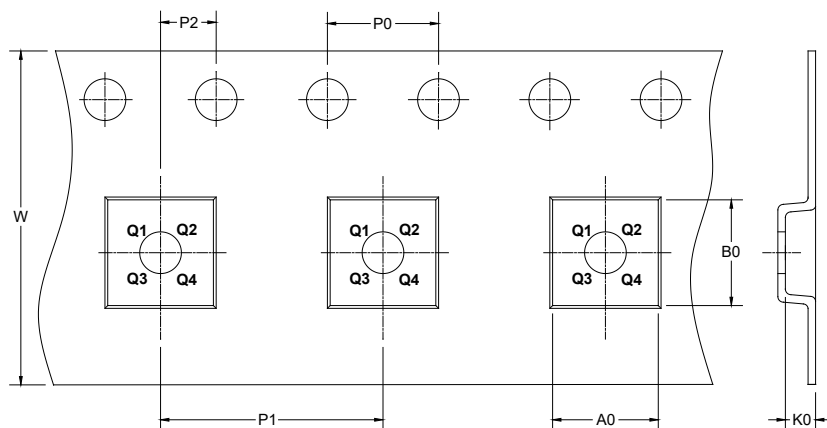
# PACKAGE INFORMATION

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



➔ DIRECTION OF FEED

NOTE: The picture is only for reference. Please make the object as the standard.

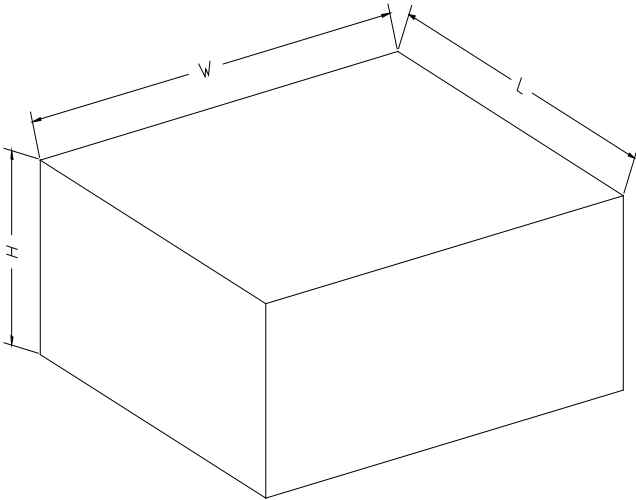
### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.88×1.28-6B	7"	9.5	0.99	1.38	0.69	4.0	4.0	2.0	8.0	Q1
TDFN-2×2-6AL	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

D00001

# PACKAGE INFORMATION

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002