



SGM40666A/SGM40666B High-Current Over-Voltage Protector

GENERAL DESCRIPTION

The SGM40666A and SGM40666B are over-voltage protection devices designed to protect low voltage systems from damage with a high voltage supply up to +31V_{DC} and +40V_{PEAK} (10s with 50mA current limit). The SGM40666A withstands +90V/-400V while SGM40666B can also withstand surges up to +80V/-400V without damage.

The integrated 28mΩ (TYP) R_{ON} FET allows it to pass through 4.5A continuous current. The FET is turned off when the input voltage exceeds the over-voltage threshold which can be adjusted between 4V and 22V with optional external resistors.

When the OVLO input is set below the external OVLO select threshold (0.27V TYP), the SGM40666A and SGM40666B automatically choose the internal trip thresholds that are preset to 6.83V typically. SGMICRO provides customized OVP threshold options for 22.2V/15.3V/10.5V/6.35V/5.95V. Please contact us if necessary.

The open-drain nACOK output indicates a stable power supply between minimum supply voltage and V_{OVLO}.

The SGM40666A and SGM40666B are available in a Green WLCSP-1.17×1.63-12B package.

FEATURES

- 2.5V to 28V Operating Input Voltage Protection
- Input Voltage up to 40V with 50mA Current Limit for 10s Duration
- Integrated 28mΩ (TYP) N-Channel MOSFET
- Adjustable Over-Voltage Protection Trip Level
- 4V to 22V Adjustable OVLO Threshold Range
- 6.83V (TYP) Internal Preset OVLO Threshold
- SGM40666A: Up to +90V/-400V Surge Immunity
- SGM40666B: Up to +80V/-400V Surge Immunity
- 32.3V Clamping Circuit Trigger Threshold when Rising Slope > 4.5V/μs (SGM40666A)
- 45V Clamping Circuit Trigger Threshold (SGM40666B)
- 50ns (TYP) Over-Voltage Shutdown Response
- Soft-Start Function
- 15ms Start-up Debounce Time
- Thermal Shutdown Protection
- Enable Function
- Power Good Flag
- Available in a Green WLCSP-1.17×1.63-12B Package

APPLICATIONS

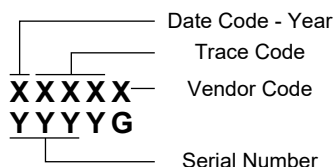
Smart Phones
Tablet PCs
Battery Charging Ports

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM40666A	WLCSP-1.17×1.63-12B	-40°C to +85°C	SGM40666AYG/TR	XXXXX RDFYG	Tape and Reel, 3000
SGM40666B	WLCSP-1.17×1.63-12B	-40°C to +85°C	SGM40666BYG/TR	XXXXX RE0YG	Tape and Reel, 3000

MARKING INFORMATION

XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

- IN-0.3V to 31V ⁽¹⁾
- IN (Peak for 10s Duration, 50mA Limit)-0.3V to 40V ⁽¹⁾
- OUT-0.3V to V_{IN} + 0.3V
- OVLO -0.3V to 26.4V
- nACOK, nEN -0.3V to 6V
- Continuous IN, OUT Current 4.5A ⁽²⁾
- Peak IN, OUT Current (10ms) 8A

Package Thermal Resistance

- WLCSP-1.17×1.63-12B, θ_{JA} 103°C/W
- Junction Temperature +150°C
- Storage Temperature Range -65°C to +150°C
- Lead Temperature (Soldering, 10s) +260°C

ESD Susceptibility

- HBM 4kV
- CDM 1kV
- Air Gap Discharge on IN Pin (IEC61000-4-2) 20kV
- Contact Discharge on IN Pin (IEC61000-4-2) 12kV

RECOMMENDED OPERATING CONDITIONS

- Supply Voltage Range 2.5V to 28V ⁽³⁾
- Operating Junction Temperature Range -40°C to +125°C

NOTES:

1. Non-frequent repeat peak voltage during input surge transient and ESD transient is not subject to this rating value, which may go higher than 40V during the surge test.
2. Continuous current limit may vary with the circuit board thermal dissipation condition.
3. If protection discharging triggered, the discharging keeps until the supply falls below the hysteresis range. Continuously force driving during discharging with a voltage in the hysteresis range would cause overstress or even damage the device. Supply voltage within the hysteresis range is not recommended.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

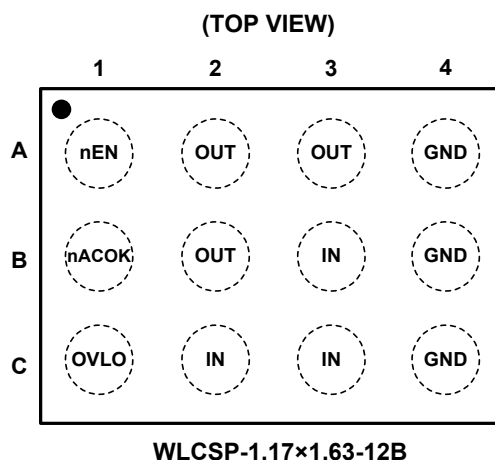
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

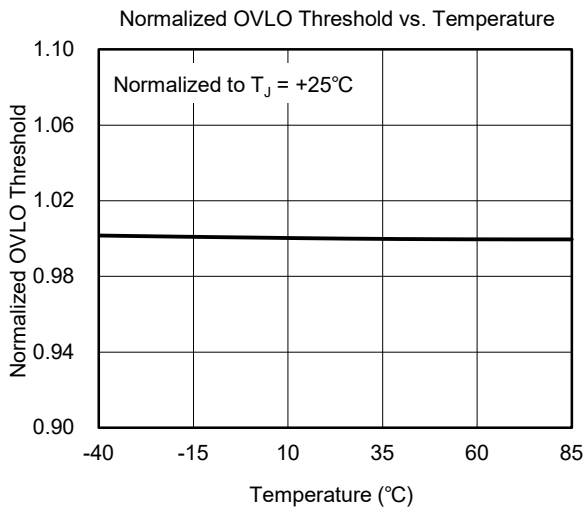
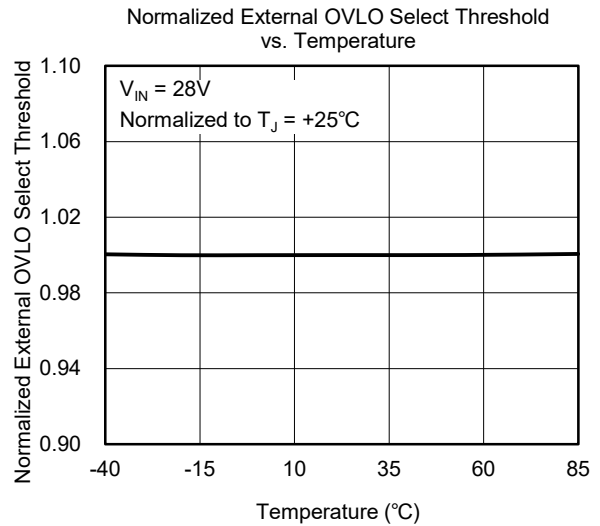
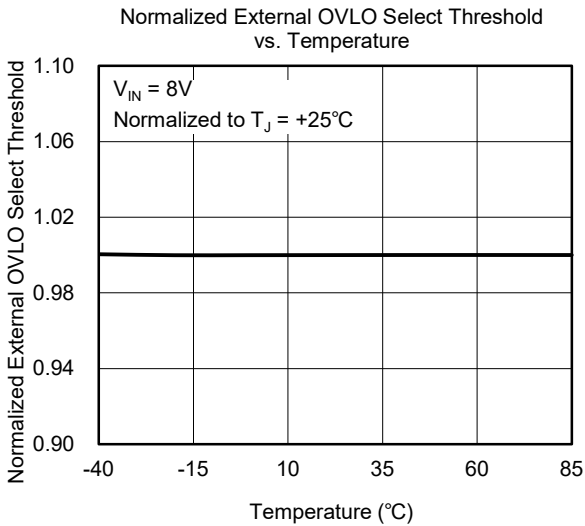
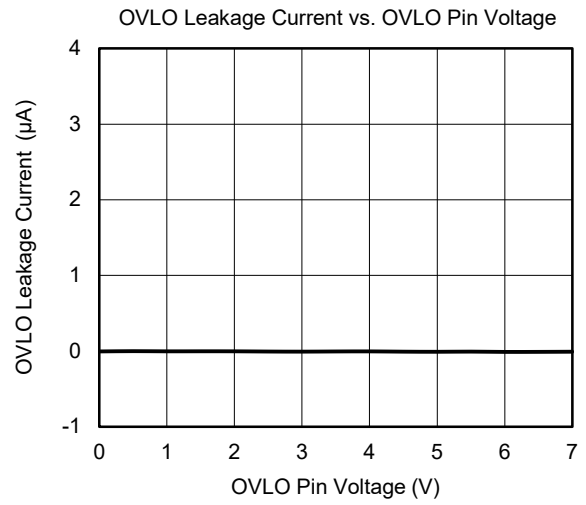
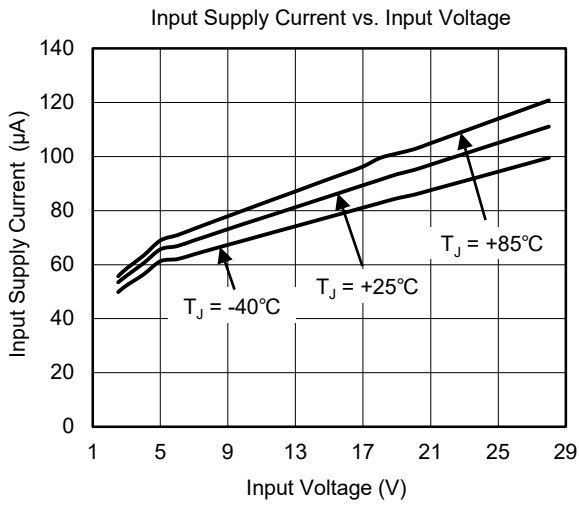
PIN	NAME	FUNCTION
A1	nEN	Device Enable Pin. Active low to enable the IN to OUT pass path.
A2, A3, B2	OUT	Output Pin. Output of internal switch.
A4, B4, C4	GND	Ground.
B1	nACOK	Open-Drain Flag Output for Power Good. When the input voltage is stable between the minimum V_{IN} and V_{OVLO} , nACOK is driven low. nACOK is high impedance if thermal shutdown occurs.
B3, C2, C3	IN	Input and Device Supply Pin. Place a 0.1 μ F ceramic capacitor as close as possible to the device.
C1	OVLO	Over-Voltage Protection Threshold Adjustment. Connect OVLO to GND when using the internal threshold. Connect to a resistor divider network to adjust the OVLO threshold.

ELECTRICAL CHARACTERISTICS

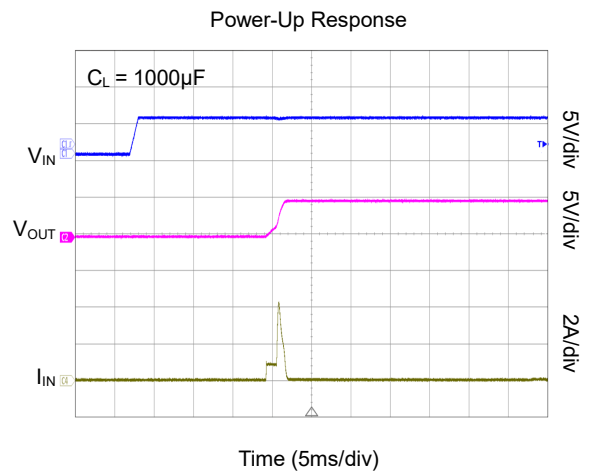
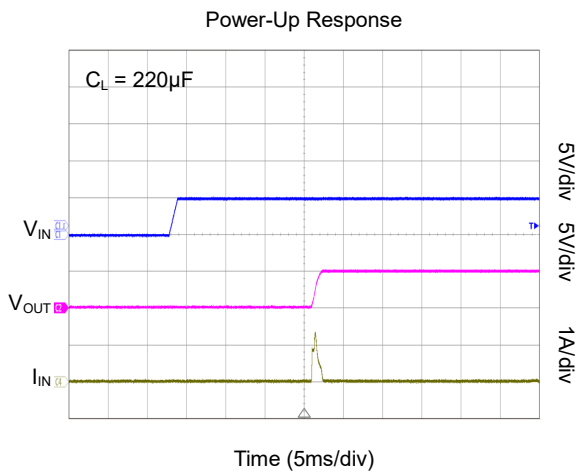
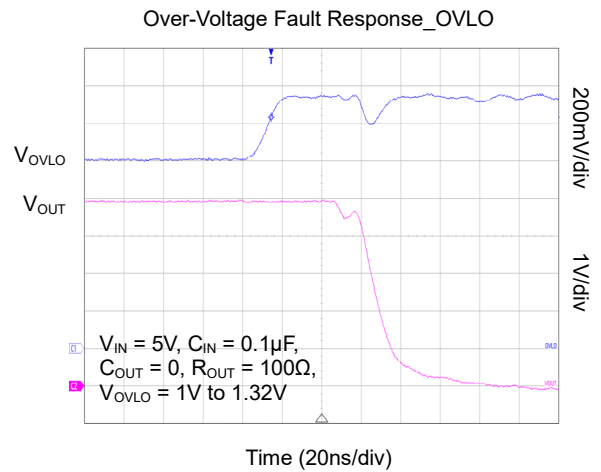
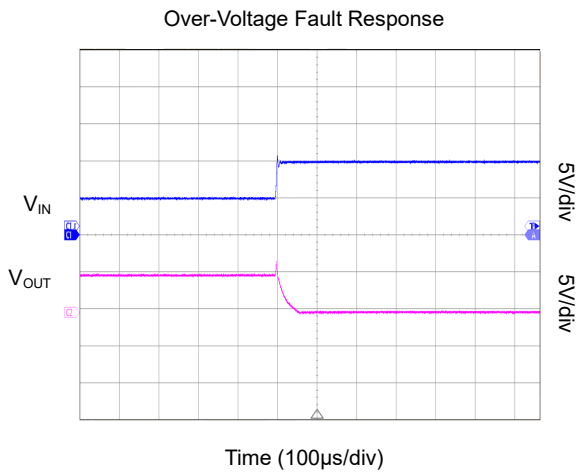
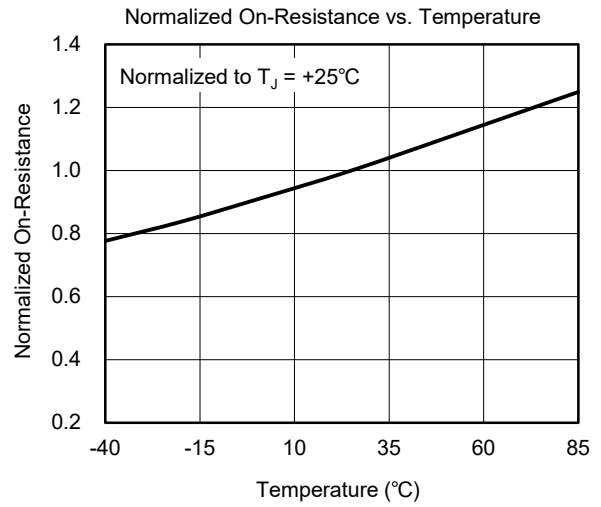
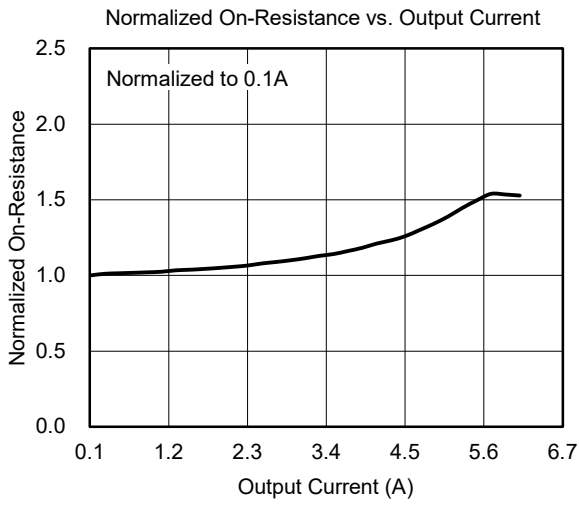
($V_{IN} = 2.5V$ to $28V$, $C_{IN} = 0.1\mu F$, $T_J = -40^\circ C$ to $+85^\circ C$, typical values are at $V_{IN} = 5V$, $I_{IN} \leq 3A$, $T_J = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		2.5		28	V
Input Supply Current	I_{IN}	$V_{IN} = 5V$		62	90	μA
OVLO Supply Current	I_{IN_Q}	$V_{OVLO} = 3V$, $V_{IN} = 5V$, $V_{OUT} = 0V$		65	95	μA
Internal Over-Voltage Trip Level	V_{IN_OVLO}	V_{IN} rising	6.69	6.83	6.97	V
		V_{IN} falling	6.61	6.76		
V_{BG} Reference	V_{BG}		1.163	1.190	1.215	V
Adjustable OVLO Threshold Range			4		22	V
External OVLO Select Threshold	V_{OVLO_SELECT}		0.24	0.27	0.29	V
Switch On-Resistance	R_{ON}	$V_{IN} = 5V$, $I_{OUT} = 0.5A$, $T_J = +25^\circ C$		28	39	m Ω
OUT Load Capacitance	C_{OUT}	$V_{IN} = 5V$, $T_J = +25^\circ C$			1000	μF
OVLO Parasitic Capacitance	C_{P_OVLO}	$T_J = +25^\circ C$		3		pF
OVLO Input Leakage Current	I_{OVLO}	$V_{OVLO} = 1.3V$, $T_J = +25^\circ C$	-100		100	nA
IN Leakage Voltage by OVLO	V_{IN_LEAK}	$V_{OVLO} = 20V$, $V_{IN} =$ unconnected, $R_{OVLO} = 1M\Omega$			0.2	V
Thermal Shutdown				150		$^\circ C$
Thermal Shutdown Hysteresis				20		$^\circ C$
Digital Signal (nACOK, nEN)						
nACOK Output Low Voltage	V_{OL}	$V_{IO} = 3.3V$, $I_{SINK} = 1mA$, see Figure 1		0.08	0.32	V
nACOK Leakage Current	I_{ACOK_LEAK}	$V_{IO} = 3.3V$, nACOK de-asserted, $T_J = +25^\circ C$, see Figure 1			1	μA
nEN Input Low Threshold	V_{LTH}				0.4	V
nEN Input High Threshold	V_{HTH}		1.2			V
nEN Input Leakage	I_{nEN_LEAK}	$V_{IN} = 5V$, $T_J = +25^\circ C$			1	μA
Timing Characteristics						
Debounce Time	t_{DEB}	Time from $V_{IN} > 2.5V$ to the time V_{OUT} starts rising, $T_J = +25^\circ C$		15		ms
Soft-Start Time	t_{SS}	Time from $V_{IN} > 2.5V$ to soft-start off, $T_J = +25^\circ C$		30		ms
Switch Turn-On Time	t_{ON}	$V_{IN} = 5V$, $R_L = 100\Omega$, $C_{LOAD} = 100\mu F$, V_{OUT} from 10%, V_{IN} to 90% V_{IN} , $T_J = +25^\circ C$		1.5		ms
Switch Turn-Off Time	t_{OFF}	$V_{IN} > V_{IN_OVLO}$ to $V_{OUT} = 80\%$ of V_{IN} , $R_L = 100\Omega$, with 20% overdrive, for the case of using the internal threshold, $T_J = +25^\circ C$		50		ns
Switch Turn-Off Propagation Delay	t_{DELAY}	$V_{OVLO} > V_{BG}$ with 20% overdrive to output falling 10%, $R_L = 100\Omega$, for the case of using external threshold, $T_J = +25^\circ C$		80		ns

TYPICAL PERFORMANCE CHARACTERISTICS

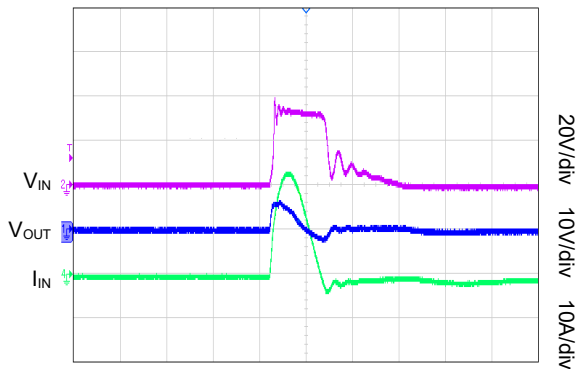


TYPICAL PERFORMANCE CHARACTERISTICS (continued)



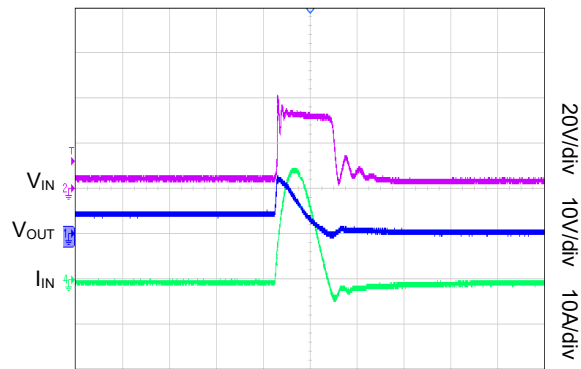
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

IN-GND 90V Surge Discharge Waveforms
(Off-State) (SGM4066A)



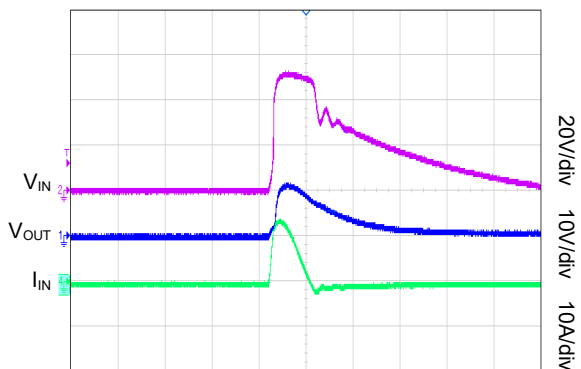
Time (20 μ s/div)

IN-GND 90V Surge Discharge Waveforms
(On-State) (SGM4066A)



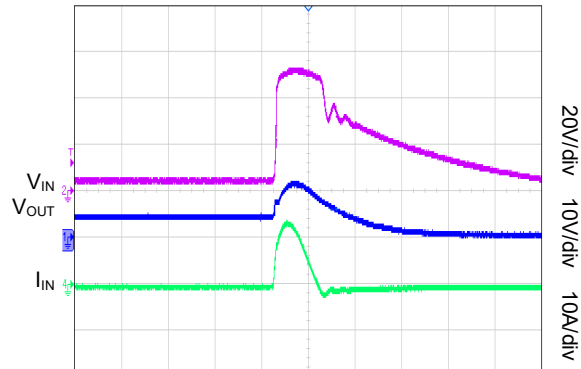
Time (20 μ s/div)

IN-GND 80V Surge Discharge Waveforms
(Off-State) (SGM4066B)



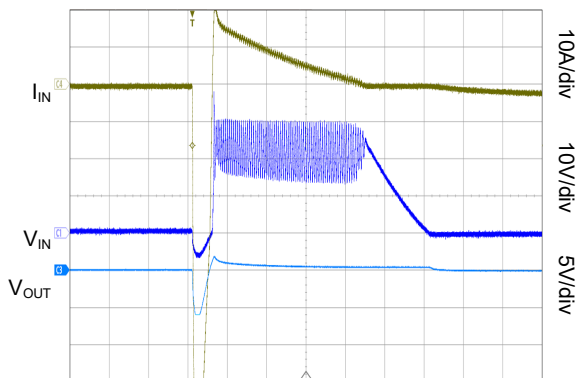
Time (20 μ s/div)

IN-GND 80V Surge Discharge Waveforms
(On-State) (SGM4066B)



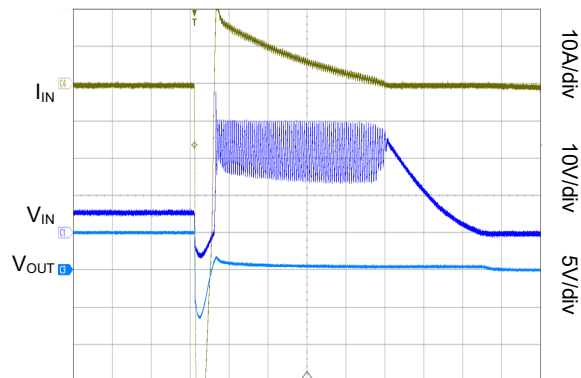
Time (20 μ s/div)

IN-GND -400V Surge Discharge Waveforms
(Off-State)



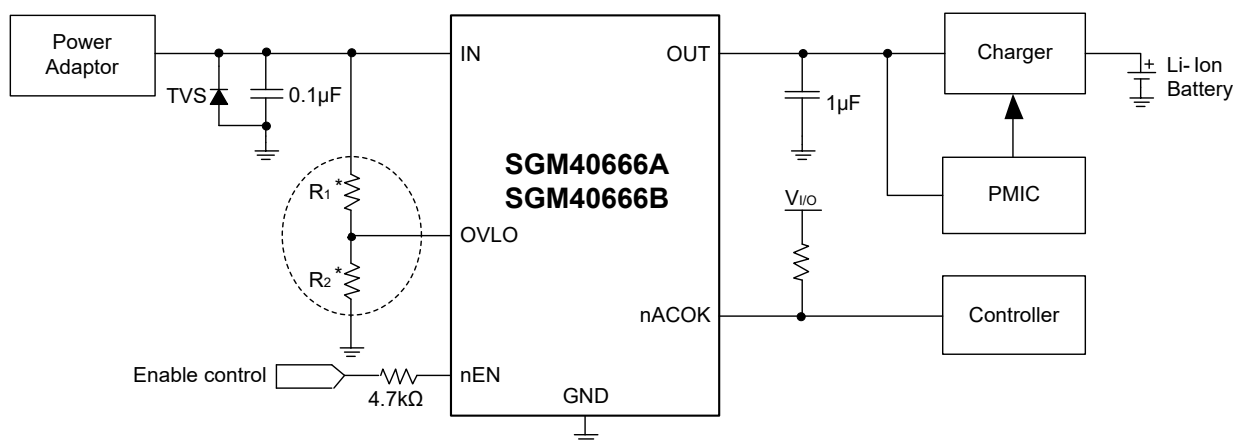
Time (50 μ s/div)

IN-GND -400V Surge Discharge Waveforms
(On-State)



Time (50 μ s/div)

TYPICAL APPLICATION



* Voltage divider network R1 and R2 is only used for adjustable OVLO;
When using the default OVP threshold, connect OVLO to GND directly.

Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

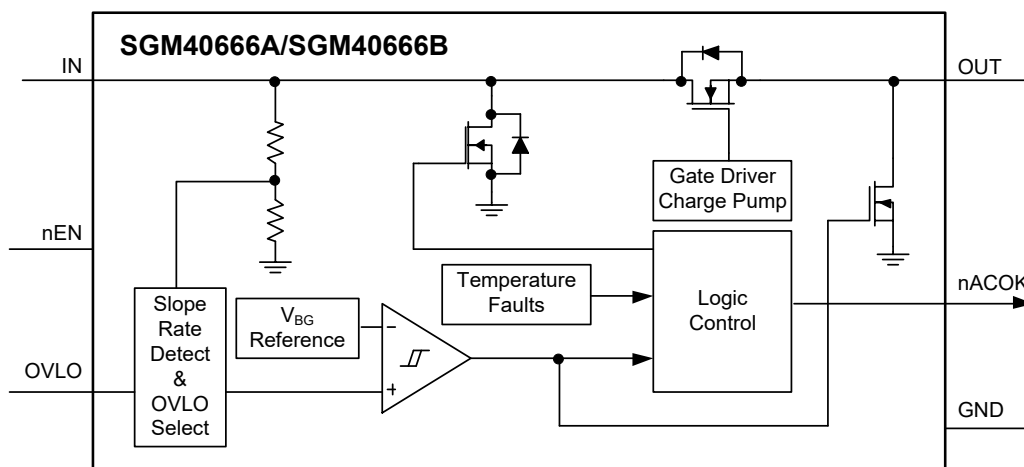
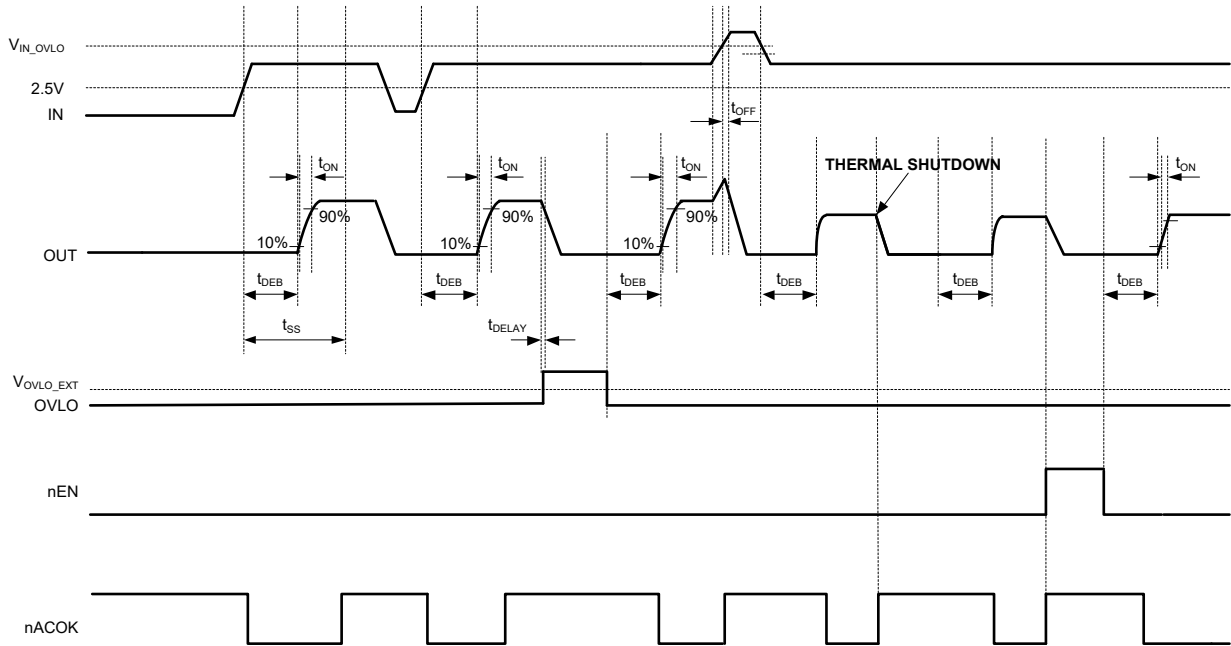


Figure 2. Functional Block Diagram

TIMING DIAGRAM



NOTE: Waveforms are not to scale.

Figure 3. Timing Diagram

SURGE UP TEST CIRCUIT

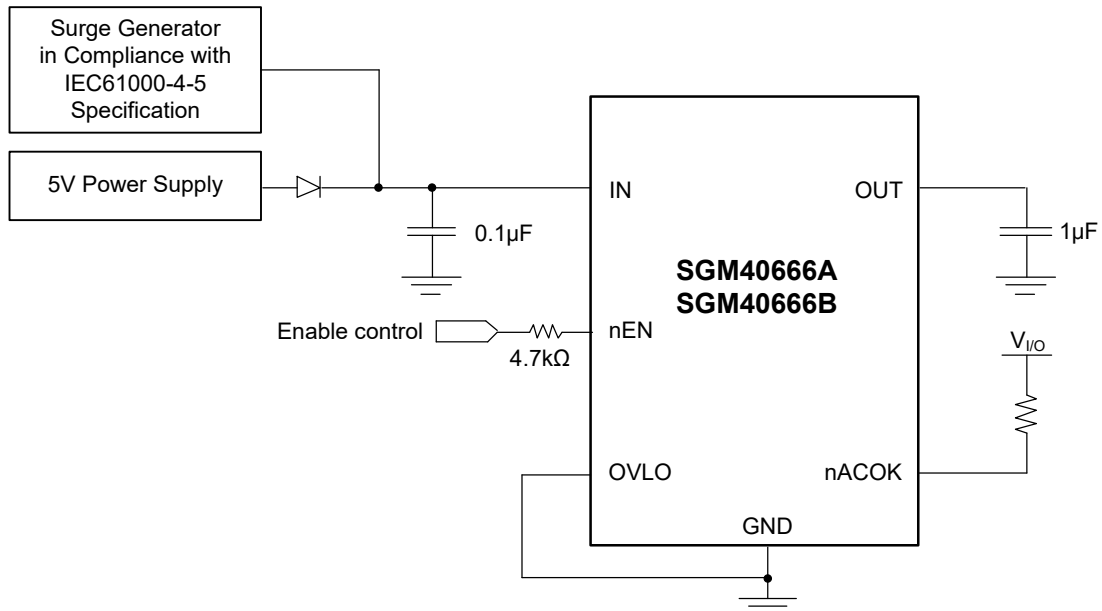


Figure 4. Surge Up Test Circuit

DETAILED DESCRIPTION

The SGM40666A and SGM40666B are designed to protect low voltage systems from damage with a high voltage supply up to +31V_{DC} and +40V_{PEAK} (10s with 50mA current limit). The SGM40666A withstands +90V/-400V while SGM40666B can also withstand surges up to +80V/-400V without damage. Surge up tests are performed according to the test circuit in Figure 4. If the input voltage exceeds the over-voltage threshold, the internal 28mΩ (TYP) low R_{ON} FET is turned off to prevent damage to the protected components. A built-in 15ms (TYP) debounce time prevents turning the internal FET on falsely during start-up.

Device Operation

The devices contain a timing logic controlled charge pump, which is used as gate driver of the internal FET. If internal trip threshold is used, the charge pump is enabled when V_{IN} < V_{IN_OVLO}, while if external trip threshold is used, it is enabled when V_{OVLO} < V_{OVLO_EXT}.

The charge pump turns the internal FET on after a 15ms (TYP) debounce delay (see Figure 3), then soft-start function limits the FET inrush current for another 15ms (TYP). Once V_{IN} rises above V_{OVLO_THRESH}, the FET is turned off.

Enable Function

The IC has an enable pin which is used to enable or disable the device. Pulling nEN high to turn off the internal pass FET, while pulling low to turn on the FET, and the IC enters the start-up routine.

Over-Voltage Lockout (OVLO)

The typical over-voltage lockout (OVLO) thresholds of the SGM40666A and SGM40666B are 6.83V.

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 50ns. The switch will remain off until V_{IN} falls below the OVP falling trip level.

External Adjustable OVLO

The devices detect voltage at the OVLO pin to check if an external divider exists.

If OVLO pin is connected to ground, the internally set OVLO value will be applied.

If an external resistor divider network is connected to OVLO pin and V_{OVLO} exceeds the OVLO select voltage, V_{OVLO_SELECT}, 0.27V (TYP), then this external resistor

divider determines the V_{IN_OVLO_EXT}. Since V_{IN_OVLO_EXT}, V_{BG}, and R₁ are known, R₂ can be calculated from the following formula:

$$V_{IN_OVLO_EXT} = V_{BG} \times \left[1 + \frac{R_1}{R_2} \right] \quad (1)$$

This external resistor divider network is completely independent from the internal resistor divider network.

NOTE: OVLO pin must not be floating.

Surge Protection

The SGM40666A integrates a clamping circuit to suppress input surge voltage. When V_{IN} voltage rises sharply (typically > 4.5V/μs) above 32.3V, the internal clamping circuit will be triggered to discharge the surge energy to the ground.

The SGM40666B discharges the surge energy to the ground when surge voltage rises above 45V.

Thermal Shutdown Protection

The SGM40666A and SGM40666B feature thermal shutdown circuitry. If the junction temperature exceeds +150°C (TYP), the internal FET turns off. And the devices exit thermal shutdown if the junction temperature cools down by 20°C (TYP).

nACOK Output

An open-drain nACOK output gives the SGM40666A and SGM40666B ability to indicate a stable power source to the host. nACOK is driven low when input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce delay. Connect a pull-up resistor from nACOK to the host system logic I/O voltage. nACOK is high impedance after thermal shutdown.

USB OTG Support

When used in an OTG application, the SGM40666A and SGM40666B can provide power from OUT to IN. Initially, the OTG voltage applied at OUT will forward-bias the power switch bulk diode and present a voltage drop of approximately 0.7V between OUT and IN. Once the voltage at IN exceeds the minimum input voltage of 2.5V and after debounce time, the main power switch will turn fully on, significantly reducing the voltage drop from OUT to IN. In this mode, the part is able to supply a continuous current up to 3.5A to the OTG load.

APPLICATION INFORMATION

IN Bypass Capacitor

For most applications, place a 0.1 μ F ceramic bypass capacitor between IN and GND pins as close as possible to the device. If the power source has significant inductance due to long lead length, the device clamps the overshoot due to LC tank circuit.

Output Capacitor

The slow turn-on time provides a soft-start function, and this allows the SGM40666A and SGM40666B to charge an output capacitor (up to 1000 μ F typically) without turning off due to over-current condition.

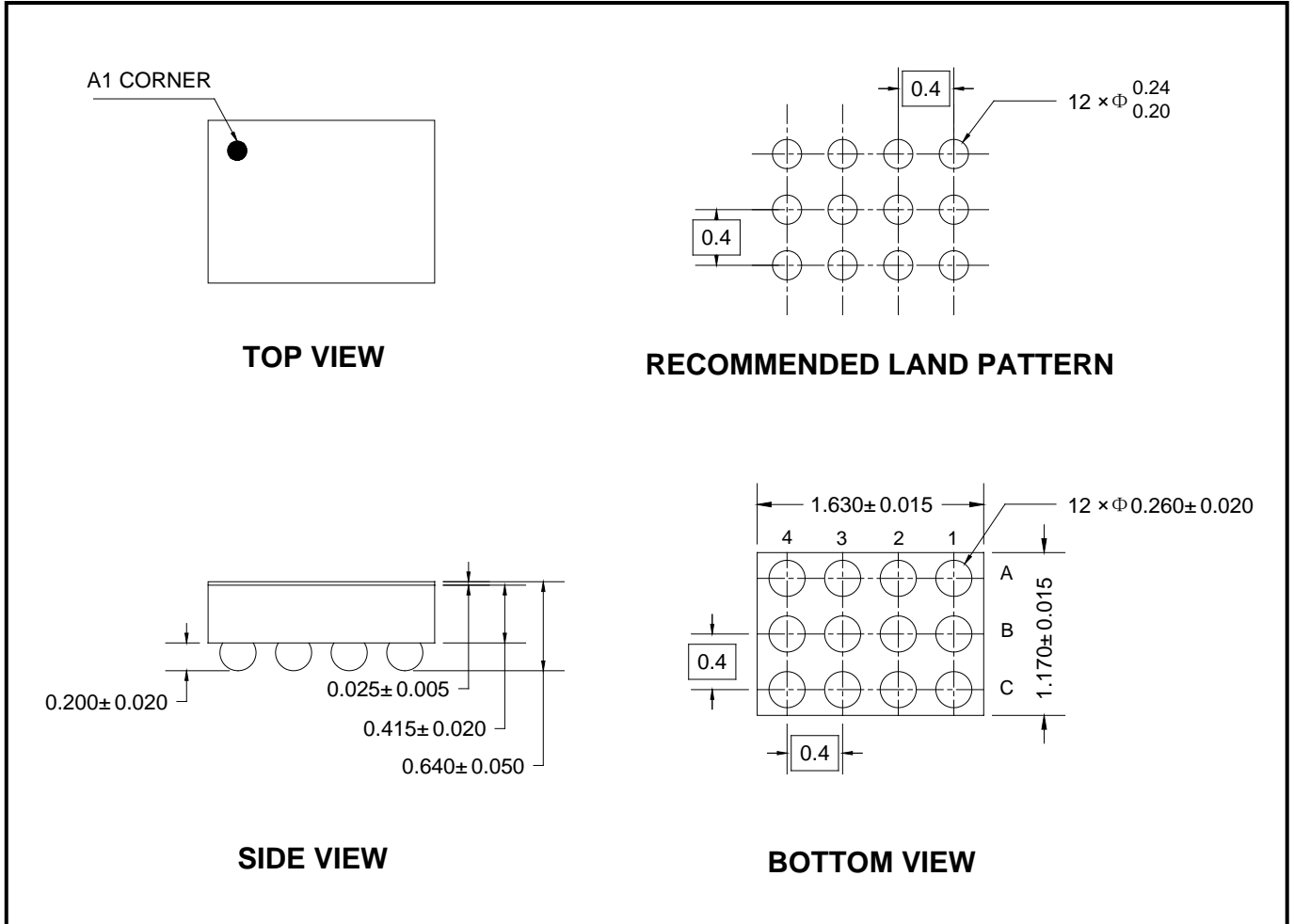
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2020) to REV.A	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

WLCSP-1.17x1.63-12B



NOTE: All linear dimensions are in millimeters.

PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.17×1.63-12B	7"	9.0	1.32	1.78	0.82	4.0	4.0	2.0	8.0	Q2

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PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002