GENERAL DESCRIPTION

BL8891B combines a dedicated current mode PWM controller with a high voltage power MOSFET. It is optimized for high performance, low standby power, and cost effective off-line flyback converter applications.

BL8891B offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). Excellent EMI performance is achieved with proprietary frequency shuffling technique together with soft switching control at the totem pole gate drive output.

The tone energy at below 20KHZ is minimized in the design and audio noise is eliminated during operation.

BL8891B is offered in DIP-7 package.

FEATURES

■Power on Soft Start Reducing MOSFET VDS Stress
■Frequency shuffling for EMI
■Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
■Audio Noise Free Operation
■Fixed 50KHZ Switching Frequency
■Internal Synchronized Slope Compensation
■Low VDD Startup Current and Low Operating Current
■Leading Edge Blanking on Current Sense Input
Good Protection Coverage With Auto Self-Recovery

- VDD Over Voltage Clamp and Under Voltage Lockout with Hysteresis (UVLO)
- Line Input Compensated Cycle-by-Cycle Over-current Threshold Setting For Constant Output Power Limiting Over Universal Input Voltage Range
- Overload Protection (OLP)
- Over voltage Protection (OVP)

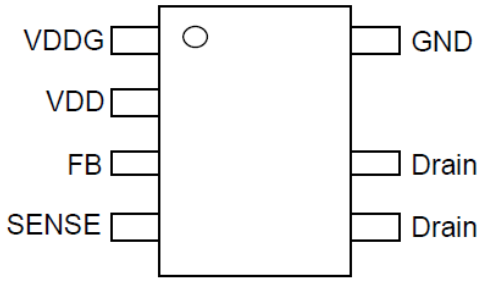
■DIP7 package

APPLICATIONS

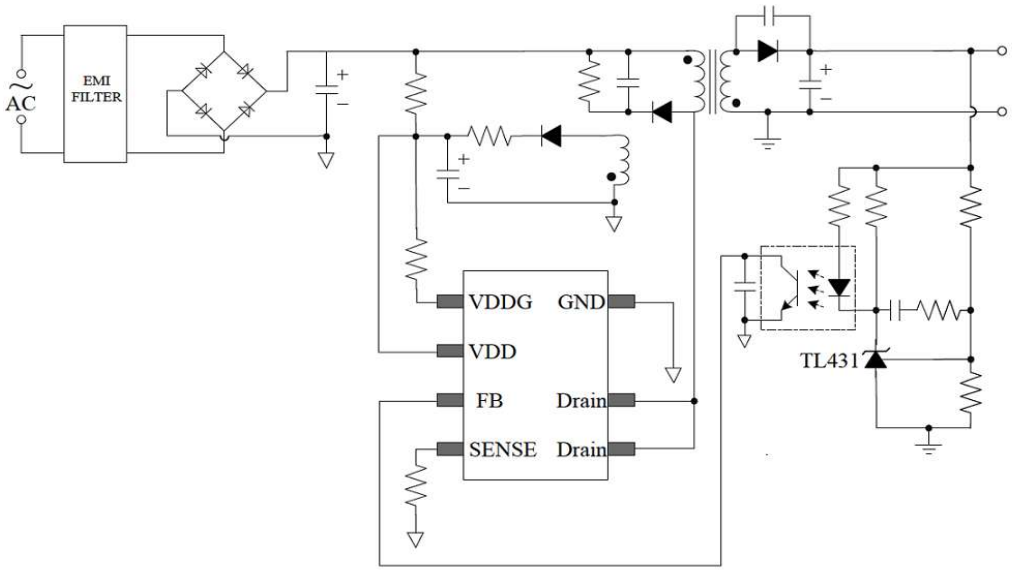
Offline AC/DC flyback converter for
■Battery Charger
■PDA power supplies
■Digital Cameras and Camcorder Adaptor
■VCR, SVR, STB, DVD&DVCD Player SM
■Set-Top Box Power
■Auxiliary Power Supply for PC and Server
■Open-frame SMPS

Pin Configuration

The BL8891B is offered in DIP7 package as shown below.



TYPICAL APPLICATION



Absolute Maximum Ratings

Drain Voltage (off state)	-0.3V to 650V
VDD Voltage	-0.3V to 30V
VDD-G Input Voltage	-0.3V to 30V
VDD Clamp Continuous Current	10mA
FB Input Voltage	-0.3V to 7V
SENSE Input Voltage	-0.3V to 7V
Min/Max Operating Junction Temperature TJ	0℃ to 125℃
Min/Max Storage Temperature Tstg	-25℃ to 150℃
Lead Temperature (Soldering,10secs)	260℃
Ambient Operating Temperature	-25℃ to 85℃
Thermal Resistance from Junction to case θ_{JC}	15℃/W
Thermal Resistance from Junction to ambient θ_{JA}	75℃/W

Note: θ_{JA} is measured with the PCB copper area of approximately 1 in^2(Multi-layer). That need connect to exposed pad.

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
GND	P	Ground
VDD-G	P	Internal Gate Driver Power Supply
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4.
SENSE	I	Current sense input
Drain	O	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer
VDD	P	IC DC power supply Input

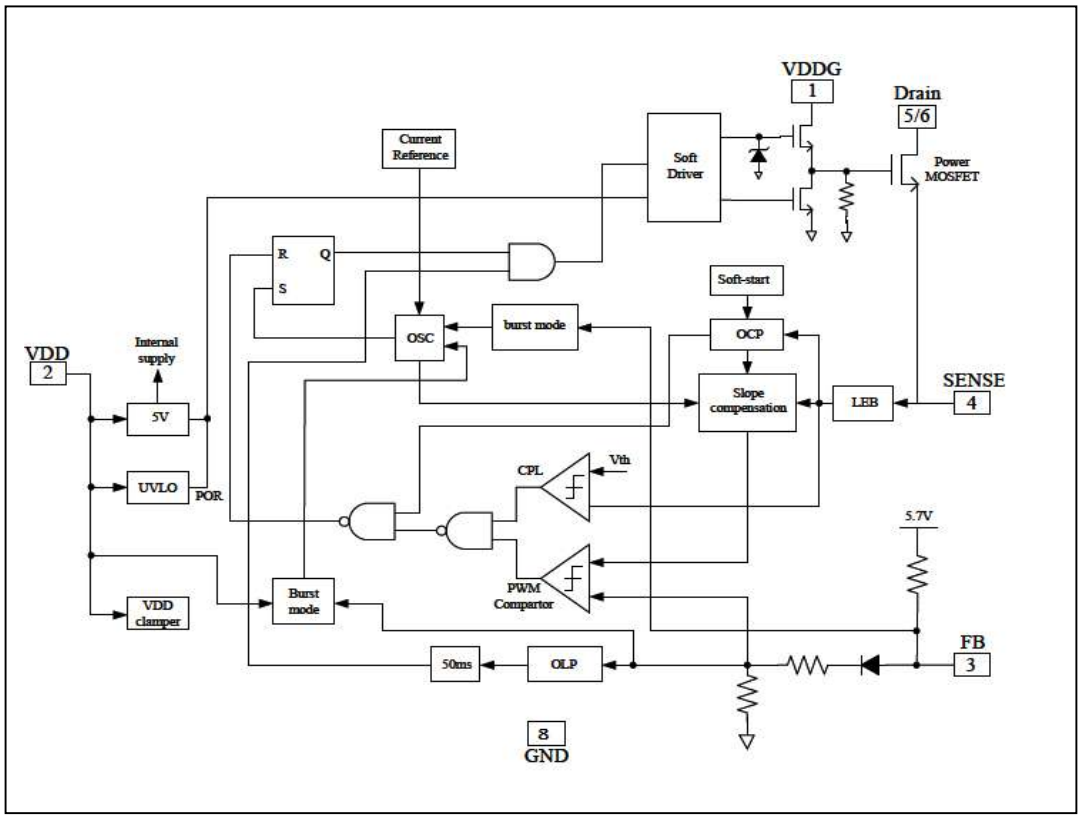
OUTPUT POWER TABLE

Product	230VAC±15%	85-264VAC	Package
	Open Frame	Open Frame	
BL8891B25	20W	15W	**DIP7**
BL8891B20	15W	12W	**DIP7**

Notes:

1. Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 50℃ ambient.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(TA = 25℃, VDD=VDDG=16V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD)						
I _start up	VDD Startup Current	VDD=14.5V,Measure Leakage current into VDD		5	20	uA
I_op	Operation Current	VFB=3V		2.1		mA
UVLO(ON)	VDD Under Voltage Lockout Enter		8.7	9.3	10.7	V
UVLO(OFF)	VDD Under Voltage Lockout Exit		14.8	15.3	16.0	V
VDD_Clamp	VDD Zener Clamp Voltage	IDD=10mA		30		V
OVP(ON)	Over Voltage Protection Threshold	CS=0V,FB=3VRamp up VDD until gate clock is off	27	28.8	30	V
Feedback Input Section (FB Pin)						
VFB _Open	VFB Open LoopVoltage		5.4	5.6	6	V
IFB _Short	FB pin short circuit current	Short FB pin to GND and measure current		1.45		mA
VTH_0D	Zero Duty Cycle FB Threshold Voltage			1.23		V
VTH_PL	Power Limiting FB Threshold Voltage			3.5		V
TD_PL	Power Limiting FB Debounce Time			50		ms
ZFB_IN	Input Impedance			4		KΩ
Current Sense Input (Sense Pin)						
Soft start time				4		ms
T_ blanking	Leading edge blanking time			270		ns
ZSENSE_ IN	Input Impedance			40		KΩ
TD_ OC	Over Current Detection and Control Delay	From Over Current occurs till the Gate drive output start to turn off		120		ns
VTH_ OC	Internal Current Limiting Threshold Voltage	FB=3.3V		0.95		V
Oscillator						
Fosc	Normal Oscillation Frequency		43	48	53	KHz
∆f_ Temp	Frequency Temperature Stability			5		%
∆f_ VDD	Frequency Voltage Stability			5		%

D_ max	Maximum duty cycle(Note)	FB=3.3V,CS=0V	70	80	90	%
F_ Burst	Burst Mode Base Frequency			22		KHz
Power MOSFET Section						
BV-DSS	MOSFET Drain-Source Breakdown Voltage		650			V
On Resistance	Rdson(Note)	BL8891B25		3.0		Ω
		BL8891B20		4.0		
Frequency						
△_VDD	Frequency Modulation range/Base frequency		-5		+5	%

Note: Guaranteed by design.

OPERATION DESCRIPTION

The BL8891B is a low power off-line SMPS Switcher optimized for off-line flyback converter applications. The 'Extended burst mode' control greatly reduces the standby power consumption and help the design easily to meet the international power conservation requirements.

● Startup Current and Start up Control

Startup current of BL8891B is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application. For AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

● Operating Current

The Operating current of BL8891B is low at 2mA.Good efficiency is achieved with BL8891B low operating current together with the 'Extended burst mode' control features.

● Soft Start

BL8891B features an internal 4ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the peak current is gradually increased from nearly zero to the maximum level of 0.95V. Every restart up is followed by a soft start.

● Frequency shuffling for EMI improvement

The frequency Shuffling (switching frequency modulation) is implemented in BL8891B. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

● Extended Burst Mode Operation

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the mosfet, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy. The switching frequency is internally adjusted at no load or light load condition.

The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drop below burst mode threshold level and device

enters Burst Mode control. The Gate drive output switches only when VDD voltage drop below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The switching frequency control also eliminates the audio noise at any loading conditions.

● **Oscillator Operation**

The switching frequency of BL8891B is internally fixed at 50KHZ. No external frequency setting components are required for PCB design simplification.

● **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in BL8891B current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of internal power MOSFET so that the external RC A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

In addition to the gate drive control scheme mentioned, the gate drive strength can also be adjusted externally by a resistor connected between VDD and VDDG, the falling edge of the Drain output can be well controlled. It provides great flexibility for system EMI design.

● **Protection Controls**

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load filtering on sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

● **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

● **Drive**

The internal power MOSFET in BL8891B is driven by a dedicated gate driver for power switch control. Too weak the gate drives strength results in higher conduction and switch loss of MOSFET while too strong gate drive results the compromise of EMI.

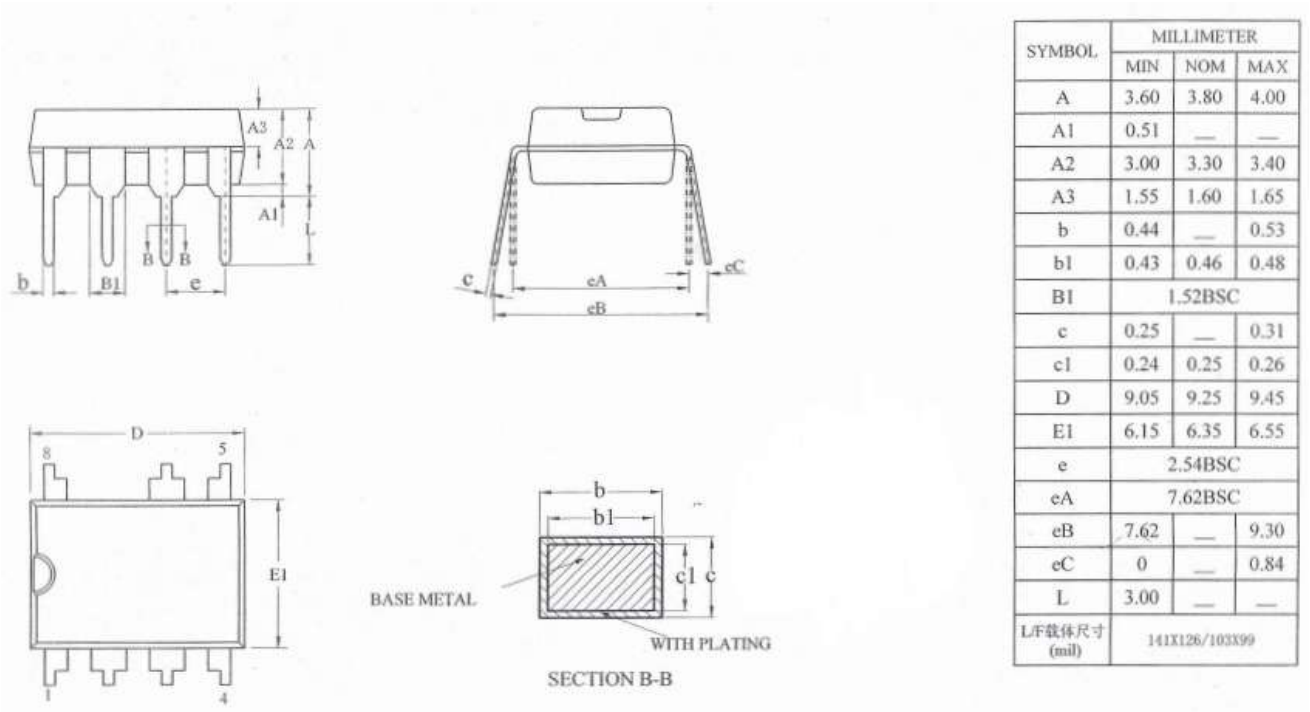
●**Protection Controls**

Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO).

With Proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the switcher. Switcher restarts when VDD voltage drop below UVLO limit.

VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than 30V. The output of BL8891B is shut down when VDD drop below UVLO_ON limit and Switcher enters power on start-up sequence.

Package Information DIP7



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	—	—
A2	3.00	3.30	3.40
A3	1.55	1.60	1.65
b	0.44	—	0.53
b1	0.43	0.46	0.48
B1	1.52BSC		
c	0.25	—	0.31
c1	0.24	0.25	0.26
D	9.05	9.25	9.45
E1	6.15	6.35	6.55
e	2.54BSC		
eA	7.62BSC		
eB	7.62	—	9.30
eC	0	—	0.84
L	3.00	—	—
L/F载体尺寸 (mil)	141X126/103X99		