I²C Controlled 13.5V/3A, 1-Cell Battery Charger with Power Path Management and USB Charger Detection

DESCRIPTION

ETA6963 is a highly-integrated 3A switch-mode battery charge and system power path management device for single cell Li-Ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smart phones, tablets and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life. Its input voltage and current regulation deliver maximum charging power. The solution is highly integrated with input reverse-blocking FET, high/low-side switching FET, and battery FET. It also integrates the bootstrap diode for the high-side gate drive. The I2C serial interface with charging and system settings makes the device a truly flexible solution. The device supports a wide range of input sources. The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. The device also meets USB On-the-Go (OTG) operation power rating specification by supplying 5.15 V on BUS pin with constant current limit up to 1.2A.The power path management regulates the system slightly above battery voltage but does not drop below 3.5 V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This Supplement Mode prevents overloading the input source.

The ETA6963 is available in a QFN4x4-24L package.

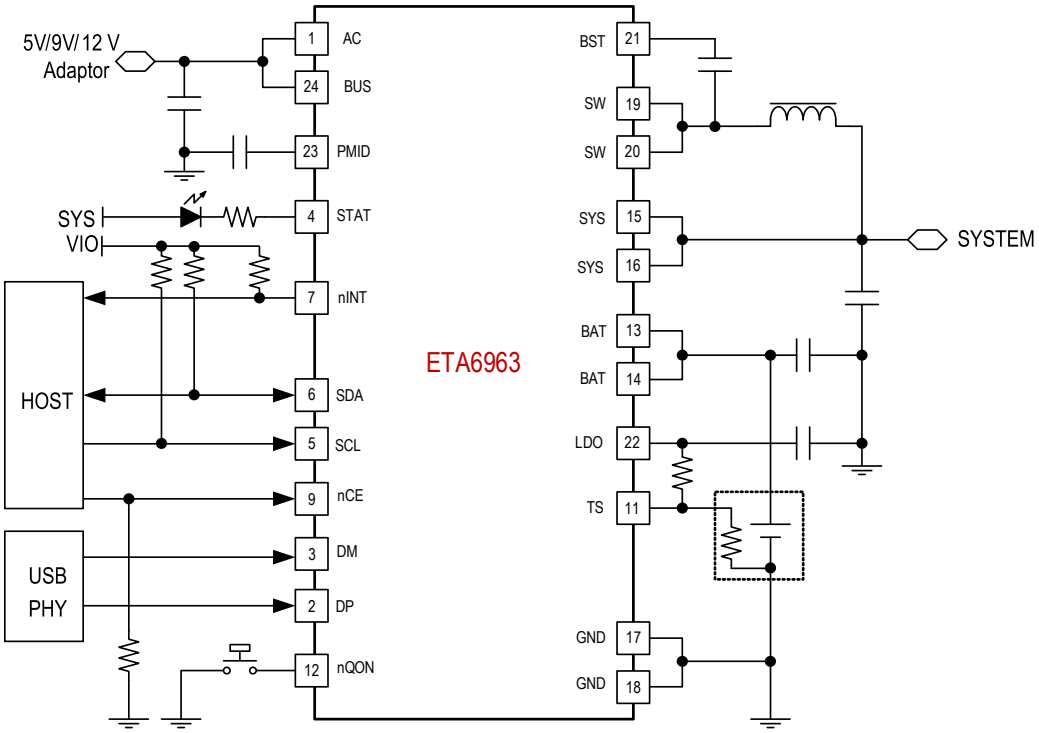
FEATURES

- High-Efficiency, 1.5MHz, Synchronous Switching Buck Charger
  - 90% Charge Efficiency at 2A from 5V Input
  - Programmable PFM Mode for Light Load Conditions
- Supports USB On-The-Go (OTG)
  - Programmable Current Limit Boost Converter with Up to 1.2A Output
- Wide Range Single Input to Support both USB Input and High Voltage Adapters
  - Support 3.9V to 13.5V Input Voltage Range With 22V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit (100mA to 3.2A With 100mA Resolution)
  - Auto Detect USB BC1.2, SDP, CDP, DCP and Non-Standard Adaptors
- Narrow VDC (NVDC) Power Path Management
- BATFET Control to Support Ship Mode, Wake Up and Full System Reset
- Flexible Autonomous and I²C Mode for Optimal System Performance
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Thermal Regulation and Thermal Shutdown
- Input UVLO and Overvoltage Protection

APPLICATIONS

- Tablet PC, Smart Phone, Internet Devices
- Portable Audio Speaker, Handheld Computers, PDA, POS

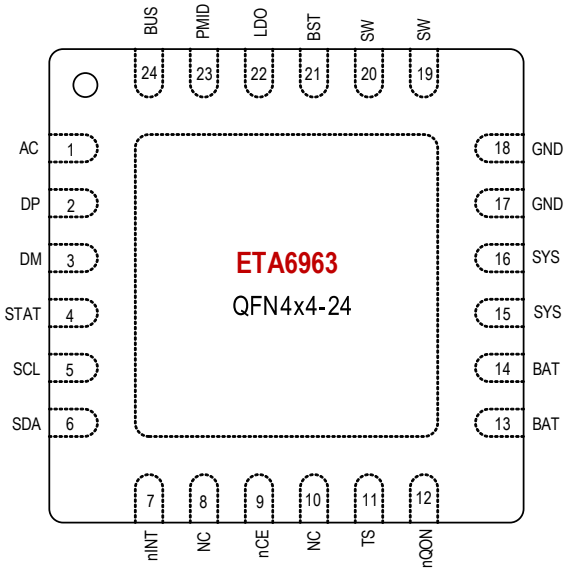
TYPICAL APPLICATION



ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA6963Q4Y	QFN4x4-24	ETA6963 YWW2L	5000

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

AC, BUS, PMID pin to GND Voltage .....–2V to 22V
SW to GND Voltage.....–0.3V to 22V
SYS, BAT to GND Voltage.....–0.3V to 6V
BST to SW Voltage .....–0.3V to 6V
All Other Pin to GND Voltage..... –0.3V to 6V
SW, BUS, BAT, SYS to PGND current.....Internally limited
Operating Temperature Range.....–40°C to 85°C
Storage Temperature Range.....–55°C to 150°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN4x4–24	35	10	°C/W

Lead Temperature (Soldering,10sec) .....260°C
ESD HBM (Human Body Mode) 2KV

ELECTRICAL CHARACTERISTICS

(V_{BAT} = 3.6V, unless otherwise specified. Typical values are at T_A = 25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
QUIESCENT CURRENTS					
Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4.5V, V_{BUS} < $V_{BUS-UVLOZ}$, leakage between BAT and BUS, T_J< 85°C			5	μA
Battery discharge current (BAT) in buck mode	V_{BAT} = 4.5V, HIZ Mode and BATFET_DIS = 1 or No V_{BUS}, I²C disabled, BATFET Disabled. T_J < 85°C		20	40	μA
Battery discharge current (BAT, SW, SYS)	V_{BAT} = 4.5V, HIZ Mode and OVPFET_DIS = 1 or No V_{BUS}, I2C Disabled, BATFET Enabled. T_J < 85°C		80	160	μA
Input supply current (V_{BUS}) in buck mode	V_{BUS} > V_{BUS_UVLO}, V_{BUS} > V_{BAT}, converter switching, V_{BAT} = 3.8V, I_{SYS} = 0A		5		mA
Battery Discharge Current in boost mode	V_{BAT} = 4.2V, boost mode, I_{BUS} = 0A, converter switching		2		mA
BUS, AC AND BAT PIN POWER-UP					
V_{BUS} operating range	V_{BUS} rising	3.9		13.5	V
V_{BUS} for active I²C, no battery Sense BUS pin voltage	V_{BUS} rising		3.3	3.6	V
I²C active hysteresis	V_{BUS} falling from above V_{BUS_UVLO}		300		mV
One of the conditions to turn on LDO	V_{BUS} rising		3.65	3.9	V
One of the conditions to turn on LDO	V_{BUS} falling		500		mV
Sleep mode falling threshold	(V_{BUS}–V_{BAT}), V_{BUSMIN_FALL} ≤ V_{BAT} ≤ V_{REG}, V_{BUS} falling	15	60	110	mV
Sleep mode rising threshold	(V_{BUS}–V_{BAT}), V_{BUSMIN_FALL} ≤ V_{BAT}≤ V_{REG}, V_{BUS} rising	110	220	330	mV
V_{BUS} 6.5V Overvoltage rising threshold	V_{BUS} rising, OVP<1:0> = '01'	6	6.5	7	V
V_{BUS} 11V Overvoltage rising threshold	V_{BUS} rising, OVP<1:0> = '10'	10	11	12	V
V_{BUS} 14V Overvoltage rising threshold	V_{BUS} rising, OVP<1:0> = '11'	13	14	15	V
V_{BUS} 6.5V Overvoltage hysteresis	V_{BUS} falling, OVP<1:0> = '01'		220		mV
V_{BUS} 11V Overvoltage hysteresis	V_{BUS} falling, OVP<1:0> = '10'		400		mV

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BUS} 14V Overvoltage hysteresis	V_{BUS} falling, OVP<1:0> = '11'		500		mV
BAT for active I²C, no adapter	V_{BAT} rising	2.5	2.7		V
Battery Depletion Threshold	V_{BAT} falling	2.2	2.4	2.6	V
Battery Depletion Threshold	V_{BAT} rising	2.35	2.58	2.8	V
Battery Depletion rising hysteresis	V_{BAT} rising		180		mV
Bad adapter detection falling threshold	V_{BUS} falling	3.7	3.9	4.1	V
Bad adapter detection hysteresis			80		mV
Bad adapter detection current source	Sink current from V_{BUS} to GND		30		mA
POWER-PATH					
System regulation voltage	V_{BAT} < SYS_MIN[2:0] = 101, BATFET Disabled (REG07[5] = 1)		3.68		V
System Regulation Voltage	I_{SYS} = 0A, V_{BAT} > V_{SYS_MIN}, BATFET disabled (REG07[5] = 1)		V_{BAT}+ 70mV		
Maximum DC system voltage output	I_{SYS} = 0A, V_{BAT} = 4.4V, BATFET disabled (REG07[5] = 1)		4.47		V
Top reverse blocking MOSFET on-resistance between VBUS and PMID - Q1	-40°C≤ TA ≤ 125°C	20	40	60	mΩ
Top switching MOSFET on-resistance between PMID and SW-Q2	V_{LDO} = 5 V , -40°C≤ T_A ≤ 125°C	35	70	105	mΩ
Bottom switching MOSFET on-resistance between SW and GND-Q3	V_{LDO} = 5 V , -40°C≤ T_A ≤ 125°C	21	43	65	mΩ
SYS-BAT MOSFET on-resistance – Q4	QFN package, Measured from BAT to SYS, V_{BAT} = 4.2V, T_J =–40-125°C	13	27	40	mΩ
BATFET forward voltage in supplement mode			30		mV
BATTERY CHARGER					
Change voltage program range		3.848		4.616	V
Charge voltage step			32		mV
Charge voltage setting	V_{REG} (REG04[7:3]= 01011) = 4.2 V	4.179	4.2	4.221	V
Charge voltage setting accuracy	V_{BAT} = 4.2 V	-0.5		+0.5	%
Charge current regulation range		0		3000	mA
Charge current regulation step			60		mA
Charge current regulation setting	I_{CHG} = 240 mA, V_{BAT} = 3.8V		0.24		A
Charge current regulation accuracy	I_{CHG} = 240 mA, V_{BAT} = 3.8V	-10		+10	%
Battery LOW falling threshold	I_{CHG} = 240mA	2.6	2.8	3	V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Battery LOW rising threshold	Pre-charge to Fast charge	2.9	3.1	3.3	V
Pre-charge current regulation	IPRECHG[3:0] = '0010'	90	180	270	mA
Termination current regulation	ITERM[3:0] = '0010',V_{BAT} = 4.2V	90	180	270	mA
Battery short voltage	V_{BAT} falling	1.8	2	2.2	V
Battery short voltage	V_{BAT} rising	2.05	2.25	2.45	V
Battery short current	V_{BAT} =1V		145		mA
Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 0	70	120	170	mV
Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 1	190	240	290	mV
INPUT VOLTAGE AND CURRENT REGULATION					
Input voltage regulation limit	VINDPM[3:0] = 0110 = 4.5 V	4.32	4.5	4.68	V
Input voltage regulation accuracy		-4		4	%
Input voltage regulation limit tracking V_{BAT}	VINDPM[3:0] = 3.9V, $V_{DPM\_VBAT\_TRACK}$ = 300mV, V_{BAT} = 4.0V	4.13	4.3	4.47	V
USB input current regulation limit	V_{BUS} = 5V, current pulled from SW, IINDPM [4:0] = 10111	2.16	2.4	2.64	A
Input current limit during system start-up sequence			200		mA
BAT PIN OVERVOLTAGE PROTECTION					
Battery overvoltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		108		%
Battery overvoltage threshold Hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		103		%
THERMAL REGULATION AND THERMAL SHUTDOWN					
Junction Temperature Regulation Threshold	Temperature Increasing, TREG = 1		110		°C
Junction Temperature Regulation Threshold	Temperature Increasing, TREG = 0		90		°C
Thermal Shutdown Rising Temperature			160		°C
Thermal Shutdown Hysteresis			30		°C
JEITA Thermistor Comparator (BUCK MODE)					
T1 (0°C) threshold, Charge suspended T1 below this temperature.	Charger suspends charge. As Percentage to V_{LDO}		73.3		% V_{LDO}
Falling	As Percentage to V_{LDO}		71.5		% V_{LDO}
T2 (10°C) threshold, Charge back to I_{CHG}/2 and 4.2 V below this temperature	As Percentage to V_{LDO}		68		% V_{LDO}
Falling	As Percentage to V_{LDO}		66.8		% V_{LDO}

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
T3 (45°C) threshold, charge back to I_{CHG} and 4.05V above this temperature.	Charger suspends charge. As Percentage to V_{LDO}		44.7		% V_{LDO}
Falling	As Percentage to V_{LDO}		45.7		% V_{LDO}
T5 (60°C) threshold, charge suspended above this temperature	As Percentage to V_{LDO}		34.2		% V_{LDO}
Falling	As Percentage to V_{LDO}		35.3		% V_{LDO}
COLD OR HOT THERMISTER COMPARATOR (BOOST MODE)					
Cold Temperature Threshold, TS pin Voltage Rising Threshold	As Percentage to V_{LDO} (Approx. -20°C w/ 103AT) TJ = –20°C - 125°C	78	80	82	% V_{LDO}
Falling	TJ = –20°C - 125°C	77	79	81	% V_{LDO}
Hot Temperature Threshold, TS pin Voltage falling Threshold	As Percentage to V_{LDO} (Approx. 60°C w/ 103AT), TJ = –20°C - 125°C	29.2	31.2	33.2	% V_{LDO}
Rising	TJ = –20°C - 125°C	32.4	34.4	36.4	% V_{LDO}
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)					
HSFET cycle-by-cycle over-current threshold		4.8	5.8	7.5	A
System over load threshold		4.7	5.2	5.7	A
CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)					
LSFET under-current falling threshold	From sync mode to non-sync mode		250		mA
PWM					
PWM switching frequency	Oscillator frequency		1500		kHz
Maximum PWM duty cycle			97		%
BOOST MODE OPERATION					
Boost mode regulation voltage	V_{BAT} = 3.8 V, I_{PMID} = 0 A, BOOSTV[1:0] = '10'	5	5.15	5.3	V
Boost mode regulation voltage accuracy	V_{BAT} = 3.8 V, I_{PMID} = 0 A, BOOSTV[1:0] = '10'	-3		3	%
Battery voltage exiting boost mode	V_{BAT} falling, MIN_VBAT_SEL = 0	2.6	2.8	3.0	V
	V_{BAT} rising, MIN_VBAT_SEL =0	2.8	3	3.2	V
	V_{BAT} falling, MIN_VBAT_SEL = 1	2.3	2.5	2.7	V
	V_{BAT} rising, MIN_VBAT_SEL = 1	2.6	2.8	3.0	V
OTG mode output current	BOOST_LIM = 1	1.2	1.4		A
	BOOST_LIM = 0	0.5	0.7		A
OTG overvoltage threshold	Rising threshold	5.6	6	6.4	V
HSFET under current falling threshold			100		mA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Hiccup Retrying timer			7		ms
Hiccup Off timer			28		ms
Maximum retry allowed	After the last retry, part clear OTG_CONFIG bit to disable Boost		7		Time
VLDO REGULATION					
LDO output voltage	V_{BUS} = 9V, I_{LDO} = 40mA		5		V
LDO output current limit	V_{BUS} = 9V, V_{LDO} = 4V		80		mA
LOGIC I/O PIN CHARACTERISTICS (nCE, SCL, SDA)					
Input low threshold				0.4	V
Input high threshold		1.3			V
High-level leakage current	Pull up rail 1.8 V			1	μA
LOGIC I/O PIN CHARACTERISTICS (STAT, nINT)					
Low-level output voltage				0.4	V
VBUS/BAT POWER UP					
Bad adapter detection duration			30		ms
BATTERY CHARGER					
Deglitch time for charge Termination			7		S
Deglitch time for recharge			32		ms
System over-current deglitch time to turn off Q4			1		ms
Battery over-voltage deglitch time to disable charge			10		μs
Typical Charge Safety Timer Range	CHG_TIMER = 1		10		Hr
Typical Top-Off Timer Range	TOP_OFF_TIMER[1:0] = 10		30		min
nQON TIMING					
nQON low time to turn on BATFET and exit ship mode	–10°C ≤ T_J ≤ 60°C		1.15		s
nQON low time to reset BATFET	–10°C ≤ T_J ≤ 60°C		10		s
BATFET off time during full system reset	–10°C ≤ T_J ≤ 60°C		320		ms
Enter ship mode delay	–10 °C ≤ T_J ≤ 60°C		12		s
DIGITAL CLOCK AND WATCHDOG TIMER					
REG05[4]=01			40		s
DP/DM DETECTION					
VDP/DM_600MVSRC	Voltage source (600 mV)		600		mV
RDM_19K			19		kΩ
VDP/DM_0P325			0.325		V
V2P7_VTH	DP/DM Threshold for non-standard adapter	2.55	2.7	2.85	V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V2P0_VTH	DP/DM Threshold for non-standard adapter	1.85	2.0	2.15	V
V1P2_VTH	DP/DM Threshold for non-standard adapter	1.05	1.2	1.35	V

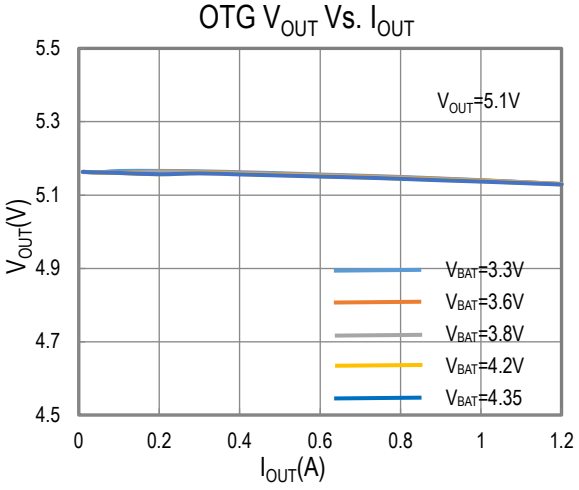
PIN DESCRIPTION

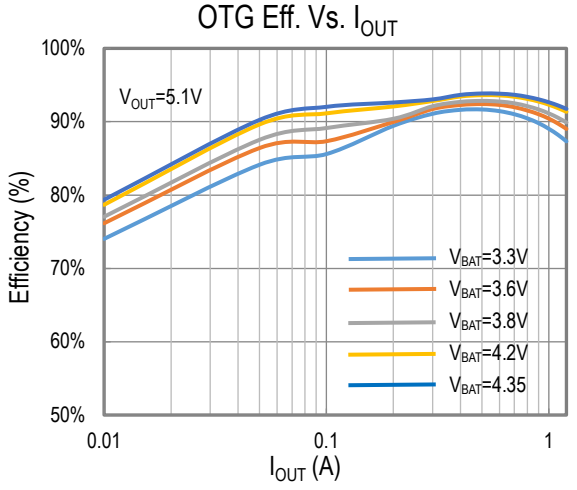
PIN NAME	PIN #	DESCRIPTION
AC	1	Charger input voltage sense. This pin must be connected to BUS pin
BUS	24	Charger input voltage. Bypass it with a 10μF ceramic capacitor from BUS to PGND. The capacitor should be close to the BUS pin
DP	2	Positive line of the USB data line pair. DP/DM based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors
DM	3	Negative line of the USB data line pair. DP/DM based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors
STAT	4	Open-drain charge status output. Connect the STAT pin to a logic rail via 10kΩ resistor. The STAT pin indicates charger status. Connect a current limit resistor and a LED from a rail to this pin. Charge in progress: LOW Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response)or No bat: 1Hz, 50% duty cycle Pulses
SCL	5	I^2C interface clock. Connect a 10kΩ pull up resistor to the logic rail
SDA	6	I^2C interface data. Connect a 10kΩ pull up resistor to the logic rail
nINT	7	Open-drain interrupt Output. Connect the nINT pin to a logic rail through 10kΩ resistor. The nINT pin sends an active low, 256μs pulse to host to report charger device status and fault
NC	8	No Connect. Keep the pin float
nCE	9	Charge disable control pin. nCE = 0, charge is enabled. nCE = 1, charge is disabled
NC	10	No Connect. Keep the pin float
TS	11	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from LDO to TS to GND. Charge suspends when either TS pin is out of range. When TS pin is not used, connect a 10kΩ resistor from LDO to TS and connect a 10kΩ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor
nQON	12	BATFET enable/reset control input. When BATFET is in ship mode, a logic low of $t_{SHIPMODE}$ (typical 1.15s) duration turns on BATFET to exit shipping mode. When V_{BUS} is not plugged-in, a logic low of t_{QON_RST} (minimum 8s) duration resets SYS (system power) by turning BATFET off for t_{BATFET_RST} (minimum 250ms) and then re-enable BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic

PIN NAME	PIN #	DESCRIPTION
BAT	13, 14	Positive battery terminal. The internal BATFET and current sensing is connected between SYS and BAT. Connect a 10μF close to the BAT pin
SYS	15, 16	Converter output connection point. The internal current sensing network is connected between SYS and BAT pin. Connect 2 x10μF close to the SYS pin
GND	17, 18	Power Ground
SW	19, 20	Switching node output . Connected to output inductor. Connect the 10nF bootstrap capacitor from SW pin to BST pin
BST	21	Bootstrap capacitor connection for the high-side FET gate driver. Connect a 10nF ceramic capacitor from BST pin to SW pin
LDO	22	LDO Output Voltage. Bypass the pin with 4.7μF (10V rating) capacitor from LDO to GND. The capacitor should be closed to the pin
PMID	23	Connection point between reverse blocking FET and high-side switching FET. Bypass it with 2 x10μF capacitor from PMID to PGND. This capacitor should be close to the PMID pin

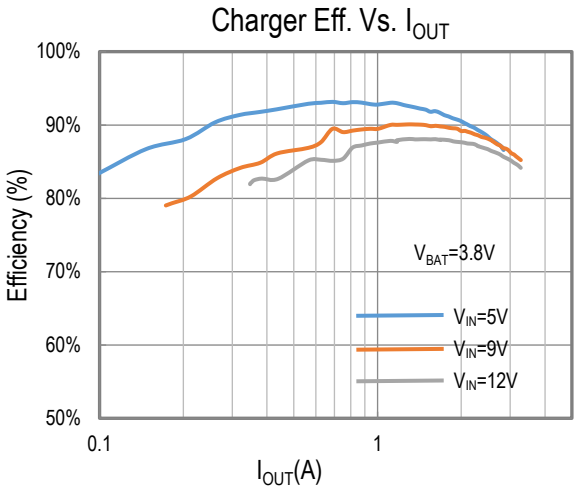
TYPICAL PERFORMANCE CHARACTERISTICS

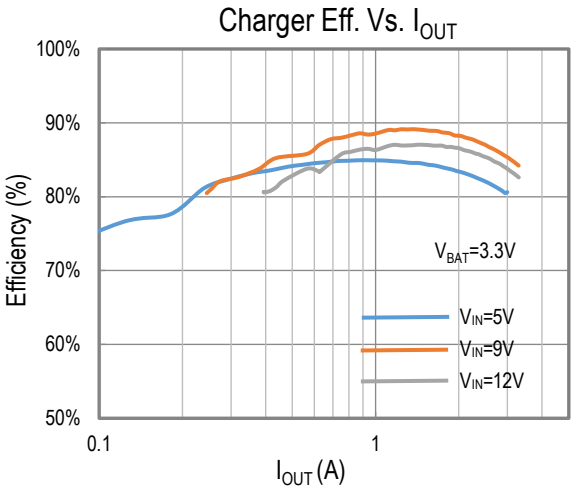
(Typical values are at T_A = 25°C unless otherwise specified.)

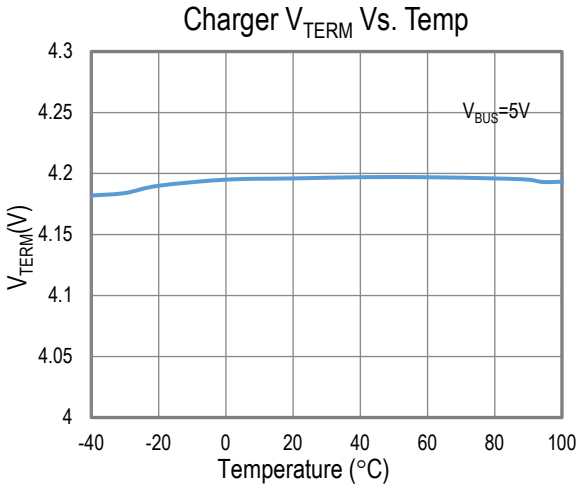


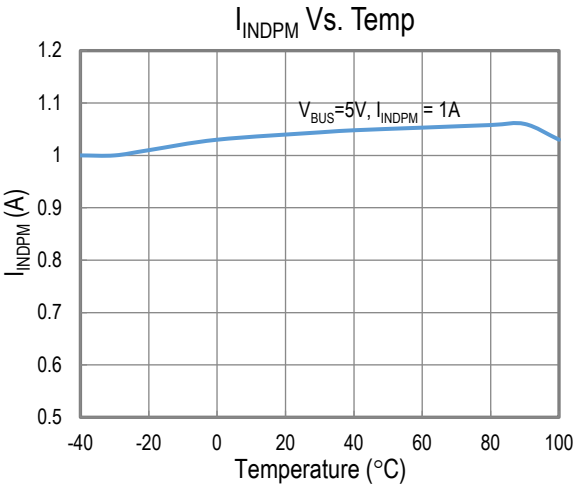


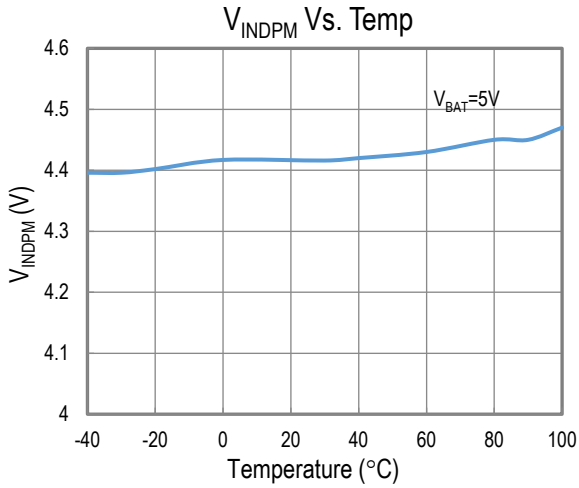
TYPICAL PERFORMANCE CHARACTERISTICS cont'

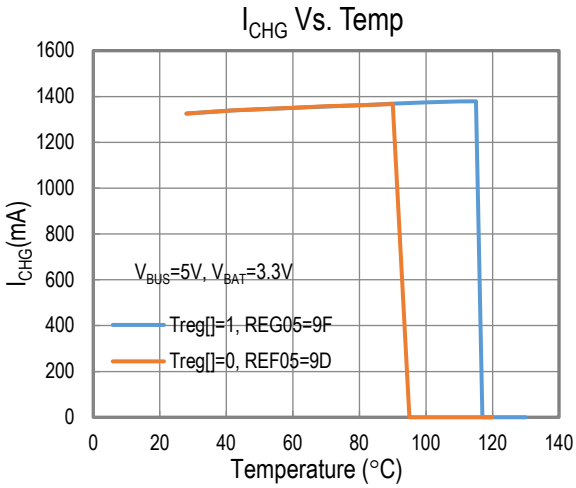












FUNCTION DESCRIPTION

ETA6963 device is a highly integrated 3A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It includes the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate drive

POWER UP FROM BATTERY WITHOUT INPUT SOURCE

When a battery is applied without other input, the device checks the battery voltage to turn on BATFET but not V_{LDO} to minimize the supply current, especially for NTC resistor network. All supply will be directly from battery. V_{LDO} is disabled until BOOST is enabled. Anyway, in order to optimize the discharge current from battery at light load, BATFET gate charge pump operates with lower frequency.

POWER UP WITH INPUT SOURCE

When an input source is plugged in, the device checks the input source voltage to turn on LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1.Power up V_{LDO}
2.Poor Source Qualification
3.Input Source Type Detection is based on D+/D– to set default input current limit (I_{INDPM}) register or input source type.
4.Input Voltage Limit Threshold Setting (V_{INDPM} threshold)
5.Converter Power-up

LDO POWER UP

V_{LDO} is enabled when the below conditions are met:

1. V_{BUS} is above 3.65V
2. V_{BUS} is above V_{BAT} + V_{SLEEP} (200mV)in Buck mode or V_{BUS} below V_{BAT} + V_{SLEEP} in Boost mode

Right after two above conditions are valid, LDO is powered up right away

POWER SOURCE QUALIFICATION

After LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to start the buck converter.

1. 200mS delay after LDO enable
2. V_{BUS} below the V_{BUS_OVP} threshold
3. V_{BUS} above 3.8V when pulling down 30mA at BUS pin

If the device fails the poor source detection in 30ms, it repeats poor source qualification every 2 seconds. Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the nINT pin is pulsed to signal to the host.

INPUT SOURCE TYPE DETECTION

After the VBUS_GD bit is set, the device will run input source detection through the DP/DM lines. The ETA6963 follows the USB Battery Charging Specification (BC1.2) to detect input source (SDP/CDP/DCP) and non-standard adapter through USB DP/DM lines, And after input type detection is completed, Input current limit register is changed

to set current limit, VBUS_STAT bits are updated.

The host can over-write IINDPM register to change the input current limit if needed. The charger input current is always limited by the IINDPM register.

DP/DM DETECTION SETS INPUT CURRENT LIMIT

The ETA6963 contains a DP/DM based input source detection to set the input current limit at V_{BUS} plug-in. The DP/DM detection includes standard USB BC1.2 and non-standard adapter. When input source is plugged in, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP) and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer expires, the non-standard adapter detection is applied to set the input current limit. The non-standard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the DP/DM pins. Base on DP/DM configuration, the input current limit will be set following the below table:

Table 1: Non-standard Adapter Detection

NON-STANDARD ADAPTER	DP THRESHOLD	DM THRESHOLD	INPUT CURRENT LIMIT (A)
Divider1	V_{DP} within V2P7_VTH	V_{DM} within V2P0_VTH	2.1
Divider2	V_{DP} within V1P2_VTH	V_{DM} within V1P2_VTH	2
Divider3	V_{DP} within V2P0_VTH	V_{DM} within V2P7_VTH	1
Divider4	V_{DP} within V2P7_VTH	V_{DM} within V2P7_VTH	2.4

Table 2: Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (A)
USB SDP	0.5
USB CDP	1.5
USB DCP	2.4
Divider1	2.1
Divider2	2
Divider3	1
Divider4	2.4
Unknown Adapter	0.5

BUCK POWER UP

After the input current is set, the device starts Buck converter and allow HSFET and LSFET switching. The ETA6963 provide soft-start time, V_{SYS} short protection to avoid overshoot current. When switching is over the soft-start time, the BATFET starts turning on then allows charging progress.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current limit is set to the lower of 200 mA or IINDPM register setting. After the system rises above 2.2 V, the device limits input current to the value of IINDPM register. As a battery charger, the device deploys a highly efficient 1.5 MHz

step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

In order to improve light load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the voltage ratio of SYS and BUS. The PFM_DIS bit can be used to prevent PFM operation in either buck or boost configuration.

BOOST POWER UP

ETA6963 provide boost converter up to 1.2A output current. The boost is enabled when the below conditions are valid:

1. V_{BAT} above the battery voltage exiting boost mode threshold
2. V_{BUS} is less than V_{BAT}+V_{SLEEP} (200mV)
3. OTG_CONFIG bit=1
4. TS pin is within acceptable range (V_{BHOT}<V_{TS}<V_{BCOLD})

During boost mode, the status register VBUS_STAT bits is set to 111, the BUS output voltage is 5.15 V by default and 1.5MHz Frequency. The output current can reach up to 1.2 A, selected through I2C (BOOST_LIM bit). The boost output is maintained when V_{BAT} is above V_{OTG_BAT} threshold. When OTG is enabled, the device starts up with PFM and later transits to PWM to minimize the overshoot. The PFM_DIS bit can be used to prevent PFM operation in either buck or boost configuration.

HOST MODE AND DEFAULT MODE

The ETA6963 is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG_FAULT bit is logic high. When the charger is in host mode, WATCHDOG_FAULT bit is logic low.

After power-on-reset, the device starts in default mode with watchdog timer expired or default mode. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 10 hours fast charging safety timer. At the end of the 10 hours, the charging is stopped and the buck converter continues to operate to supply system load.

Writing a ‘1’ to the WD_RST bit transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing ‘1’ to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set) or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer expires (WATCHDOG_FAULT bit = 1), the device returns to default mode and all registers are reset to default values except IINDPM, VINDPM, BATFET_DLY, BATFET_DIS, EN_ICHG_MON, PFM_DIS, SYS_Min, Min_VBAT_SEL, Q1_FULLON, OVP, BOOSTV, VDPM_BAT_TRACK, and VINDPM_INT_MASK bits.

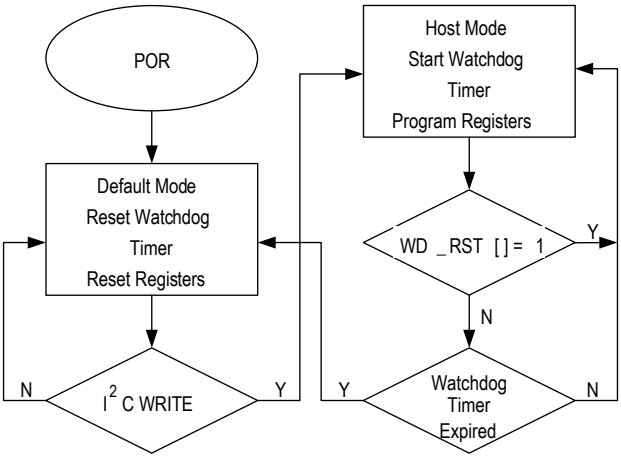


Figure 1: Watchdog Timer Flow Chart

AUTONOMOUS BATTERY CHARGER

The device charges 1cell Li-Ion battery with up to 3A charge current for high capacity tablet battery. The 27mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

With battery charging is enabled (CHG_CONFIG = 1 and nCE pin is LOW), the device autonomously completes a charging cycle without host involvement. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I²C.

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled (CHG_CONFIG bit = 1 and ICHG register is not 0 mA and CE is low)
- No thermistor fault on TS
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit = 0)

Table 3: Charging Parameter Default Setting

Default Mode	ETA6963
Charging Voltage	4.2V
Charging Current	2.048A
Pre-charge Current	180mA
Termination Current	180mA
Temperature Profile	JEITA
Safety Timer	10 hours

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device not is in DPM mode or thermal regulation.

When a full battery voltage is discharged below recharge threshold (selectable through VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, toggle nCE pin or CHG_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting EN_ICHG_MON bits = 11. In addition, the status register (CHRG_STAT) indicates the different charging phases:

- 00-charging disable
- 01-precharge
- 10-fast charge (constant current) and constant voltage mode
- 11-charging done

Once a charging cycle is completed, an INT pulse is asserted to notify the host.

BATTERY CHARGER PROFILE

The device charges the battery in five phases: battery short, pre-conditioning, constant current, constant voltage and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. in this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

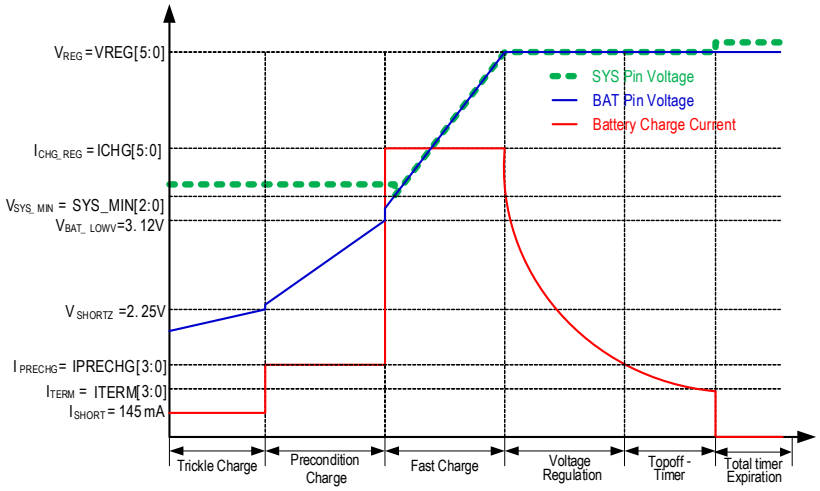


Figure 2: Battery Charger Profile

CHARGE TERMINATION CONFIGURATION

When battery voltage reach regulation level set by VREG[4:0], the device allow charger enter termination if EN_TERM[ ] = 1. In this state, when charge current falls below I_{TERM} level, charger will be terminated after T_{TOPOFF}. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

When termination occurs, the status register CHRG_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents, due to the comparator offset, the actual termination current may be higher than the termination target. In order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The termination timer will follow safety timer constraints, such that if safety timer is suspended, so will the termination timer. Similarly, if safety timer is doubled, so will the termination timer.

TOPOFF_ACTIVE bit reports whether the top off timer is active or not. The host can read CHRG_STAT and TOPOFF_ACTIVE to find out the termination status.

Top off timer gets reset at one of the following conditions:

- Charge disable to enable
- Termination status low to high
- REG_RST register bit is set

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination will have no effect unless a recharge cycle is initiated. An INT pulse is asserted to the host when entering top-off timer segment as well as when top-off timer expires.

CHARGE SAFETY TIMER

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below V_{BATLOW} threshold. The user can program fast charge safety timer through I^2C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an INT pulse is asserted to the host. The safety timer feature can be disabled through I^2C by setting EN_TIMER bit.

During input voltage, current, JEITA cool or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM_STAT = 1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X_EN bit.

During the fault, timer is suspended. Once the fault goes away, fault resumes. If user stops the current charging cycle, and start again, timer gets reset (toggle nCE pin or CHRG_CONFIG bit).

MINIMUM SYS VOLTAGE

Because the rail that provide power to system is SYS voltage, so to make sure the system always has enough voltage, ETA6963 provide minimum SYS voltage selection. The minimum system voltage is set by SYS_MIN[2:0] bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5 V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET.

When the battery charging is disabled and above minimum system voltage setting or charging is terminated, the system is always regulated at typically 70mV above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

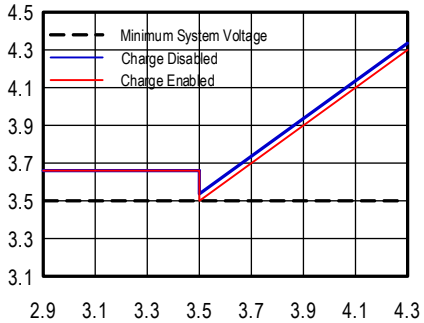


Figure 3: System Voltage vs Battery Voltage

DYNAMIC POWER MANAGEMENT

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (I_{INDPM}) or the voltage falls below the input voltage limit (V_{INDPM}). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VDPM_STAT (V_{INDPM}) or IDPM_STAT (I_{INDPM}) goes high.

SUPPLEMENT MODE

When the system voltage falls 10 mV ($V_{BAT} > V_{SYSMIN}$ when Q4 is full on. In this condition, discharge current is almost 1A.) or 20mV ($V_{BAT} < V_{SYSMIN}$ when Q4 is in regulation. In this condition, gate of Q4 is regulated at about only threshold voltage of the FET, then discharge current is almost zero.) below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET V_{DS} stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

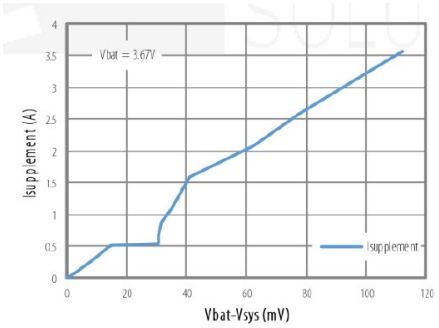


Figure 4: BATFET Current at Entering Supplement Mode

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce RDSON until the BATFET is in full conduction. At this point onwards, the BATFET VDS linearly increases with discharge current. Following figure shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

SHIPPING MODE AND nQON PIN

BATFET DISALBE MODE (SHIPPING MODE)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configured by BATFET_DLY bit.

BATFET ENABLE (EXIT SHIPPING MODE)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. Clear BATFET_DIS bit
3. Set REG_RST bit to reset all registers including BATFET_DIS bit to default (0)

4. A logic high to low transition on nQON pin with $t_{SHIPMODE}$ deglitch time (1.15s typical) to enable BATFET to exit shipping mode

BATFET FULL SYSTEM RESET

The BATFET functions as a load switch between battery and system when input source is not plugged-in. By changing the state of BATFET from on to off, systems connected to SYS can be effectively forced to have a power-on-reset. The nQON pin supports push-button interface to reset system power without host by changing the state of BATFET.

When the QON pin is driven to logic low for t_{QON_RST} while input source is not plugged in and BATFET is enabled (BATFET_DIS = 0), the BATFET is turned off for t_{BATFET_RST} and then it is re-enabled to reset system power. This function can be disabled by setting BATFET_RST_EN bit to 0.

nQON PIN OPERATION

Internally, there is a 500K pull up resistor from nQON pin to V_{DD}(maximum of V_{BAT} and V_{LDO}).So default, nQON will be high. Then nQON logic low and high voltage threshold are 0.68V and 0.88V respectively. The nQON pin incorporates two functions to control BATFET.

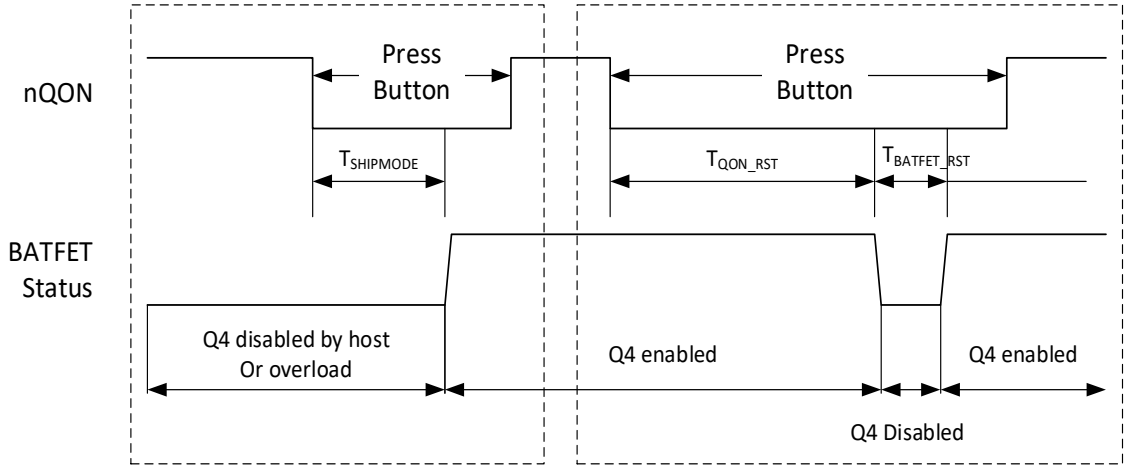
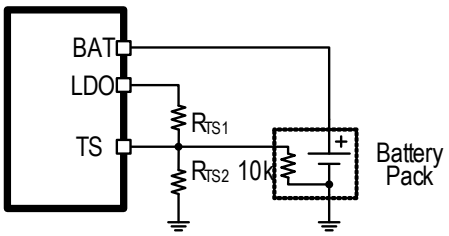


Figure 5: nQON Timing

1. BATFET Enable: A nQON logic transition from high to low with longer than $t_{SHIPMODE}$ deglitch turns on BATFET and exit shipping mode
2. BATFET Reset: When nQON is driven to logic low by at least t_{QON_RST} (12s typical) while adapter is not plugged in (and BATFET_DIS = 0), the BATFET is turned off for t_{BATFET_RST} (10s typical). The BATFET is re-enabled after t_{BATFET_RST} duration. This function allows systems connected to SYS to have power-on-reset. This function can be disabled by setting BATFET_RST_EN bit to 0.

THERMISTOR QUALIFICATION DURING CHARGING MODE

The charger device provides a single thermistor input for battery temperature monitor.



To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the V_{T1} to V_{T5} thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range. At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1V.

The charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3-T5) can be V_{REG} or 4.1V (configured by JEITA_VSET). The current setting at cool temperature (T1-T2) can be further reduced to 20% of fast charge current (JEITA_ISET).

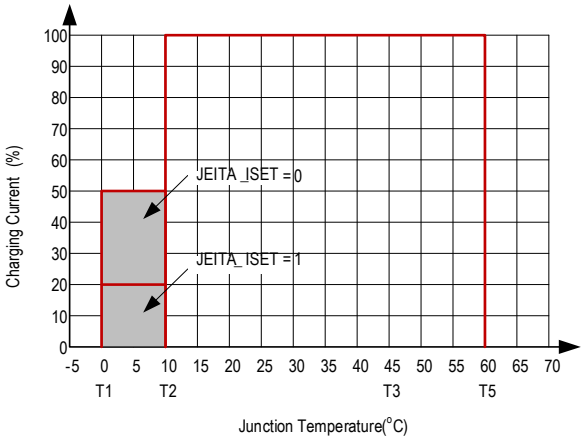


Figure 7: JEITA Profile: Charging Current

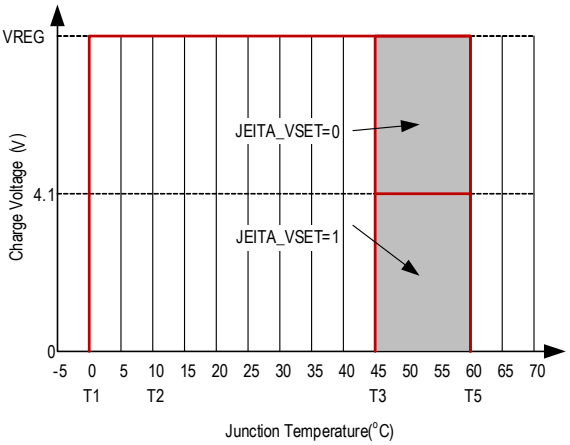


Figure 8: JEITA Profile: Charging Voltage

The resistor bias network has been updated as below.

$$R_{TS1}=\frac{\left(\frac{V_{LDO}}{V_{T1}}-1\right)}{\frac{1}{R_{TS2}}+\frac{1}{R_{TH_{COLD}}}} \qquad R_{TS2}=\frac{V_{LDO}\times R_{TH_{COLD}}\times R_{TH_{HOT}}\times\left(\frac{1}{V_{T1}}-\frac{1}{V_{T5}}\right)}{R_{TH_{HOT}}\times\left(\frac{V_{LDO}}{V_{T5}}-1\right)-R_{TH_{COLD}}\times\left(\frac{V_{LDO}}{V_{T1}}-1\right)}$$

THERMISTOR QUALIFICATION DURING BATTERY DISCHARGE MODE

For battery protection during boost mode, the device monitors the battery temperature to be within the V_{BCOLD} to V_{BHOT} thresholds. When temperature is outside of the temperature thresholds, the boost mode is suspended. in additional, VBUS_STAT bits are set to 000 and NTC_FAULT is reported. Once temperature returns within thresholds, the boost mode is recovered and NTC_FAULT is cleared.

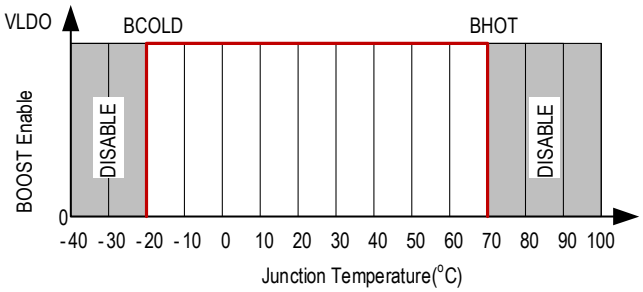


Figure 9: TS Pin Thermistor Sense Threshold in Boost

CHARGING STATUS INDICATION ON STAT PIN

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED. The STAT pin function can be disabled by setting the STAT_CONFIG[1:0] = 11. When STAT_CONFIG[1:0] = 00, STAT indication operates

as shown as in below table.

Table 4 STAT Indication table

CHARGE STATE	STAT INDICATION
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (input overvoltage, TS fault, timer fault or system overvoltage) Boost Mode suspend (due to TS fault)	Blinking at 1Hz (0.5s LOW / 0.5s HIZ)

HOST INTERRUPT ON nINT PIN

ETA6963 provides a comfortable feature that host does not need to always monitor the charger operation. The nINT pulse notifies the system on the device operation. The following events will generate 256μs INT pulse.

- USB/Adapter Source Detection (through DP/DM pins)
- BUS Pass Poor Source Detection
- Input removed
- Charge Complete
- Any FAULT event in REG09
- V_{INDPM} event detected. Masked by VINDPM_INT_ MASK = 1.
- I_{INDPM} event detected. Masked by IINDPM_INT_ MASK = 1.

When a fault occurs, the charger device sends out nINT and keeps the fault state in REG09 until the host reads the fault register. Before the host reads REG09 and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG09 two times consecutively. The first read reports the pre-existing fault register status and the second read reports the current fault register status.

INPUT OVERVOLTAGE PROTECTION IN CHARGE MODE (ACOV)

If V_{BUS} exceeds the V_{BUS} over voltage threshold V_{BUS_OV} (programmable via OVP[1:0] bits) the device stops switching immediately. During input overvoltage event, the fault register CHRG_FAULT bits are set to 01. An nINT pulse is asserted to the host. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold.

SYSTEM OVERVOLTAGE PROTOECTION IN CHARGE MODE (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 14% above system regulation voltage. Upon SYSOVP, converter stops immediately to clamp the overshoot.

BUS OUTPUT SHORT PROTECTION IN BOOST MODE

The device monitors boost output voltage and other conditions to provide output short circuit and overvoltage protection. The Boost build-in accurate constant current regulation to allow OTG to adaptive to various types of load. If short circuit is detected on V_{BUS}, the Boost turns off and retry 7 times. If retries are not successful, OTG is disabled with OTG_CONFIG bit cleared. In addition, the BOOST_FAULT bit is set and an nINT pulse is generated. The BOOST_FAULT bit can be cleared by host by re-enabling boost mode

BUS OVERVOLTAGE PROTECTION IN BOOST MODE

When the V_{BUS} rises above regulation target and exceeds the over voltage threshold V_{OTG_OVP}, the device enters overvoltage protection which stops switching, clears OTG_CONFIG bit and exits boost mode. At Boost overvoltage

duration, the fault register bit (BOOST_FAULT) is set high to indicate fault in boost operation. An nINT pulse is also asserted to the host.

THERMAL REGULATION IN BUCK MODE

The ETA6963 monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature at 110°C in buck mode. When the internal junction temperature exceeds thermal regulation limit (110°C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Thermal limit is programmable to 90°C by programming TREG bit.

THERMAL SHUTDOWN

The device monitors the internal junction temperature to provide thermal shutdown during any mode. When IC surface temperature exceeds T_{SHUT} (160°C) ,BATFET and Converter are disabled. OTG_CONFIG bit is cleared if in BOOST mode and BOOST_FAULT bit is set. In Charge mode, CHARGE_FAULT bit is set. An nINT pulse is asserted to the host.

When IC temperature is T_{SHUT_HYS} (30°C) below T_{SHUT} (160°C), The BATFET and charger are enabled following enable condition, Boost can be enabled by host.

BATTERY OVER-VOLTAGE PROTECTION

The battery overvoltage limit is clamped at 7% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register BAT_FAULT bit goes high and an nINT pulse is asserted to the host

BATTERY OVER-DISCHARGE PROTECTION

When battery is discharged below the battery depletion falling threshold $V_{BAT\_DPL\_FALL}$, the BATFET is turned off to protect battery from over discharge. To recover from over discharge, an input source is required at V_{BUS}. When an input source is plugged in, the BATFET turns on. The battery is charged with I_{SHORT} (typically 150 mA) current when the V_{BAT} is smaller than the trickle charge voltage threshold V_{SHORT}, or pre-charge current as set in I_{PRECHG} register when the battery voltage is between V_{SHORT} and the pre-charge voltage threshold V_{BAT_LOWV}.

SYSTEM OVER-CURRENT PROTECTION

When the system is shorted or significantly overloaded ($I_{BAT} > I_{BATOP}$) so that its current exceeds the overcurrent limit, the device latches off BATFET. Section BATFET Enable (Exit Shipping Mode) can reset the latch-off condition and turn on BATFET.

I²C COMMUNICATION

The device uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²C™ is a bi-directional 2 wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address D6H, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG0B. The I2C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits), connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

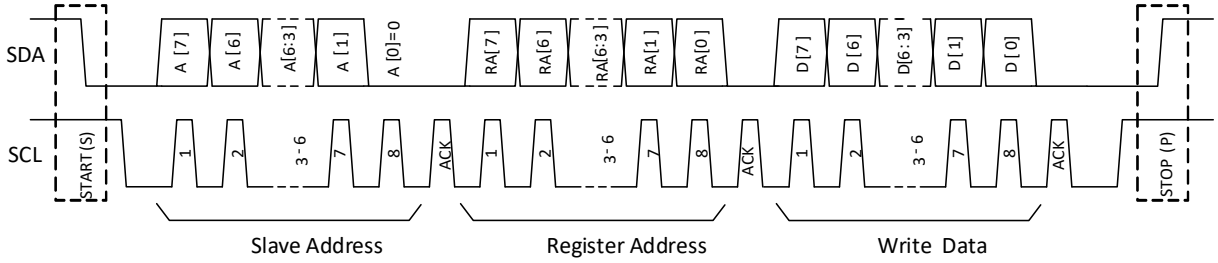


Figure 10: Single Write

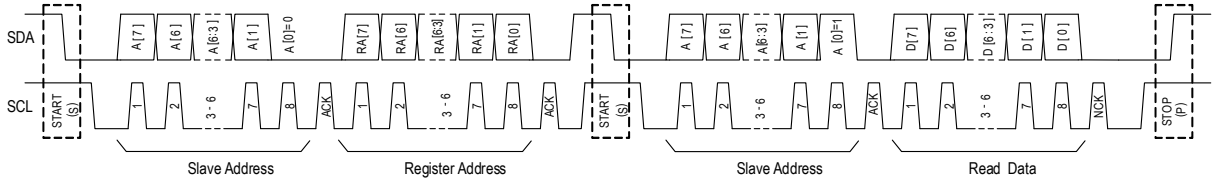


Figure 11: Single Read

Device address is understood value of A[7:0] while A[0] is “0”. This is also the address to write the data to the device registers. To read data from register, sending the command to address with A[0] is “1”. Register address are in RA[7:0]. Data to or from register are D[7:0].

REGISTER MAP

Table 5: REG00

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION	NOTE
7	EN_HIZ	0	R/W	by REG_RST by Watchdog	0-Disable, 1-Enable	Enable HIZ Mode 0-Disable (default) 1-Enable
6	EN_ICHG_MON[1]	0	R/W	by REG_RST	00 - Enable STAT pin function (default) 01 - Reserved 10 - Reserved 11 - Disable STAT pin function (float pin)	
5	EN_ICHG_MON[0]	0				
4	IINDPM[4]	1	R/W	by REG_RST	1600 mA	Input Current Limit Offset: 100 mA Range: 100 mA (000000) – 3.2 A (11111) Default:2400 mA (10111), maximum input current limit, not typical. IINDPM bits are changed automatically after input source detection is completed Host can over-write IINDPM register bits after input source detection is completed.
3	IINDPM[3]	0	R/W	by REG_RST	800 mA	
2	IINDPM[2]	1	R/W	by REG_RST	400 mA	
1	IINDPM[1]	1	R/W	by REG_RST	200 mA	
0	IINDPM[0]	1	R/W	by REG_RST	100 mA	

Table 6: REG01

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION	NOTE
7	PFM _DIS	0	R/W	by REG_RST	0 – Enable PFM 1 – Disable PFM	Default: 0 - Enable
6	WD_RST	0	R/W	by REG_RST by Watchdog	I²C Watchdog Timer Reset 0 –Normal; 1 – Reset	Default: Normal (0) Back to 0 after watchdog timer reset
5	OTG_CONFIG	0	R/W	by REG_RST by Watchdog	0 – OTG Disable 1 – OTG Enable	Default: OTG disable (0) Note: 1. OTG_CONFIG would over-ride Charge Enable Function in CHG_CONFIG

Table 6: REG01

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION	NOTE
4	CHG_CONFIG	1	R/W	by REG_RST by Watchdog	0 - Charge Disable 1- Charge Enable	Default: Charge Battery (1) Note: Charge is enabled when both CE pin is pulled low AND CHG_CONFIG bit is 1
3	SYS_Min[2]	1	R/W	by REG_RST	System Minimum Voltage	000: 2.6 V 001: 2.8 V 010: 3 V 011: 3.2 V 100: 3.4 V 101: 3.5 V 110: 3.6 V 111: 3.7 V Default: 3.5 V (101)
2	SYS_Min[1]	0	R/W	by REG_RST		
1	SYS_Min[0]	1	R/W	by REG_RST		
0	Min_VBAT_SEL	0	R/W	by REG_RST	0 – 2.8 V BAT falling, 1 – 2.5 V BAT falling	Minimum battery voltage for OTG mode. Default falling 2.8 V (0); Rising threshold 3.0 V (0)

Table 7: REG02

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION	NOTE
7	BOOST_LIM	1	R/W	by REG_RST by Watchdog	0 = 0.5 A 1 = 1.2 A	Default: 1.2 A (1) Note: The current limit options listed are minimum current limit specs.
6	Q1_FULLON	0	R/W	by REG_RST	0 – Use higher Q1 RDSON when programmed IINDPM < 700mA (better accuracy) 1 – Use lower Q1 RDSON always (better efficiency)	In boost mode, full FET is always used and this bit has no effect
5	ICHG[5]	1	R/W	by REG_RST by Watchdog	1920 mA	Fast Charge Current Default: 2040mA (100010) Range: 0 mA (0000000) – 3000mA (110010) Note: I_{CHG} = 0 mA disables charge. I_{CHG} > 3000 mA (110010) clamped to register value 3000 mA (110010)
4	ICHG[4]	0	R/W	by REG_RST by Watchdog	960 mA	
3	ICHG[3]	0	R/W	by REG_RST by Watchdog	480 mA	
2	ICHG[2]	0	R/W	by REG_RST by Watchdog	240mA	
1	ICHG[1]	1	R/W	by REG_RST by Watchdog	120mA	
0	ICHG[0]	0	R/W	by REG_RST by Watchdog	60mA	

Table 8: REG03

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION	NOTE
7	IPRECHG[3]	0	R/W	by REG_RST by Watchdog	480mA	Precharge Current Default: 180 mA (0010) Offset: 60 mA Note: I_{PRECHG} > 780 mA clamped to 780 mA (1100)
6	IPRECHG[2]	0	R/W	by REG_RST by Watchdog	240mA	
5	IPRECHG[1]	1	R/W	by REG_RST by Watchdog	120mA	
4	IPRECHG[0]	0	R/W	by REG_RST by Watchdog	60mA	
3	ITERM[3]	0	R/W	by REG_RST by Watchdog	480mA	Termination Current Default: 180 mA (0010) Offset: 60 mA
2	ITERM[2]	0	R/W	by REG_RST by Watchdog	240mA	
1	ITERM[1]	1	R/W	by REG_RST by Watchdog	120mA	
0	ITERM[0]	0	R/W	by REG_RST by Watchdog	60mA	

Table 9: REG04

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION	NOTE
7	VREG[4]	0	R/W	by REG_RST by Watchdog	512mV	Charge Voltage Offset: 3.848 V Range: 3.848 V to 4.616 V (11000) Default: 4.2 V (01011) Note: Value above 11000 is clamped to register value 11000 (4.616 V)
6	VREG[3]	1	R/W	by REG_RST by Watchdog	256mV	
5	VREG[2]	0	R/W	by REG_RST by Watchdog	128mV	
4	VREG[1]	1	R/W	by REG_RST by Watchdog	64mV	
3	VREG[0]	1	R/W	by REG_RST by Watchdog	32mV	
2	TOPOFF_TIMER[1]	0	R/W	by REG_RST by Watchdog	00 – Disabled (Default) 01 – 15 minutes 10 – 30 minutes 11 – 45 minutes	The extended time following the termination condition is met. When disabled, charge terminated when termination conditions are met.
1	TOPOFF_TIMER[0]	0	R/W	by REG_RST by Watchdog		
0	VRECHG	0	R/W	by REG_RST by Watchdog	0 – 120 mV 1 – 240 mV	Recharge threshold Default: 120mV

Table 10: REG05

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION	NOTE
7	EN_TERM	1	R/W	by REG_RST by Watchdog	0 – Disable 1 - Enable	Default: Enable termination (1)
6	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
5	WATCHDOG[1]	0	R/W	by REG_RST by Watchdog	00 – Disable timer 01 – 40s 10 – 80s 11 – 160s	Default: 40s (01)
4	WATCHDOG[0]	1	R/W	by REG_RST by Watchdog		
3	EN_TIMER	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable both fast charge and pre-charge timer	Default: Enable (1)
2	CHG_TIMER	1	R/W	by REG_RST by Watchdog	0 – 5 hrs 1 – 10 hrs	Default: 10 hours (1)
1	TREG	1	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold: 0 - 90°C 1 - 110°C	Default: 110°C (1)
0	JEITA_ISET (0°C-10°C)	1	R/W	by REG_RST by Watchdog	0 – 50% of ICHG 1 – 20% of ICHG	Default: 20% (1)

Table 11: REG06

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION	NOTE
7	OVP[1]	0	R/W	by REG_RST	Default: 6.5V (01)	V_{BUS_OVP} threshold: 00 - 5.5 V 01 – 6.5 V (5V input) 10 – 10.5 V (9V input) 11 – 14 V (12V input)
6	OVP[0]	1	R/W	by REG_RST		
5	BOOSTV[1]	1	R/W	by REG_RST	Default: 5.15V (10)	Boost Regulation Voltage: 00 - 4.85V 01 - 5.00V 10 - 5.15V 11 - 5.30V
4	BOOSTV[0]	0	R/W	by REG_RST		
3	VINDPM[3]	0	R/W	by REG_RST	800mV	Absolute VINDPM Threshold Offset: 3.9 V Range: 3.9 V (0000) – 5.4 V (1111) Default: 4.5V (0110)
2	VINDPM[2]	1	R/W	by REG_RST	400mV	
1	VINDPM[1]	1	R/W	by REG_RST	200mV	
0	VINDPM[0]	0	R/W	by REG_RST	100mV	

Table 12: REG07

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION	NOTE
7	IINDET_EN	0	R/W	by REG_RST by Watchdog	0 - Not in input current limit detection 1 - Force input current limit detection when VBUS is present	Returns to 0 after input detection is complete
6	TMR2X_EN	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Safety timer slowed by 2X during input DPM (both V and I) or JEITA cool, or thermal regulation	
5	BATFET_DIS	0	R/W	by REG_RST	0 – Allow Q4 turn on, 1 – Turn off Q4 with TBATFET_DLY delay time (REG07[3])	Default: Allow Q4 turn on (0)
4	JEITA_VSET (45°C-60°C)	0	R/W	by REG_RST by Watchdog	0 – Set Charge Voltage to 4.1V (max), 1 – Set Charge Voltage to VREG	
3	BATFET_DLY	1	R/W	by REG_RST	0 – Turn off BATFET immediately when BATFET_DIS bit is set 1 –Turn off BATFET after TBATFET_DLY (typ. 10s) when BATFET_DIS bit is set	Default: 1 Turn off BATFET after T_{BATFET_DLY} (typ. 10s) when BATFET_DIS bit is set
2	BATFET_RST _EN	1	R/W	by REG_RST by Watchdog	0 – Disable BATFET reset function 1 – Enable BATFET reset function	Default: 1 Enable BATFET reset function
1	VDPM_BAT_ TRACK[1]	0	R/W	by REG_RST	00 - Disable function (VINDPM set by register) 01 - V_{BAT} + 200mV 10 - V_{BAT} + 250mV 11 - V_{BAT} + 300mV	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of register value and V_{BAT} + $V_{DPM\_BAT\_TRACK}$
0	VDPM_BAT_ TRACK[0]	0	R/W	by REG_RST		

Table 13: REG08

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION
7	VBUS_STAT[2]	X	R	NA	V_{BUS} Status register 000: No input 001: USB Host SDP 010: USB CDP: (1.5A) 011: USB DCP (2.4 A) 101: Unknown Adapter (500 mA) 110: Non-Standard Adapter (1A/2A/2.1A/2.4A) 111: OTG Software current limit is reported in IINDPM register
6	VBUS_STAT[1]	X	R	NA	
5	VBUS_STAT[0]	X	R	NA	
4	CHRG_STAT[1]	X	R	NA	Charging status: 00 – Not Charging 01 – Pre-charge (< V_{BATLOW}) 10 – Fast Charging 11 – Charge Termination
3	CHRG_STAT[0]	X	R	NA	
2	PG_STAT	X	R	NA	Power Good status: 0 – Power Not Good 1 – Power Good
1	THERM_STAT	X	R	NA	0 – Not in thermal regulation 1 – in thermal regulation
0	VSYS_STAT	X	R	NA	0 – Not in V_{SYS_MIN} regulation (V_{BAT} > V_{SYS_MIN}) 1 – in V_{SYS_MIN} regulation (V_{BAT} < V_{SYS_MIN})

Table 14: REG09

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION
7	WATCHDOG_FAULT	X	R	NA	0 – Normal, 1- Watchdog timer expiration
6	BOOST_FAULT	X	R	NA	0 – Normal, 1 – V_{BUS} overloaded in OTG, or V_{BUS_OVP}, or battery is too low (any conditions that we cannot start boost function)
5	CHRG_FAULT[1]	X	R	NA	00 – Normal, 01 – input fault (V_{BUS_OVP} or V_{BAT} < V_{BUS} < 3.8 V) 10 -Thermal shutdown, 11 – Charge Safety Timer Expiration
4	CHRG_FAULT[0]	X	R	NA	
3	BAT_FAULT	X	R	NA	0 – Normal, 1 – BATOVP
2	NTC_FAULT[2]	X	R	NA	JEITA 000 – Normal, 010 – Warm, 011 – Cool, 101 – Cold, 110 – Hot (Buck mode) 000 – Normal, 101 – Cold, 110 – Hot (Boost mode)
1	NTC_FAULT[1]	X	R	NA	
0	NTC_FAULT[0]	X	R	NA	

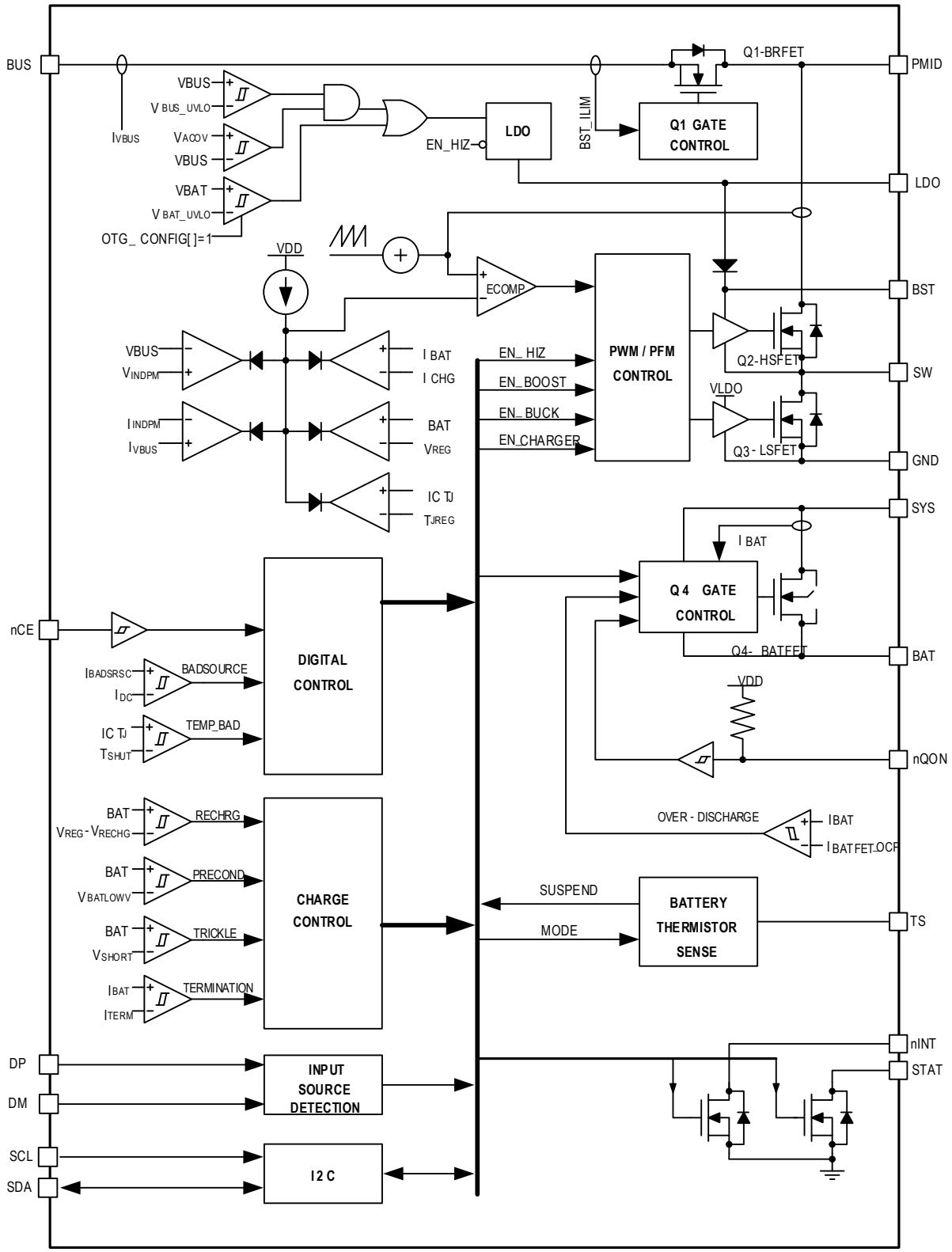
Table 15: REG0A

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION	
7	VBUS_GD	X	R	NA	0 – Not V_{BUS} attached	1 – V_{BUS} Attached
6	VINDPM_STAT	X	R	NA	0 – Not in VINDPM	1 – in VINDPM
5	IINDPM_STAT	X	R	NA	0 – Not in IINDPM	1 – in IINDPM
4	Reserved	X	R	NA	Reserved	Reserved
3	TOPOFF_ACTIVE	X	R	NA	0 – Top off timer not counting	1 – Top off timer counting
2	ACOV_STAT	X	R	NA	0 – Device is NOT in ACOV	1 – Device is in ACOV
1	VINDPM_INT_ MASK	0	R/W	by REG_RST	0 - Allow VINDPM INT pulse	1 - Mask VINDPM INT pulse
0	VINDPM_INT_ MASK	0	R/W	by REG_RST	0 - Allow IINDPM INT pulse	1 - Mask IINDPM INT pulse

Table 16: REG0B

BIT	NAME	POR	TYPE	RESET BY	DESCRIPTION
7	REG_RST	X	R/W	NA	Register reset 0 – Keep current register setting 1 – Reset to default register value and reset safety timer Note: Bit resets to 0 after register reset is completed
6	PIN[3]	0	R	NA	ETA6963: 0111
5	PIN[2]	1	R	NA	
4	PIN[1]	1	R	NA	
3	PIN[0]	1	R	NA	
2	ETA_PART ID	1	R	NA	ETA Part ID for recognition
1	DEV_REV[1]	X	R	NA	
0	DEV_REV[0]	X	R	NA	

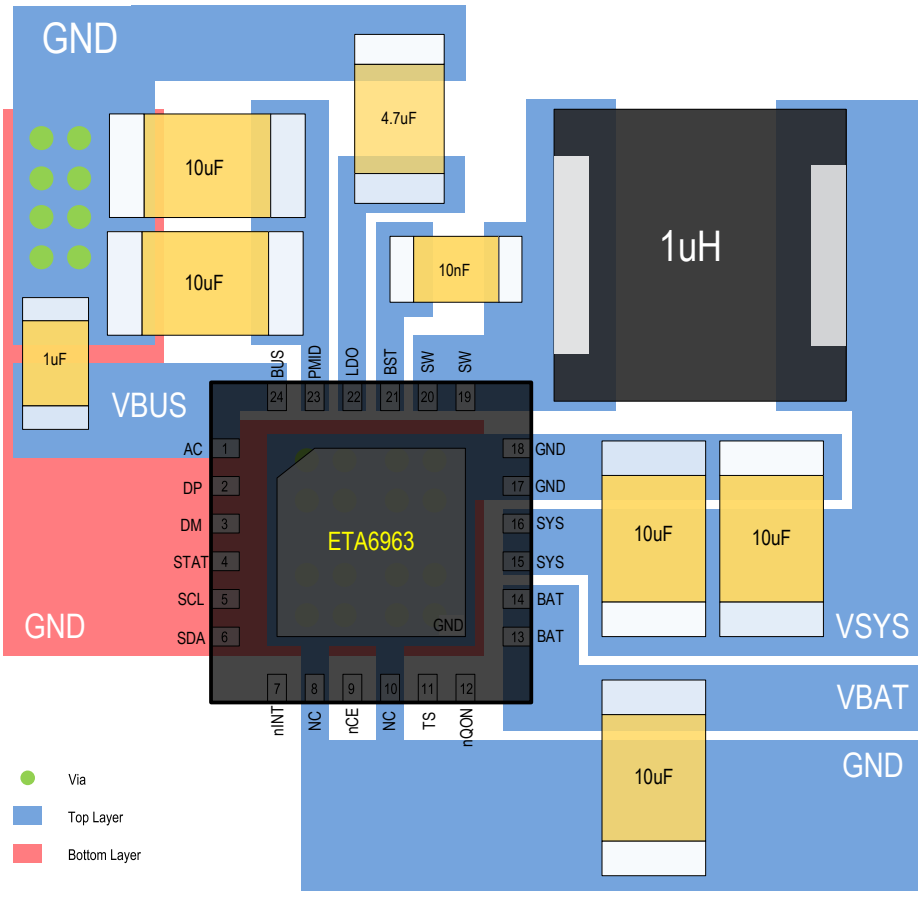
FUNCTION BLOCK DIAGRAM



PCB DESIGN GUIDELINE

In order to have as clean as possible supply for converter, please follow following suggestion:

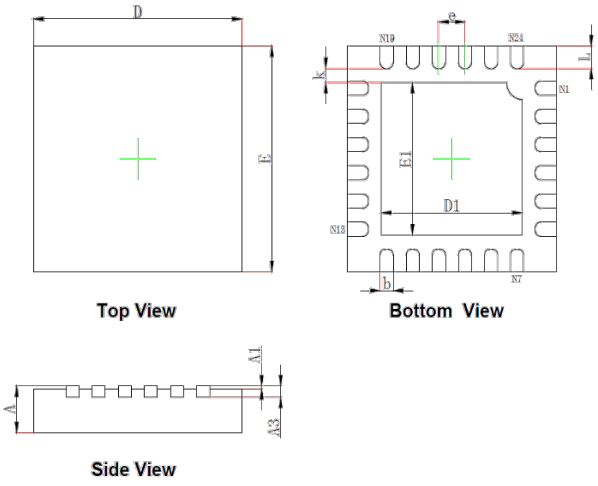
1. Place the BUS, PMID, BAT, SYS, LDO capacitor as close as possible to the pins and wide bottom layer for PGND connections. Also add as much as possible vias for PGND to minimize copper resistance added to PMID capacitor.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Use thermal pad as the single ground connection point.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Ensure that the number and sizes of vias allow enough copper for a given current path.
9. Ensure almost the bottom layer be ground unless bridge connection.



PACKAGE OUTLINE

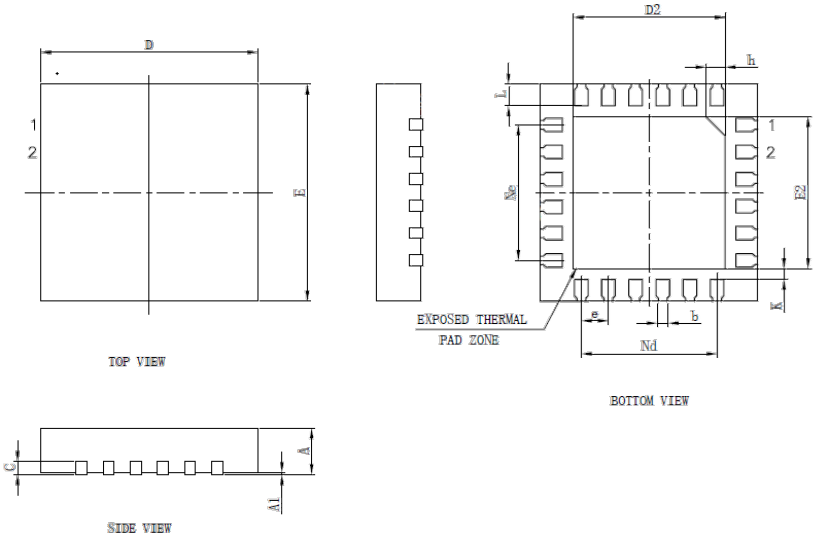
QFN4x4-24

From assembly house 1:



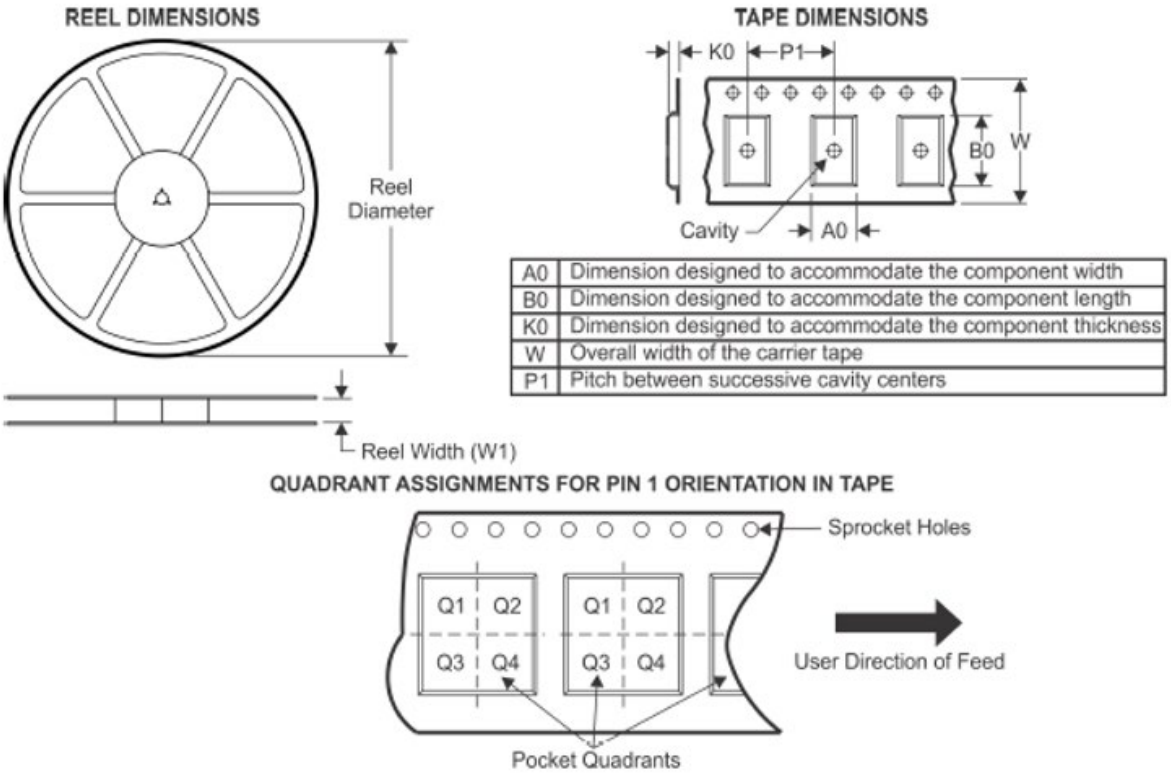
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

From assembly house 2:



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.85	0.90	0.95
	0.80	0.85	0.90
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.35	0.40	0.45
K	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸	2.9X2.9		

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA6963Q4Y	QFN4*4-24	24	5000	330	12.4	4.3	4.3	1.1	8	12	Q2