

## WD3133

### HIGH EFFICIENCY, 1.2-MHz DC-DC STEP-UP CONVERTERS

[Http://www.sh-willsemi.com](http://www.sh-willsemi.com)

#### Descriptions

The WD3133 is a high efficiency, high power, peak current mode step-up converter. Internal 0.35Ω HV power MOSFET with Min. 1A current limit. For portable device with Li-ion battery application, WD3133 could output typical 12V / 200mA ~300mA from 3.3V~5V input.

The boost converter WD3133 runs in Pulse-Width Modulation (PWM) mode, at 1.2MHz fixed switching frequency to reduce output ripple, improve conversion efficiency. It allows for the use of small external components. At light load currents the converter enters Skipping Mode to maintain a high efficiency over a wide load current range. The build-in soft start circuitry minimizes the inrush current at start-up.

The WD3133 is available in SOT-23-5L package. Standard product is Pb-free and Halogen-free.

#### Features

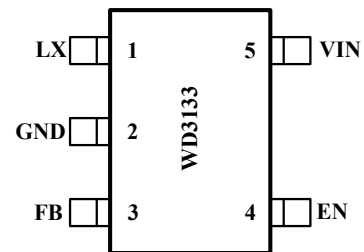
- Wide input voltage range from 2.7-V to 5.5-V
- 1.25-V (±2%) high accuracy reference voltage
- 1.2-MHz switching frequency
- Up to 93% efficiency
- Over 1-A (min.) power switch current limit
- Provide typical 12V / 200mA~300mA output from 3.3V~5V input
- Built-in Soft-Start

#### Applications

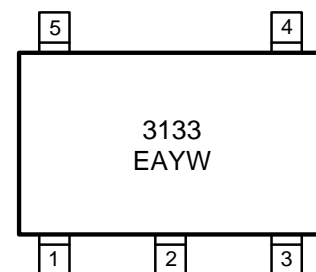
- Smart Phones
- Tablets
- Portable games
- PADs



SOT-23-5L



Pin configuration (Top view)



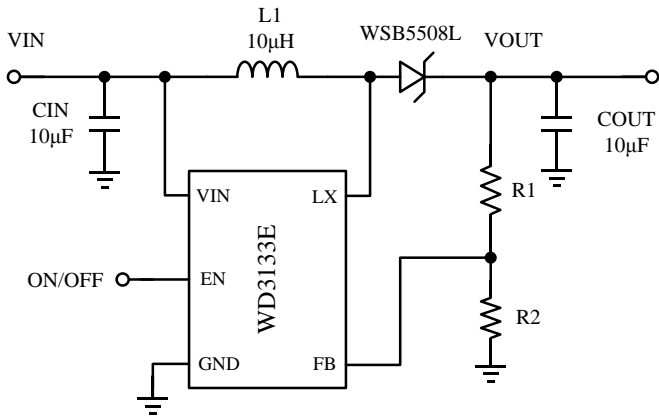
3133 = Device code  
 EA = Special code  
 Y = Year code  
 W = Week code

#### Marking

#### Order information

Device	Package	Shipping
WD3133E-5/TR	SOT-23-5L	3000/Reel&Tape

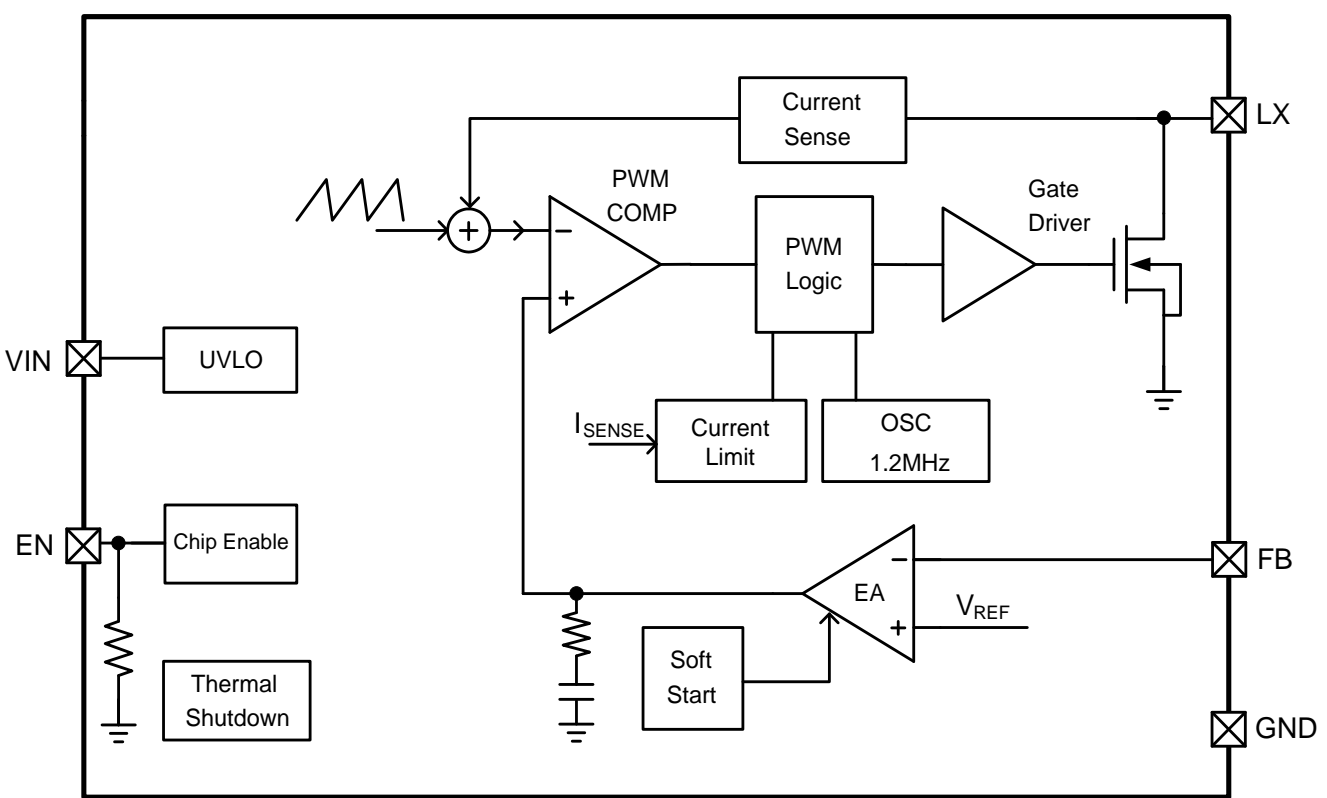
Typical applications



Pin descriptions

Symbol	SOT-23-5L	Descriptions
LX	1	Switch Node
GND	2	Ground
FB	3	Feedback
EN	4	Enable, Active High
VIN	5	Power Supply

Block diagram



### Absolute maximum ratings

Parameter	Symbol	Value	Unit
VIN pin voltage range	$V_{IN}$	-0.3~6.5	V
EN pin voltage range	-	-0.3~ $V_{IN}$	V
LX pin voltage range (DC)	-	-0.3~40	V
Power Dissipation – SOT-23-5L (Note 1)	$P_D$	0.5	W
Power Dissipation – SOT-23-5L (Note 2)		0.3	W
Junction to Ambient Thermal Resistance – SOT-23-5L (Note 1)	$R_{\theta JA}$	250	°C/W
Junction to Ambient Thermal Resistance – SOT-23-5L (Note 2)		416	°C/W
Junction temperature	$T_J$	150	°C
Lead temperature(Soldering, 10s)	$T_L$	260	°C
Operation temperature	$T_{opr}$	-40 ~ 85	°C
Storage temperature	$T_{stg}$	-55 ~ 150	°C

These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**Note 1:** Surface mounted on FR-4 Board using 1 square inch pad size, dual side, 1oz copper

**Note 2:** Surface mounted on FR-4 board using minimum pad size, 1oz copper

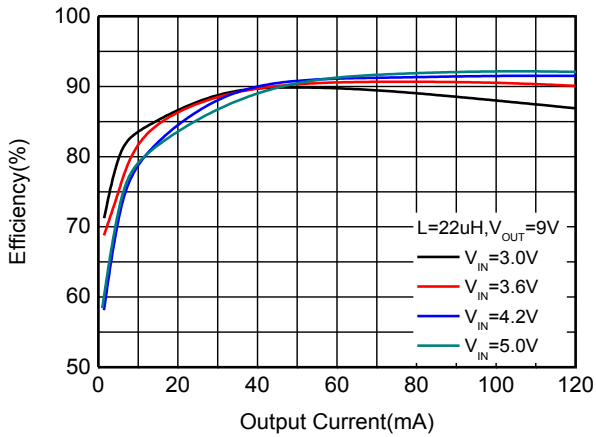
## Electronics Characteristics

( $T_a=25^\circ\text{C}$ ,  $V_{IN}=3.6\text{V}$ ,  $V_{EN}=V_{IN}$ ,  $C_{IN}=10\mu\text{F}$ ,  $C_{OUT}=10\mu\text{F}$ ,  $L=10\mu\text{H}$ , unless otherwise noted)

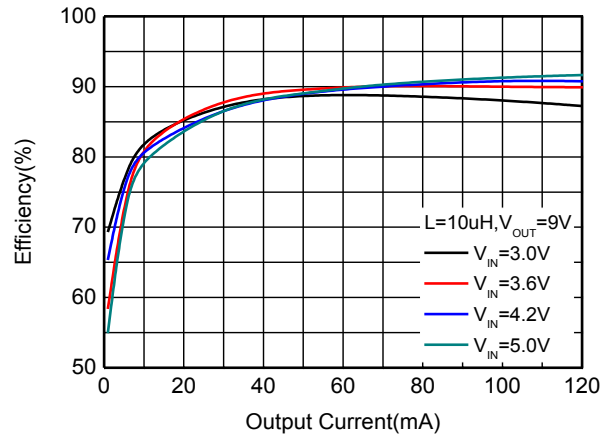
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Operation Voltage Range	$V_{IN}$		2.7	--	5.5	V
Under Voltage Lockout	$V_{UVLO}$	$V_{IN}$ Rising	1.8	2.2	2.5	V
UVLO Hysteresis	$V_{UVLO-HYS}$			0.1		V
Quiescent Current	$I_Q$	No Switching		0.3	1	mA
Supply Current	$I_S$	Switching		1.5	3	mA
Shutdown Current	$I_{SD}$	$V_{EN} < 0.4\text{V}$			1	$\mu\text{A}$
Operation Frequency	$f_{OSC}$		1.0	1.2	1.4	MHz
Maximum Duty Cycle	$D_{MAX}$		92			%
Feedback Reference	$V_{REF}$		1.225	1.25	1.275	V
On Resistance	$R_{ON}$	$I_{LX}=100\text{mA}$		0.35		$\Omega$
Current Limit	$I_{LIM}$		1	1.5		A
EN Threshold Voltage	$V_{ENL}$				0.4	V
	$V_{ENH}$		1.5			V
EN Pull Down Resistance	$R_{EN}$			1.5		$\text{M}\Omega$
Thermal Shutdown Temperature	$T_{SD}$			160		$^\circ\text{C}$
$T_{SD}$ Hysteresis	$T_{SD-HYS}$			30		$^\circ\text{C}$

**Typical Characteristics**

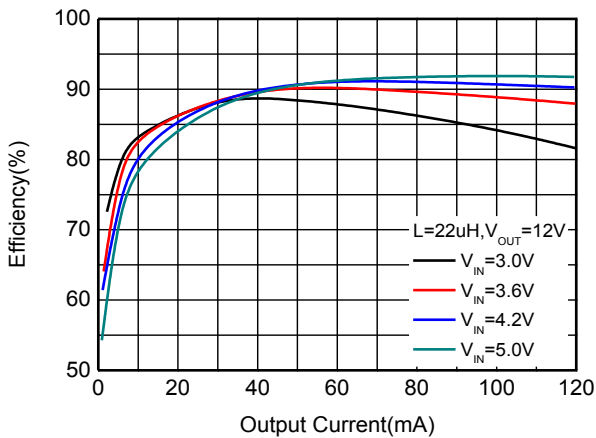
( $T_a=25^\circ\text{C}$ ,  $V_{IN}=3.6\text{V}$ ,  $V_{EN}=V_{IN}$ ,  $C_{IN}=10\mu\text{F}$ ,  $C_{OUT}=10\mu\text{F}$ ,  $L=10\mu\text{H}$ , unless otherwise noted)



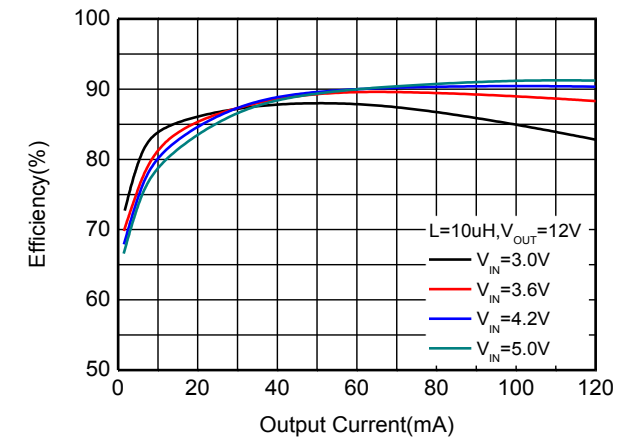
**Efficiency vs. Output Current**



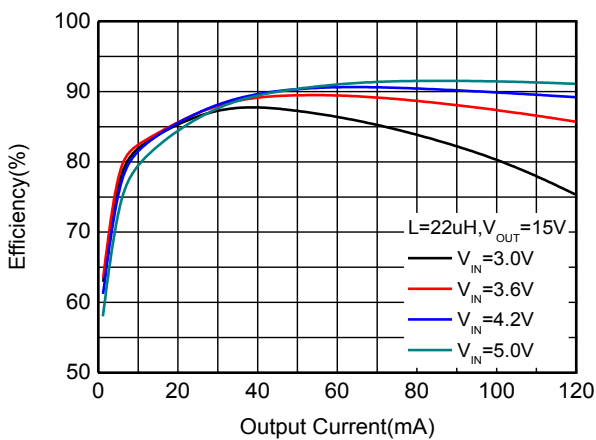
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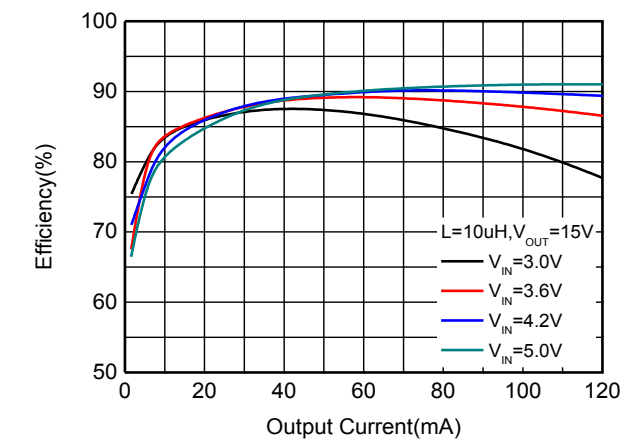
**Efficiency vs. Output Current**



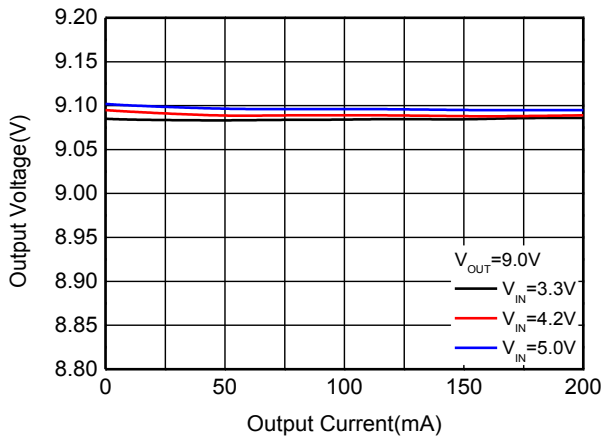
**Efficiency vs. Output Current**



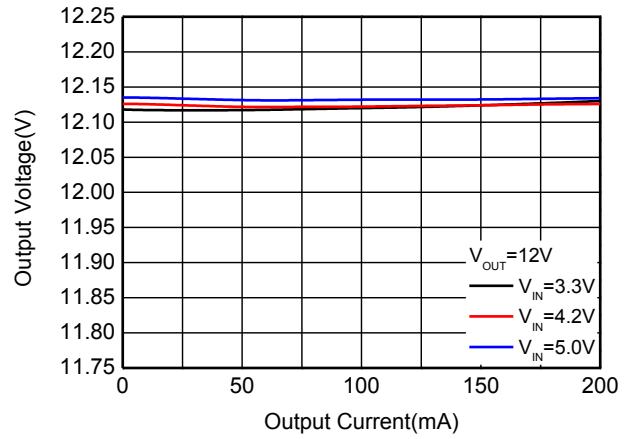
**Efficiency vs. Output Current**



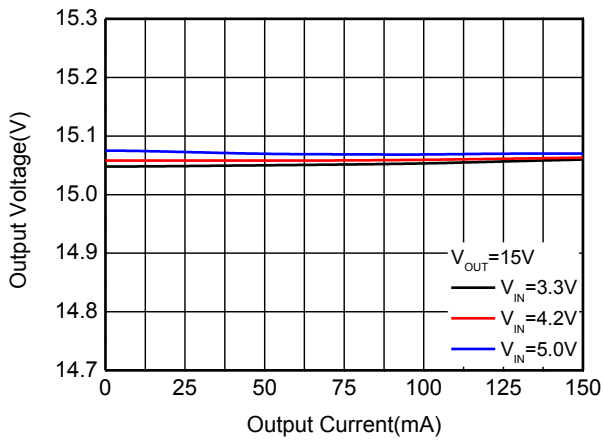
**Efficiency vs. Output Current**



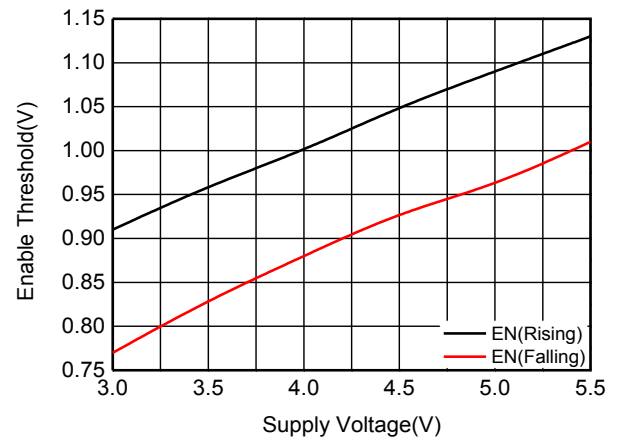
Output Voltage vs. Load Current



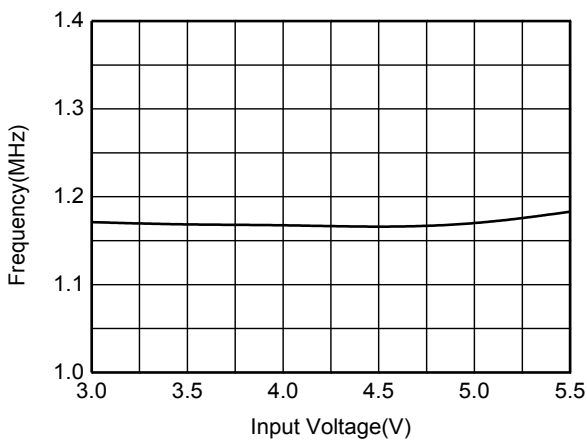
Output Voltage vs. Load Current



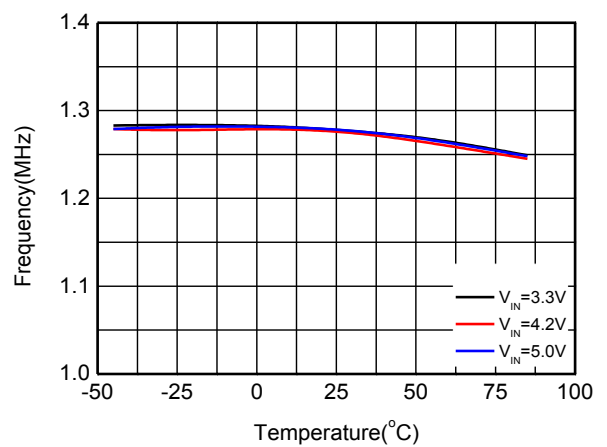
Output Voltage vs. Load Current



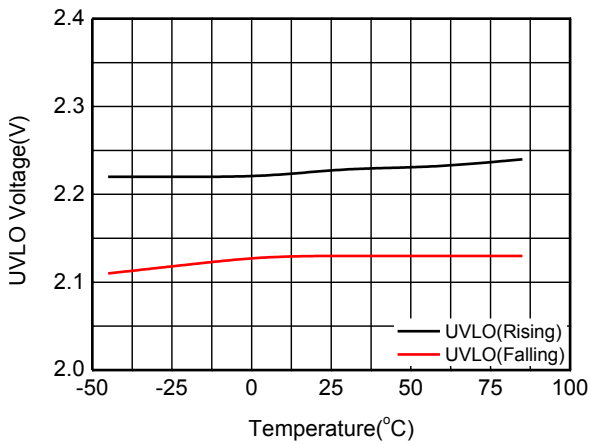
Enable Threshold vs. Supply Voltage



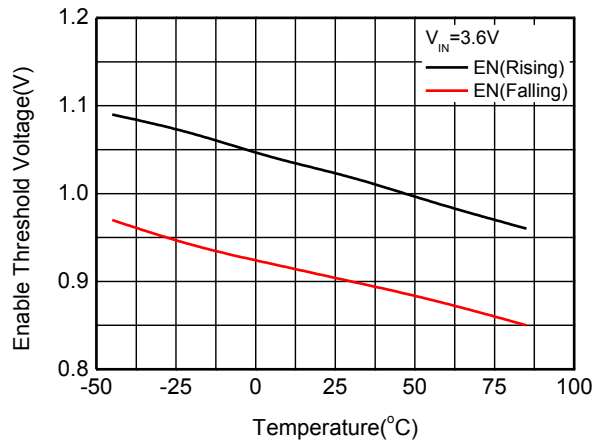
Operation Frequency vs. Supply Voltage



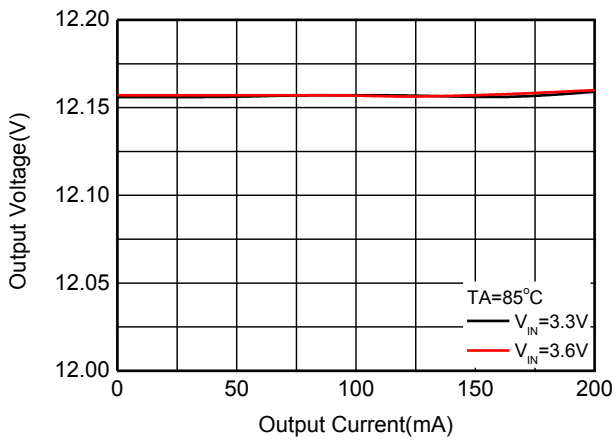
Operation Frequency vs. Temperature



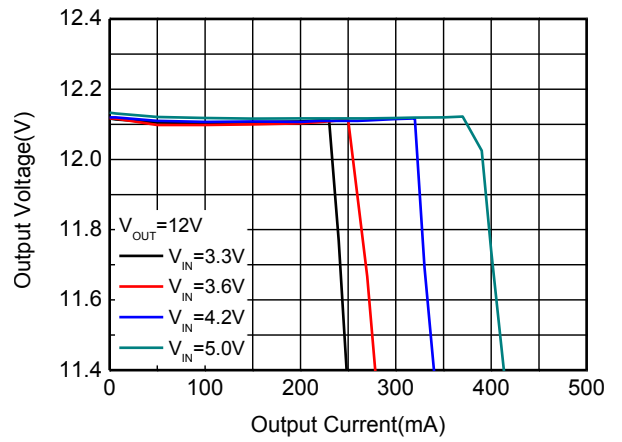
UVLO Threshold vs. Temperature



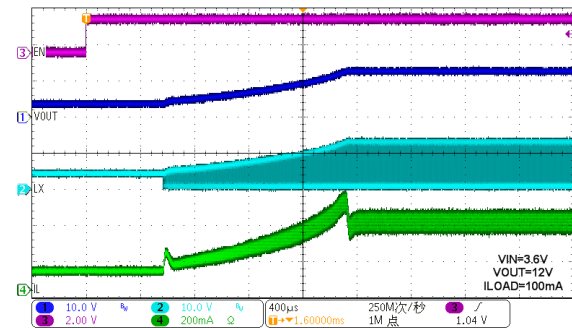
Enable Threshold vs. Temperature



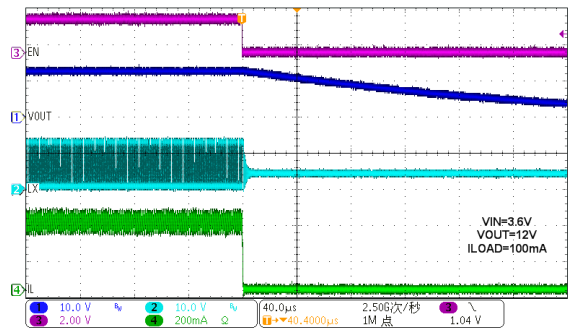
Load Regulation at TA=85°C



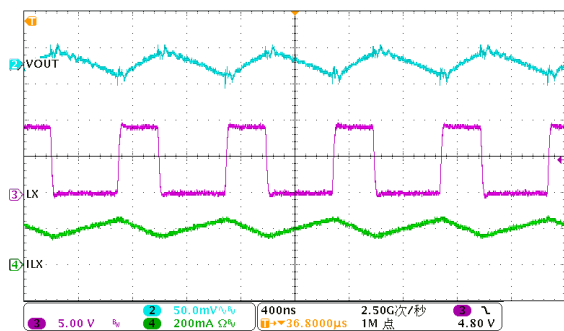
Output Current Capability



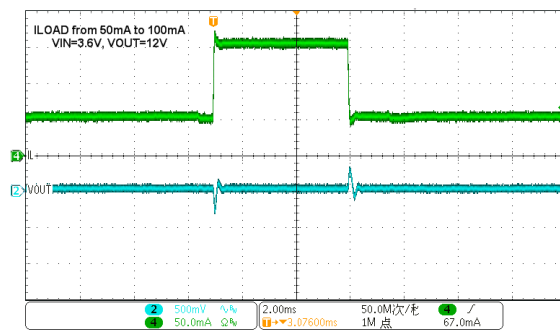
Start-up from EN



Shut-down from EN



Operation Waveforms



Load Transient Response



## Operation Information

### Normal Operation

The WD3133 is an adjustable voltage output, peak current mode controlled DC-DC boost converter. This means that switch duty cycle is directly controlled by the peak switch current rather than only by output voltage, with benefit of fast load transient response.

The WD3133 regulates the output voltage using a combined pulse-width (PWM) and pulse-skipping modulation topology. In PWM mode, the device runs at a 1.2MHz fixed frequency. Referring to the block diagram, the switch is turned ON at the start of each oscillator cycle. It is turned OFF when switch current reaches a predetermined level. The current trip level is set by using an error amplifier which senses the converter output voltage. The main switch current sensing voltage signal is summed by a slope compensation voltage signal. Slope compensation is necessary to prevent sub-harmonic oscillations that may occur in peak current mode architectures when exceeding 50% duty cycle. At very light loads, the WD3133 will automatically enter pulse skipping mode. When the converter output voltage is slightly higher than regulated voltage, the device will stop switching and skip some periods to maintain output regulation.

The WD3133 is highly integrated with a low on-resistance N-MOS switch, internal control-loop compensation network and soft-start circuitry. Additional features include Cycle-By-Cycle Current Limit Protection and Over Temperature Protection.

### Start-Up

The build-in soft-start function of WD3133 is implemented to suppress the inrush current to an acceptable value at the beginning of power on.

### Cycle by Cycle Current Limit

The WD3133 uses a cycle-by-cycle current limit circuitry to limit the inductor peak current in the event of an overload condition. The current flow

through inductor in charging phase is detected by a current sensing circuit. As the value comes across the current limiting threshold the N- MOSFET turns off, so that the inductor will be forced to leave charging stage and enter discharging stage. Therefore, the inductor current will not increase over the current limiting threshold.

### UVLO Protection

To avoid malfunction of the WD3133 at low input voltages, an under voltage lockout is included that disables the device, until the input voltage exceeds 2.2V (Typ.).

### Shutdown Mode

Drive EN to GND to place the WD3133 in shutdown mode. In shutdown mode, the reference, control circuit, and the main switch turn off. Input current falls to smaller than 1 $\mu$ A during shutdown mode.

### Over Temperature Protection (OTP)

As soon as the junction temperature ( $T_J$ ) exceeds 160°C (Typ.), the WD3133 goes into thermal shutdown. In this mode, the main N-MOSFET is turned off until temperature falls below typically 130°C. Then the device starts switching again.

## Application Information

External component selection for the application circuit depends on the load current requirements. Certain tradeoffs between different performance parameters can also be made.

### Boost Inductor Selection

A 4.7 $\mu$ H to 22 $\mu$ H inductor with low DCR and high saturation current is recommended. The minimum and maximum inductor values are constrained by many considerations. The minimum inductance is limited by the peak inductor-current value. The ripple current in the inductor is inversely proportional to the inductance value, so the output voltage may fall out of regulation if the peak inductor current exceeds the current-limit value (1A minimum). Using a nominal 10 $\mu$ H inductor allows full recommended current operation even if the inductance is 20% low due to component variation. However, for  $V_{OUT} > 30V$  applications, a 4.7 $\mu$ H inductor is recommended.

The saturation current of inductor should be higher enough than the peak switch current. And the inductor should have low core losses at 1.2MHz and low DCR (copper wire resistance).

### Input Capacitor Selection

Connect the input capacitance from VDD to the reference ground plane. Input capacitance reduces the ac voltage ripple on the input rail by providing a low-impedance path for the switching current of the boost converter. The WD3133 does not have a minimum or maximum input capacitance requirement for operation, but a 4.7 $\mu$ F~10 $\mu$ F, X7R or X5R ceramic capacitor is recommended for most applications for reasonable input-voltage ripple performance. There are several scenarios where it is recommended to use additional input capacitance.

### Output Capacitor Selection

Connect the boost-converter output capacitance from Output to the reference ground plane. The

Output capacitance controls the ripple voltage on the Output rail and provides a low-impedance path for the switching and transient-load currents of the boost converter. It also sets the location of the output pole in the control loop of the boost converter. There are limitations to the minimum and maximum capacitance on Output. The recommended minimum capacitor on Output is 4.7 $\mu$ F, X5R or X7R ceramic capacitor. For heavier load current, larger output capacitor should be selected. The low ESR of the ceramic capacitor minimizes ripple voltage and power dissipation from the large, pulsating currents of the boost converter and provides adequate phase margin across all recommended operating conditions. The allowed maximum operating voltage of output capacitor should be larger enough than  $V_{OUT}$ .

### Diode Selection

The rectifier diode supplies current path to the inductor when the internal MOSFET is off. Use a Schottky with low forward voltage to reduce losses. The diode should be rated for a reverse blocking voltage greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current.

Diode the following requirements:

- Low forward voltage
- High switching speed : 50ns max.
- Reverse voltage :  $> V_{OUT}$
- Rated current :  $I_{PK}$  or more

### PC Board Layout Considerations

A good circuit board layout aids in extracting the most performance from the WD3133. Poor circuit layout degrades the output ripple and the electromagnetic interference (EMI) or electromagnetic compatibility (EMC) performance. The evaluation board layout is optimized for the WD3133. Use this layout for best performance. If this layout needs changing, use the following guidelines:

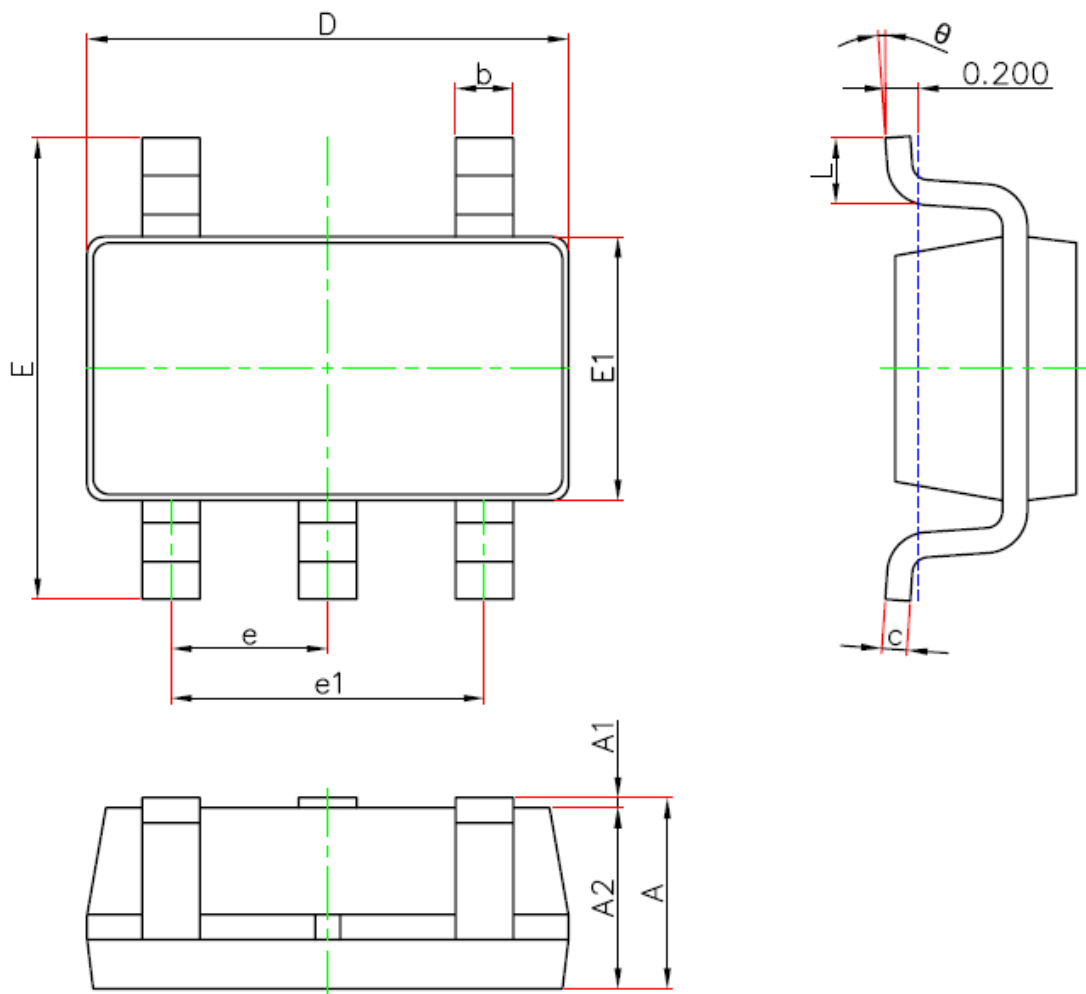
1. Use separate analog and power ground planes.

Connect the sensitive analog circuitry (such as voltage divider components) to analog ground. Connect the power components (such as input and output bypass capacitors) to power ground. Connect the two ground planes together near the load to reduce the effects of voltage dropped on circuit board traces.

2. Locate  $C_{IN}$  as close to the VDD pin as possible, and use separate input bypass capacitors for the analog.
3. Route the high current path from  $C_{IN}$ , through L to the LX and PGND pins as short as possible.
4. Keep high current traces as short and as wide as possible.
5. The output filter of the boost converter is also critical for layout. The Diode and Output capacitors should be placed to minimize the area of current loop through Output –PGND– LX.
6. Avoid routing high impedance traces, such as FB, near the high current traces and components or near the Diode node (D). If high impedance traces are routed near high current and/or the LX node, place a ground plane shield between the traces.

## Package outline dimensions

## SOT-23-5L



Symbol	Dimensions in millimeter		
	Min.	Typ.	Max.
A	1.050	-	1.250
A1	0.000	-	0.100
A2	1.050	-	1.150
b	0.300	-	0.500
c	0.100	-	0.200
D	2.820	-	3.020
E1	1.500	-	1.700
E	2.650	-	2.950
e	0.950(BSC)		
e1	1.800	-	2.000
L	0.300	-	0.600
$\theta$	0°	-	8°