SBAS457A – OCTOBER 2010 – REVISED JULY 2011

# Ultra-Small, Low-Power, SPI™-Compatible, 16-Bit Analog-to-Digital Converter and Temperature Sensor with Internal Reference

**Check for Samples: ADS1118**

## FEATURES

- **Ultra-Small QFN Package: 2mm × 1,5mm × 0,4mm**
- **Wide Supply Range: 2.0V to 5.5V**
- **Low Current Consumption:**
  - **Continuous Mode: Only 150μA**
  - **Single-Shot Mode: Auto Shutdown**
- **Programmable Data Rate: 8SPS to 860SPS**
- **Single-Cycle Settling**
- **Internal Low-Drift Voltage Reference**
- **Internal Temperature Sensor:**
  - **0.5°C Max Error**
- **Internal Oscillator**
- **Internal PGA**
- **Four Single-Ended or Two Differential Inputs**

## APPLICATIONS

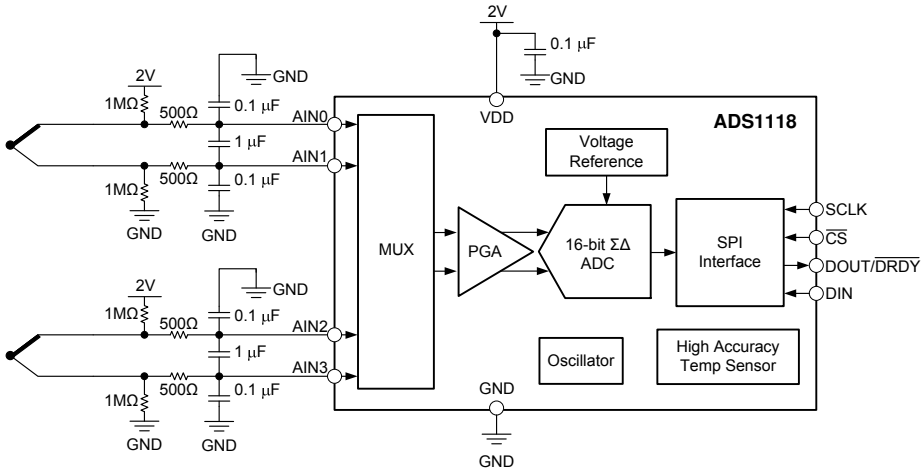
- **Temperature Measurement:**
  - **Thermocouple Measurement**
  - **Cold Junction Compensation**
  - **Thermistor Measurement**
- **Portable Instrumentation**
- **Factory Automation and Process Controls**

## DESCRIPTION

The ADS1118 is a precision analog-to-digital converter (ADC) with 16 bits of resolution offered in an ultra-small, leadless QFN-10 package or an MSOP-10 package. The ADS1118 is designed with precision, power, and ease of implementation in mind. The ADS1118 features an onboard reference and oscillator. Data are transferred via a serial peripheral interface (SPI). The ADS1118 operates from a single power supply ranging from 2V to 5.5V.

The ADS1118 can perform conversions at rates up to 860 samples per second (SPS). An onboard programmable gain amplifier (PGA) is available on the ADS1118 that offers input ranges from the supply to as low as ±256mV. This range allows both large and small signals to be measured with high resolution. The ADS1118 also features an input multiplexer (MUX) that provides two differential or four single-ended inputs. The ADS1118 can also function as a high-accuracy temperature sensor. This temperature sensor can be used for system-level temperature monitoring or cold junction compensation for thermocouples.

The ADS1118 operates either in continuous conversion mode or a single-shot mode that automatically powers down after a conversion. Single-shot mode significantly reduces current consumption during idle periods. The ADS1118 is specified from –40°C to +125°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

| | | ADS1118 | UNIT |
|---|---|---|---|
| VDD to GND | | –0.3 to +5.5 | V |
| Analog input current | | 100, momentary | mA |
| Analog input current | | 10, continuous | mA |
| Analog input voltage to GND | | –0.3 to VDD + 0.3 | V |
| DIN, DOUT/$\overline{\text{DRDY}}$, SCLK, $\overline{\text{CS}}$ voltage to GND | | –0.3 to +5.5 | V |
| ESD ratings | Human body model (HBM)<br>JEDEC standard 22, test method A114-C.01, all pins | ±4000 | V |
| | Charged device model (CDM)<br>JEDEC standard 22, test method C101, all pins | ±1000 | V |
| Operating temperature range | | –40 to +125 | °C |
| Maximum junction temperature | | +150 | °C |
| Storage temperature range | | –60 to +150 | °C |

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PRODUCT FAMILY

| DEVICE | RESOLUTION (Bits) | MAXIMUM SAMPLE RATE (SPS) | SPECIAL FEATURES | PGA | INTERFACE | INPUT CHANNELS (Differential/ Single-Ended) |
|---|---|---|---|---|---|---|
| ADS1118 | 16 | 860 | Temperature sensor | Yes | SPI | 2/4 |
| ADS1018 | 12 | 3300 | Temperature sensor | Yes | SPI | 2/4 |
| ADS1115 | 16 | 860 | Comparator | Yes | $I^2C$ | 2/4 |
| ADS1114 | 16 | 860 | Comparator | Yes | $I^2C$ | 1/1 |
| ADS1113 | 16 | 860 | None | No | $I^2C$ | 1/1 |
| ADS1015 | 12 | 3300 | Comparator | Yes | $I^2C$ | 2/4 |
| ADS1014 | 12 | 3300 | Comparator | Yes | $I^2C$ | 1/1 |
| ADS1013 | 12 | 3300 | None | No | $I^2C$ | 1/1 |

## ELECTRICAL CHARACTERISTICS

Maximum/minimum specifications at –40°C to +125°C, VDD = 3.3V, data rate = 8SPS, and full-scale (FS) = ±2.048V, unless otherwise noted. Typical values are at +25°C, VDD = 3.3V, data rate = 8SPS, and full-scale (FS) = ±2.048V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | ADS1118 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **ANALOG INPUT** | | | | | |
| Full-scale input voltage(1) | $V_{IN} = (AIN_P) – (AIN_N)$ | | ±4.096/PGA | | V |
| Analog input voltage | $AIN_P$ or $AIN_N$ to GND | GND | | VDD | V |
| Differential input impedance | | | See Table 1 | | |
| Common-mode input impedance | FS = ±6.144V(1) | | 8 | | MΩ |
| | FS = ±4.096V(1), ±2.048V | | 6 | | MΩ |
| | FS = ±1.024V | | 3 | | MΩ |
| | FS = ±0.512V, ±0.256V | | 100 | | MΩ |
| **SYSTEM PERFORMANCE** | | | | | |
| Resolution | No missing codes | 16 | | | Bits |
| Data rate (DR) | | 8, 16, 32, 64, 128, 250, 475, 860 | | | SPS |
| Data rate variation | All data rates | –10 | | 10 | % |
| Output noise | | See Typical Characteristics | | | |
| Integral nonlinearity | DR = 8SPS, FS = ±2.048V, best fit(2) | | | 1 | LSB |
| Offset error | FS = ±2.048V, differential inputs | | ±0.1 | ±2 | LSB |
| | FS = ±2.048V, single-ended inputs | | ±0.25 | | LSB |
| Offset drift | FS = ±2.048V | | 0.002 | | LSB/°C |
| Offset power-supply rejection | FS = ±2.048V, with dc supply variation | | 0.2 | | LSB/V |
| Gain error(3) | FS = ±2.048V at +25°C | | 0.01 | 0.15 | % |
| Gain drift(3)(4) | FS = ±0.256V | | 7 | | ppm/°C |
| | FS = ±2.048V | | 5 | 40 | ppm/°C |
| | FS = ±6.144V(1) | | 5 | | ppm/°C |
| Gain power-supply rejection | | | 10 | | ppm/V |
| PGA gain match(3) | Match between any two PGA gains | | 0.01 | 0.1 | % |
| Gain match | Match between any two inputs | | 0.01 | 0.1 | % |
| Offset match | Match between any two inputs | | 0.6 | | LSB |
| Common-mode rejection | At dc and FS = ±0.256V | | 105 | | dB |
| | At dc and FS = ±2.048V | | 100 | | dB |
| | At dc and FS = ±6.144V(1) | | 90 | | dB |
| | $f_{CM}$ = 60Hz, DR = 860SPS | | 105 | | dB |
| | $f_{CM}$ = 50Hz, DR = 860SPS | | 105 | | dB |
| **TEMPERATURE SENSOR** | | | | | |
| Temperature sensor range | | –40 | | +125 | °C |
| Temperature sensor resolution | | | 0.03125 | | °C/LSB |
| Temperature sensor accuracy | 0°C to +70°C | | 0.2 | ±0.5 | °C |
| | –40°C to +125°C | | 0.4 | ±1 | °C |
| | vs supply | | 0.03125 | ±0.25 | °C/V |

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than the smaller of VDD + 0.3V or 5.5V be applied to this device.
(2) Best fit INL covers 99% of full-scale.
(3) Includes all errors from onboard PGA and reference.
(4) Not production tested; ensured by characterization.

## ELECTRICAL CHARACTERISTICS (continued)

Maximum/minimum specifications at –40°C to +125°C, VDD = 3.3V, data rate = 8SPS, and full-scale (FS) = ±2.048V, unless otherwise noted. Typical values are at +25°C, VDD = 3.3V, data rate = 8SPS, and full-scale (FS) = ±2.048V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | ADS1118 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic level | | | | | |
| $V_{IH}$ | | 0.7VDD | | VDD | V |
| $V_{IL}$ | | GND | | 0.2VDD | V |
| $V_{OH}$ | $I_{OH}$ = 1mA | 0.8VDD | | | V |
| $V_{OL}$ | $I_{OL}$ = 1mA | GND | | 0.2VDD | V |
| Input leakage | | | | | |
| $I_H$ | $V_{IH}$ = 5.5V | | | ±10 | µA |
| $I_L$ | $V_{IL}$ = GND | | | ±10 | µA |
| **POWER-SUPPLY REQUIREMENTS** | | | | | |
| Power-supply voltage | | 2 | | 5.5 | V |
| Supply current | Power-down current at +25°C | | 0.5 | 2 | µA |
| | Power-down current up to +125°C | | | 5 | µA |
| | Operating current at +25°C | | 150 | 200 | µA |
| | Operating current up to +125°C | | | 300 | µA |
| Power dissipation | VDD = 5.0V | | 0.9 | | mW |
| | VDD = 3.3V | | 0.5 | | mW |
| | VDD = 2.0V | | 0.3 | | mW |
| **TEMPERATURE** | | | | | |
| Storage temperature | | –60 | | +150 | °C |
| Specified temperature | | –40 | | +125 | °C |

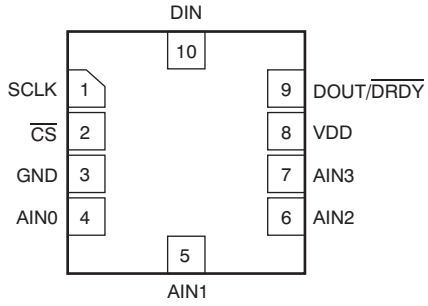
## THERMAL INFORMATION

| THERMAL METRIC(1) | | ADS1118 DGS 10 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 186.8 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 51.5 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 108.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.7 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 106.5 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | n/a | |

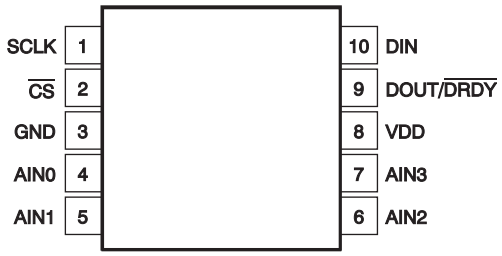
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## PIN CONFIGURATIONS

**RUG PACKAGE**
**QFN-10**
**(TOP VIEW)**




**DGS PACKAGE**
**MSOP-10**
**(TOP VIEW)**




## PIN DESCRIPTIONS

| PIN # | PIN NAME | ANALOG/ DIGITAL INPUT/ OUTPUT | DESCRIPTION |
|---|---|---|---|
| 1 | SCLK | Digital input | Serial clock input |
| 2 | $\overline{CS}$ | Digital input | Chip select; active low |
| 3 | GND | Analog | Ground |
| 4 | AIN0 | Analog input | Differential channel 1: positive input or single-ended channel 1 input |
| 5 | AIN1 | Analog input | Differential channel 1: negative input or single-ended channel 2 input |
| 6 | AIN2 | Analog input | Differential channel 2: positive input or single-ended channel 3 input |
| 7 | AIN3 | Analog input | Differential channel 2: negative input or single-ended channel 4 input |
| 8 | VDD | Analog | Power supply: 2V to 5.5V |
| 9 | DOUT/$\overline{DRDY}$ | Digital output | Serial data out combined with data ready; active low |
| 10 | DIN | Digital input | Serial data input |

## SPI TIMING CHARACTERISTICS

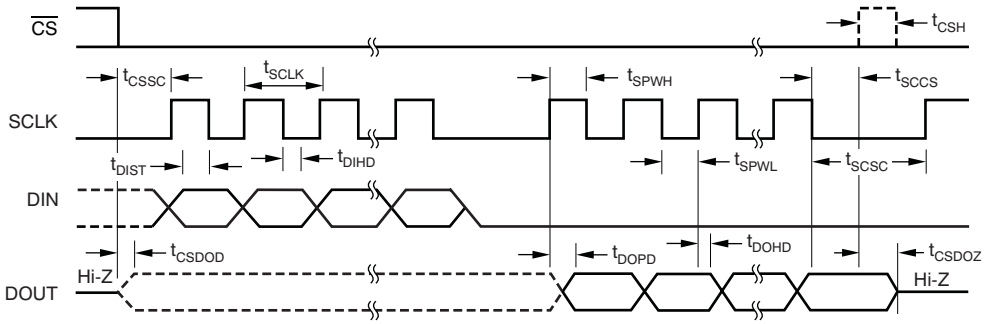



**Figure 1. Serial Interface Timing**

## TIMING REQUIREMENTS: SERIAL INTERFACE TIMING

At $T_A$ = –40°C to +125°C and VDD = 2V to 5.5V, unless otherwise noted.

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{CSSC}$ | $\overline{CS}$ low to first SCLK: setup time(1) | 100 | | ns |
| $t_{SCLK}$ | SCLK period | 250 | | ns |
| $t_{SPWH}$ | SCLK pulse width: high | 100 | | ns |
| $t_{SPWL}$ | SCLK pulse width: low(2) | 100 | | ns |
| | | | 28 | ms |
| $t_{DIST}$ | Valid DIN to SCLK falling edge: setup time | 50 | | ns |
| $t_{DIHD}$ | Valid DIN to SCLK falling edge: hold time | 50 | | ns |
| $t_{DOPD}$ | SCLK rising edge to valid new DOUT: propagation delay(3) | | 50 | ns |
| $t_{DOHD}$ | SCLK rising edge to DOUT invalid: hold time | 0 | | ns |
| $t_{CSDOD}$ | $\overline{CS}$ low to DOUT driven: propagation delay | 100 | | ns |
| $t_{CSDOZ}$ | $\overline{CS}$ high to DOUT Hi-Z: propagation delay | 100 | | ns |
| $t_{CSH}$ | $\overline{CS}$ high pulse | 200 | | ns |
| $t_{SCCS}$ | Final SCLK falling edge to $\overline{CS}$ high | 100 | | ns |

(1) $\overline{CS}$ can be tied low.
(2) Holding SCLK low longer than 28ms resets the SPI interface.
(3) DOUT load = 20pF || 100kΩ to DGND.

# TYPICAL CHARACTERISTICS

At $T_A$ = +25°C and VDD = 3.3V, unless otherwise noted.

### TOTAL ERROR vs INPUT SIGNAL

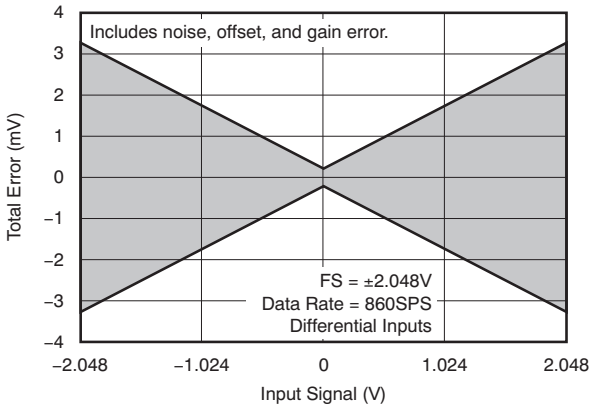



**Figure 2.**

### DATA RATE vs TEMPERATURE

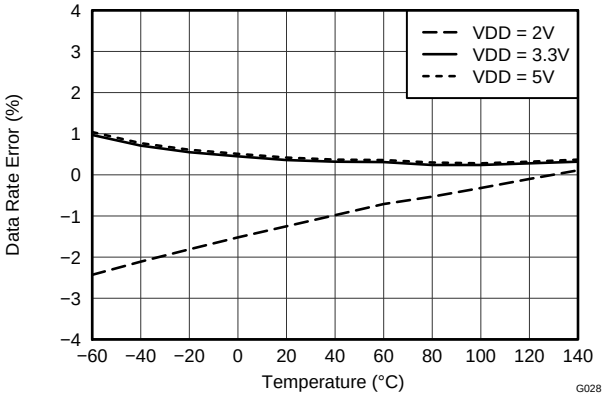



**Figure 3.**

### NOISE vs INPUT SIGNAL

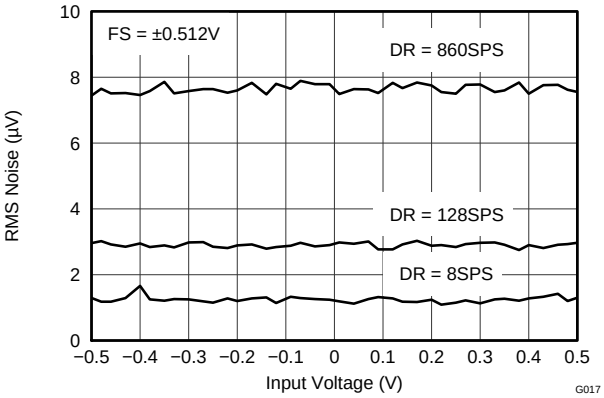



**Figure 4.**

### NOISE vs SUPPLY VOLTAGE

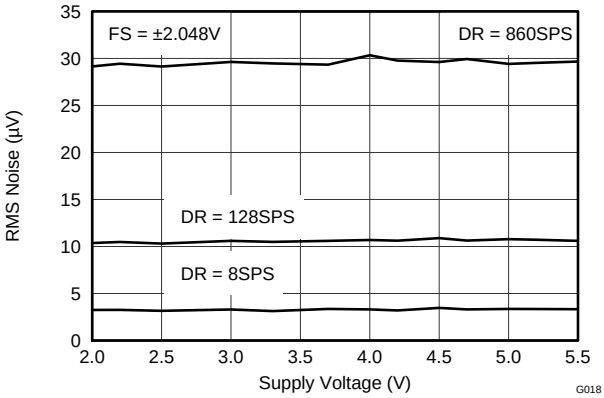



**Figure 5.**

### NOISE vs TEMPERATURE

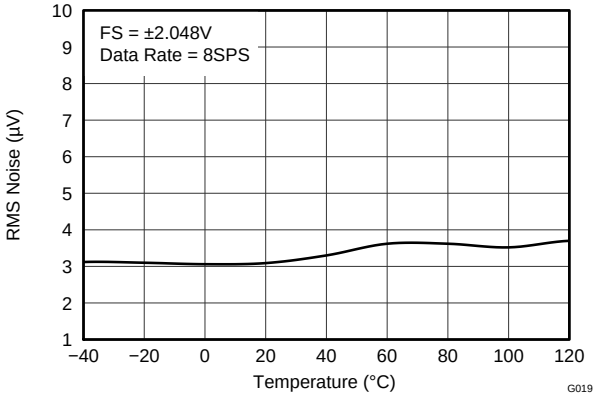



**Figure 6.**

### INL vs SUPPLY VOLTAGE(1)

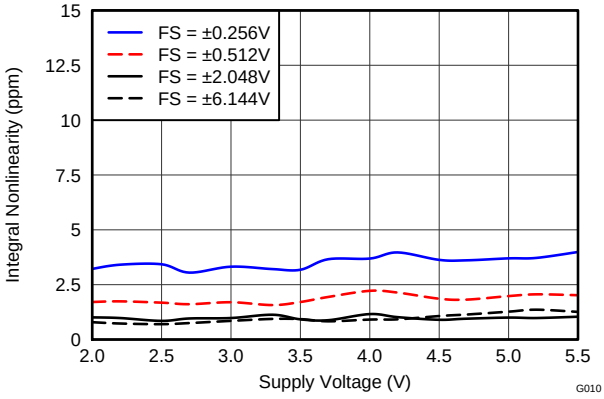



**Figure 7.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C and VDD = 3.3V, unless otherwise noted.

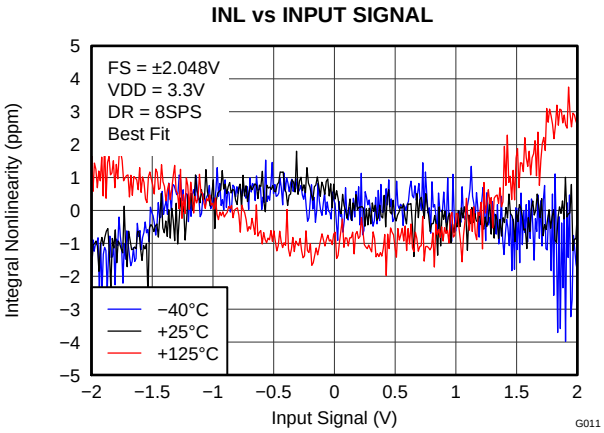



Figure 8.

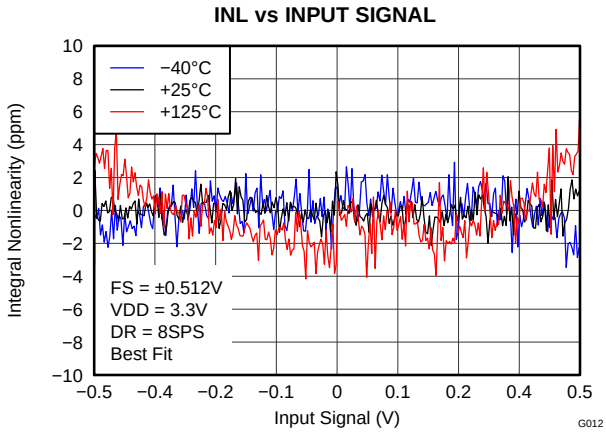



Figure 9.

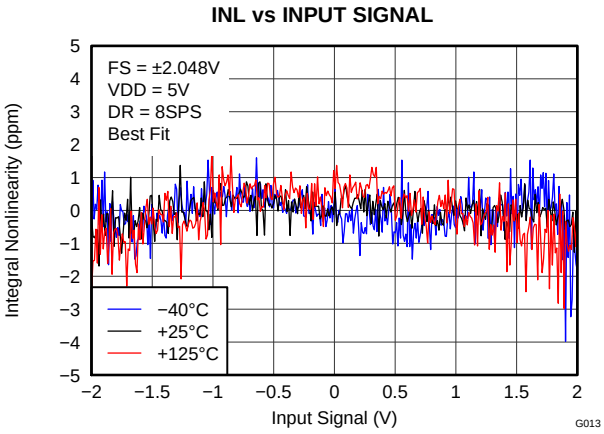



Figure 10.

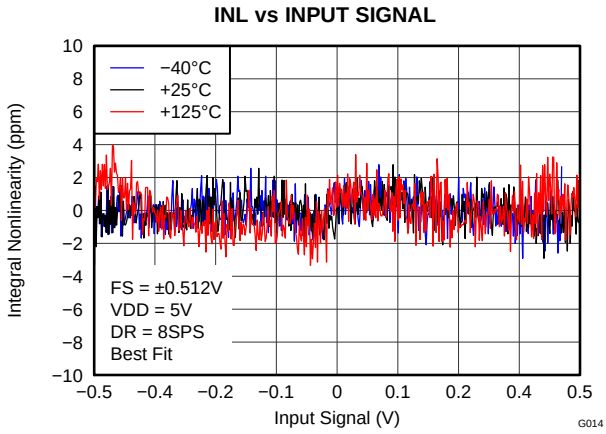



Figure 11.

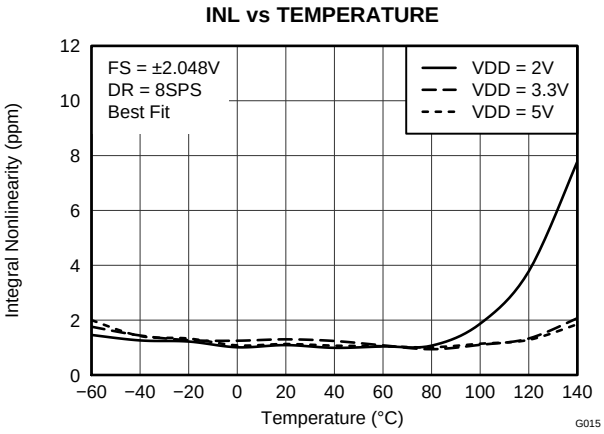



Figure 12.

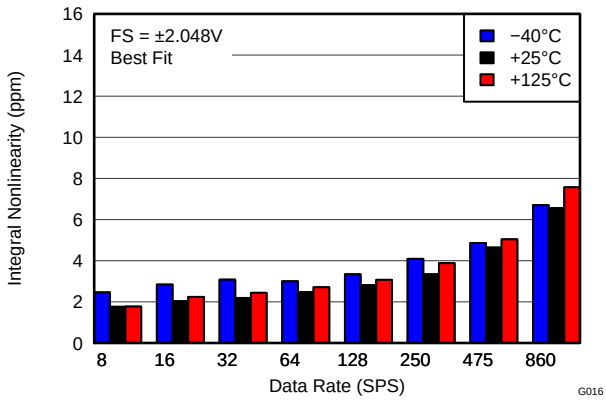



Figure 13.

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C and VDD = 3.3V, unless otherwise noted.

**SINGLE-ENDED OFFSET vs TEMPERATURE**

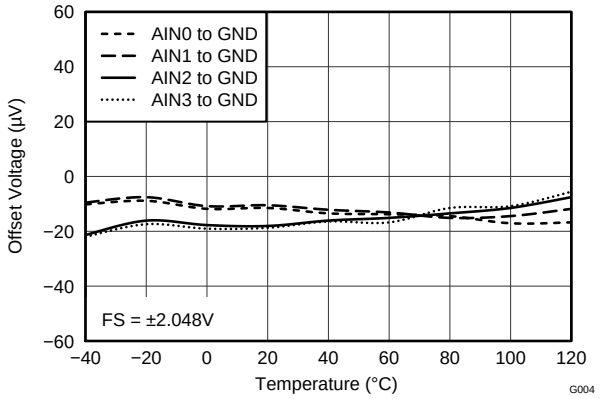



**Figure 14.**

**SINGLE-ENDED OFFSET vs SUPPLY**

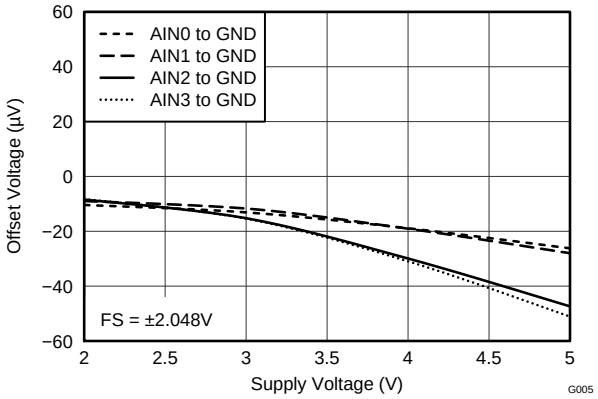



**Figure 15.**

**DIFFERENTIAL OFFSET vs TEMPERATURE**

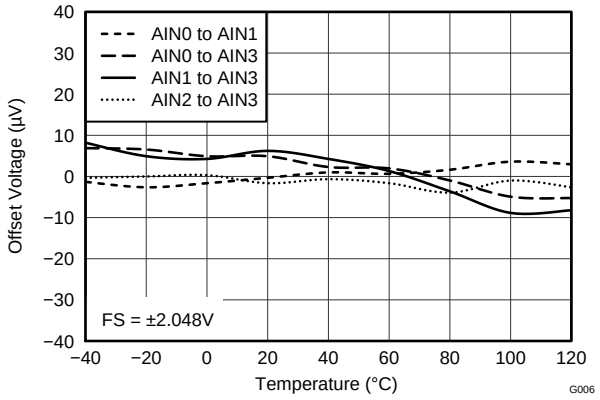



**Figure 16.**

**DIFFERENTIAL OFFSET vs SUPPLY**

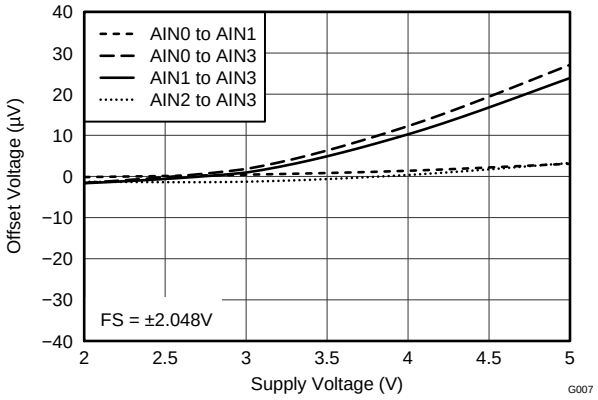



**Figure 17.**

**OFFSET DRIFT HISTOGRAM**

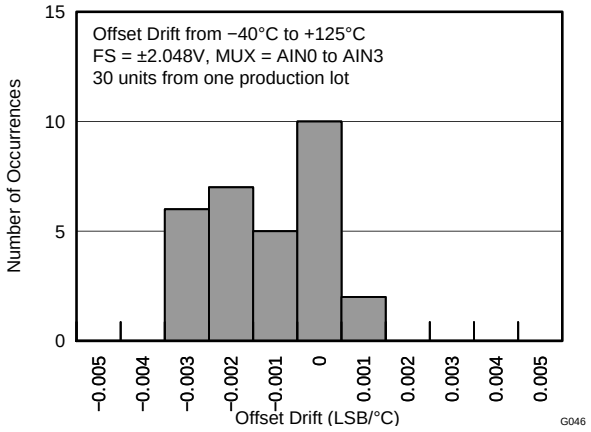



**Figure 18.**

**OFFSET HISTOGRAM**

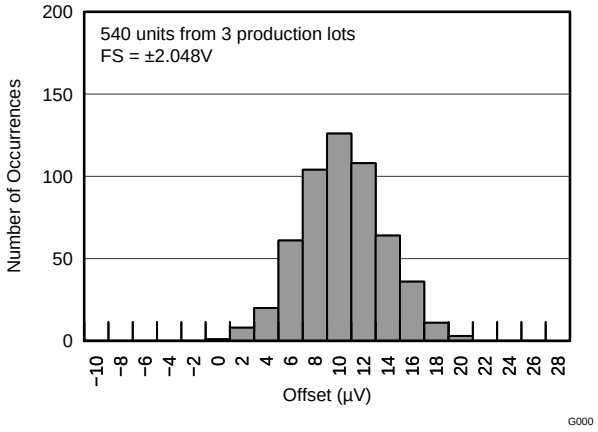



**Figure 19.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C and VDD = 3.3V, unless otherwise noted.

**GAIN ERROR vs TEMPERATURE**

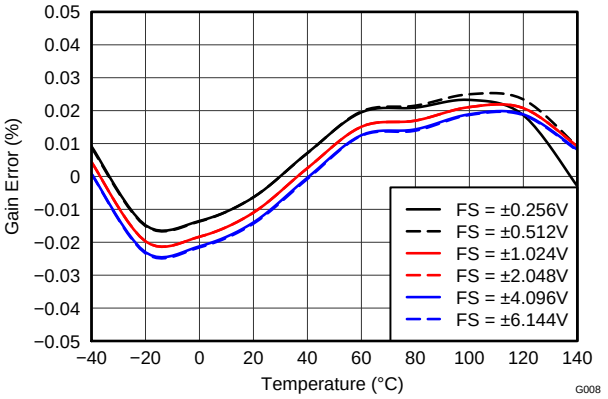



**Figure 20.**

**GAIN ERROR vs SUPPLY**

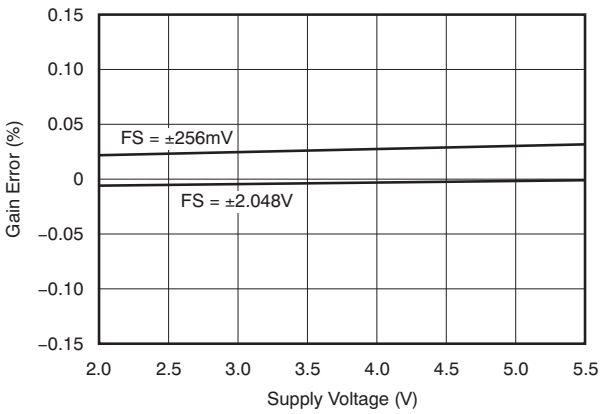



**Figure 21.**

**GAIN ERROR HISTOGRAM**

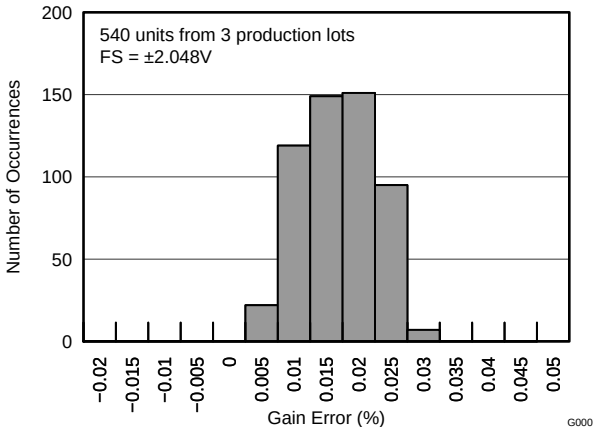



**Figure 22.**

**TEMPERATURE SENSOR ERROR vs AMBIENT TEMPERATURE**

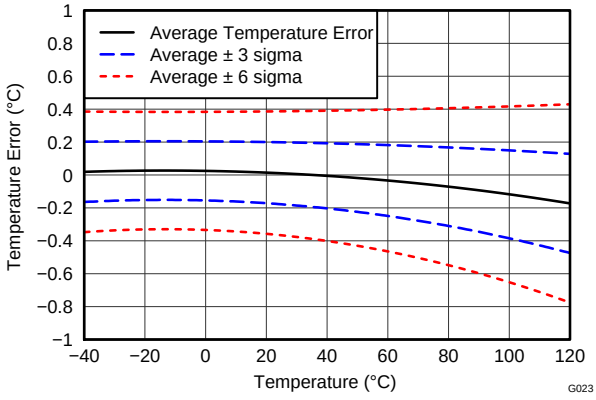



**Figure 23.**

**TEMPERATURE SENSOR ERROR HISTOGRAM**

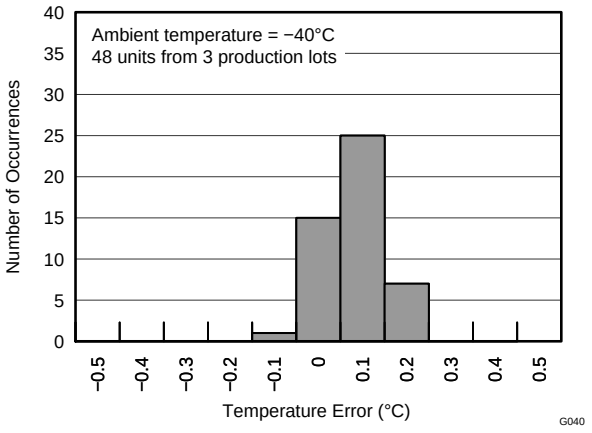



**Figure 24.**

**TEMPERATURE SENSOR ERROR HISTOGRAM**

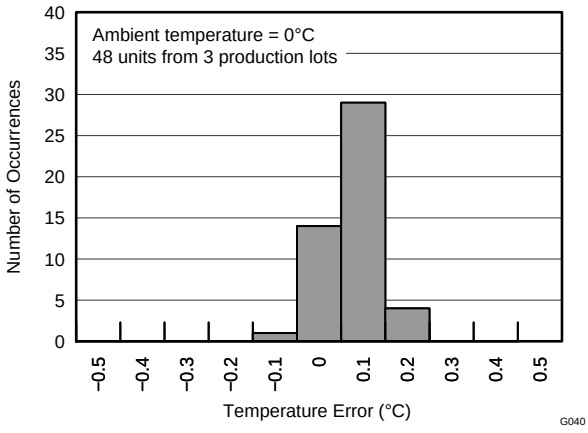



**Figure 25.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C and VDD = 3.3V, unless otherwise noted.

**TEMPERATURE SENSOR ERROR HISTOGRAM**

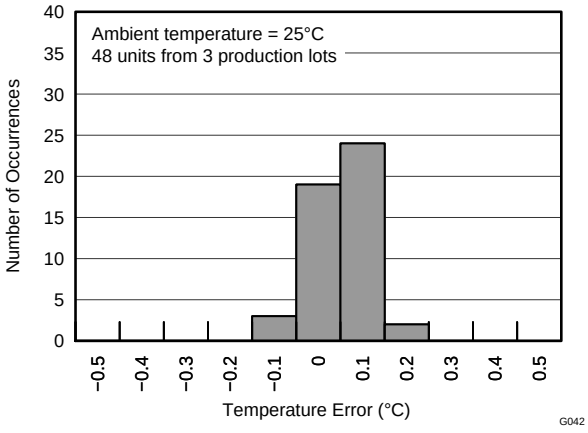



**Figure 26.**

**TEMPERATURE SENSOR ERROR HISTOGRAM**

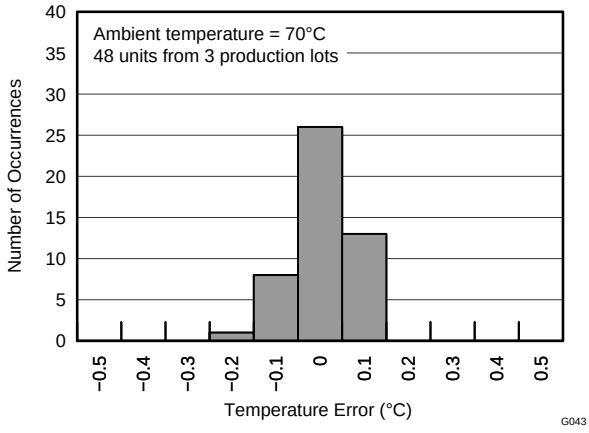



**Figure 27.**

**TEMPERATURE SENSOR ERROR HISTOGRAM**

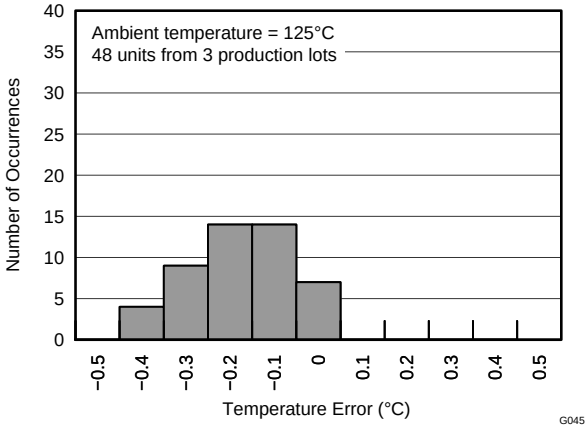



**Figure 28.**

**OPERATING CURRENT vs TEMPERATURE**

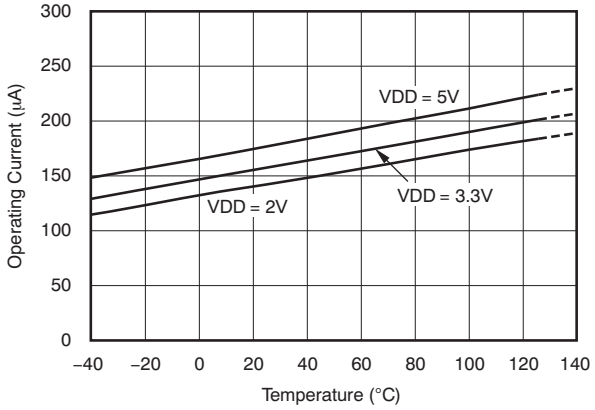



**Figure 29.**

**SHUTDOWN CURRENT vs TEMPERATURE**

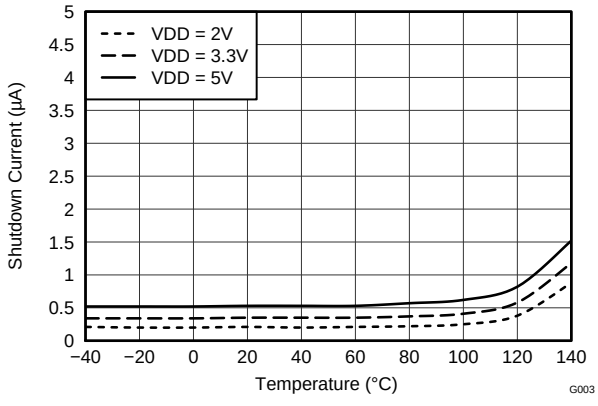



**Figure 30.**

**FREQUENCY RESPONSE**

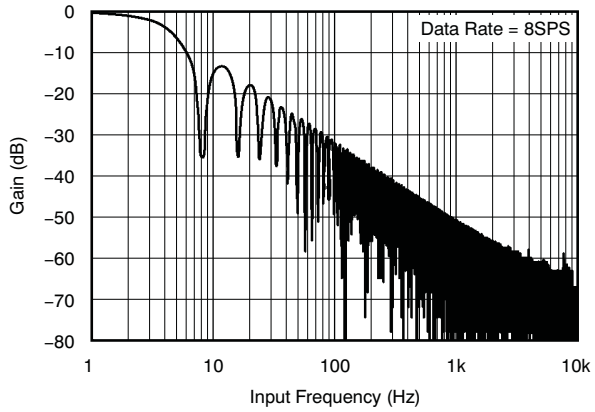



**Figure 31.**

## OVERVIEW

The ADS1118 is a very small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS1118 is extremely easy to configure and design into a wide variety of applications, and allows precise measurements to be obtained with very little effort. Both experienced and novice users of data converters find designing with the ADS1118 family to be intuitive and problem-free.

The ADS1118 consists of a ΔΣ analog-to-digital (A/D) core with adjustable gain, an internal voltage reference, a clock oscillator, and an SPI. This device is also a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. Figure 32 shows the ADS1118 functional block diagram.

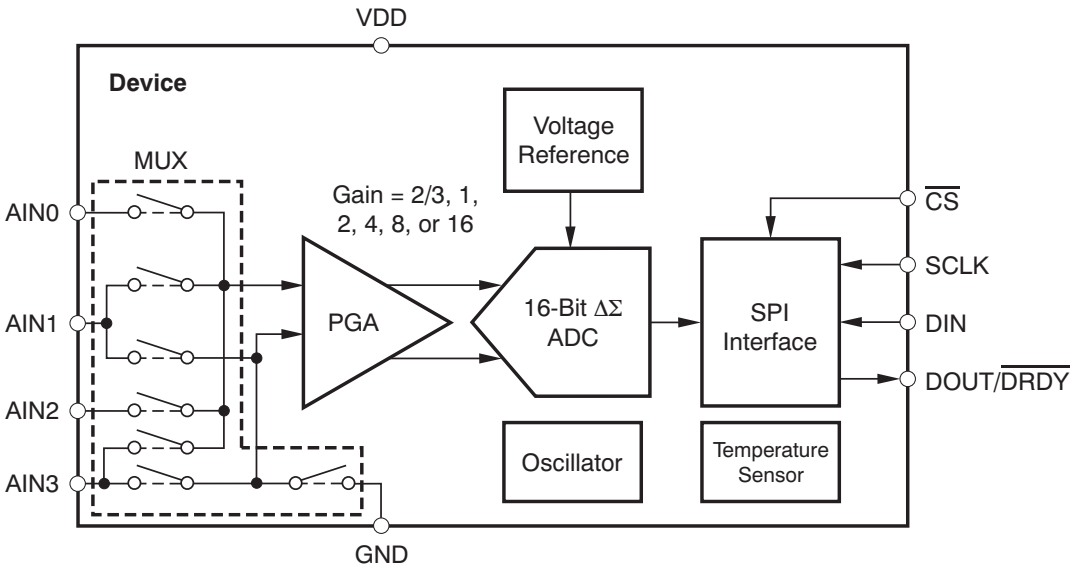



**Figure 32. ADS1118 Functional Block Diagram**

The ADS1118 A/D core measures a differential signal, $V_{IN}$, that is the difference of $AIN_P$ and $AIN_N$. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation in any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1118 has two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal conversion register. The device then enters a low-power shutdown mode. This mode is intended to provide significant power savings in systems that require only periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recent completed conversion.

## MULTIPLEXER

The ADS1118 contains an input multiplexer, as shown in Figure 33. Either four single-ended or two differential signals can be measured. Additionally, AIN0 and AIN1 may be measured differentially to AIN3. The multiplexer is configured by three bits in the Config Register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

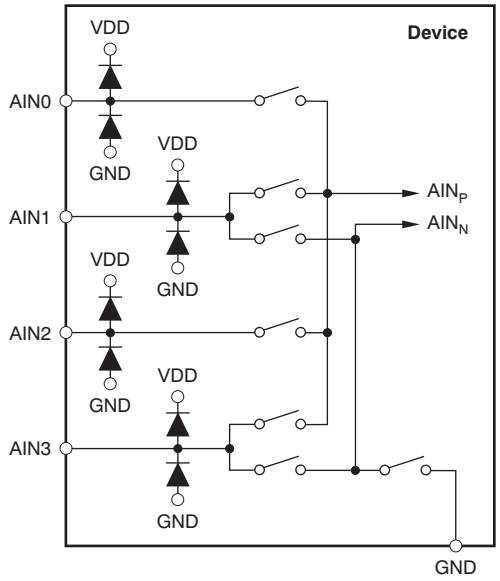



**Figure 33. ADS1118 MUX**

When measuring single-ended inputs, it is important to note that the negative range of the output codes are not used. These codes are for measuring negative differential signals, such as ($AIN_P$ – $AIN_N$) < 0. Electrostatic discharge (ESD) diodes to VDD and GND protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range of Equation 1:

GND – 0.3V < AINx < VDD + 0.3V (1)

If it is possible that the voltages on the input pins may violate these conditions, external Schottky clamp diodes and/or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table). While the analog inputs can support signals marginally above supply, under no circumstances should any analog or digital input or output be driven to greater than 5.5V with respect to the GND pin.

Also, overdriving one unused input on the ADS1118 may affect conversions taking place on other input pins. If overdrive on unused inputs is possible, it is recommended to clamp the signal with external Schottky diodes.

## ANALOG INPUTS

The ADS1118 uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between $AIN_P$ and $AIN_N$. The capacitors used are small, and to external circuitry, the average loading appears resistive. This structure is shown in Figure 34. The resistance is set by the capacitor values and the rate at which they are switched. Figure 35 shows the on/off setting of the switches illustrated in Figure 34. During the sampling phase, switches $S_1$ are closed. This event charges $C_{A1}$ to $AIN_P$, $C_{A2}$ to $AIN_N$, and $C_B$ to ($AIN_P$ – $AIN_N$). During the discharge phase, $S_1$ is first opened and then $S_2$ is closed. Both $C_{A1}$ and $C_{A2}$ then discharge to approximately 0.7V and $C_B$ discharges to 0V. This charging draws a very small transient current from the source driving the ADS1118 analog inputs. The average value of this current can be used to calculate the effective impedance ($R_{eff}$), where $R_{eff} = V_{IN}/I_{AVERAGE}$.

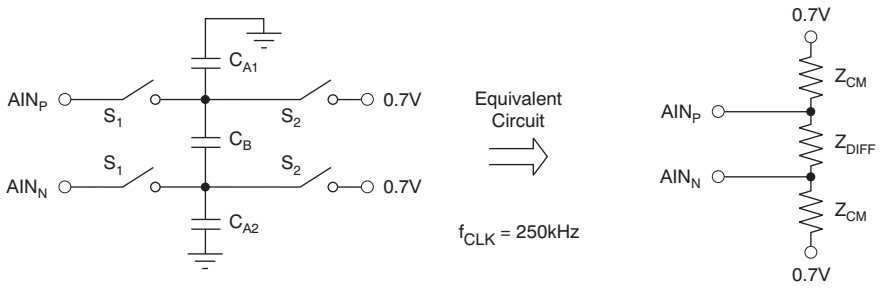



**Figure 34. Simplified Analog Input Circuit**

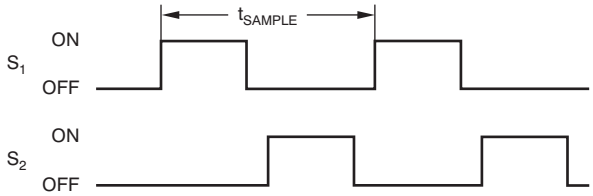



**Figure 35. $S_1$ and $S_2$ Switch Timing for Figure 34**

The common-mode input impedance is measured by applying a common-mode signal to the shorted $AIN_P$ and $AIN_N$ inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the PGA gain setting, but is approximately 6MΩ for the default PGA gain setting. In Figure 34, the common-mode input impedance is $Z_{CM}$.

The differential input impedance is measured by applying a differential signal to $AIN_P$ and $AIN_N$ inputs where one input is held at 0.7V. The current that flows through the pin connected to 0.7V is the differential current and scales with the PGA gain setting. In Figure 34, the differential input impedance is $Z_{DIFF}$. Table 1 describes the typical differential input impedance.

**Table 1. Differential Input Impedance**

| FS (V) | DIFFERENTIAL INPUT IMPEDANCE |
|---|---|
| ±6.144V(1)(1) | 22MΩ |
| ±4.096V(1)(1) | 15MΩ |
| ±2.048V | 4.9MΩ |
| ±1.024V | 2.4MΩ |
| ±0.512V | 710kΩ |
| ±0.256V | 710kΩ |

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

The typical value of the input impedance cannot be neglected. Unless the input source has a low impedance, the ADS1118 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Note that active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock oscillator frequency drifts slightly with temperature, the input impedances also drift. For many applications, this input impedance drift can be ignored, and the values given in Table 1 for typical input impedance are valid.

## FULL-SCALE INPUT

A PGA is implemented before the ΔΣ core of the ADS1118. The PGA can be set to gains of 2/3, 1, 2, 4, 8, and 16. Table 2 shows the corresponding full-scale (FS) ranges. The PGA is configured by three bits in the Config register. The PGA = 2/3 setting allows input measurement to extend up to the supply voltage when VDD is larger than 4V. Note, however, in this case (as well as for PGA = 1 and VDD < 4V) that it is not possible to reach a full-scale output code on the ADC. Analog input voltages may never exceed the analog input voltage limits given in the Electrical Characteristics table.

**Table 2. PGA Gain Full-Scale Range**

| PGA SETTING | FS (V) |
|---|---|
| 2/3 | ±6.144V(1) (1) |
| 1 | ±4.096V(1) |
| 2 | ±2.048V |
| 4 | ±1.024V |
| 8 | ±0.512V |
| 16 | ±0.256V |

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

## DATA FORMAT

The ADS1118 provides 16 bits of data in binary twos complement format. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 3 summarizes the ideal output codes for different input signals. Figure 36 shows code transitions versus input voltage.

**Table 3. Input Signal versus Ideal Output Code**

| INPUT SIGNAL, $V_{IN}$ ($AIN_P$ – $AIN_N$) | IDEAL OUTPUT CODE(1) |
|---|---|
| ≥ FS ($2^{15}$ – 1)/$2^{15}$ | 7FFFh |
| +FS/$2^{15}$ | 0001h |
| 0 | 0 |
| –FS/$2^{15}$ | FFFFh |
| ≤ –FS | 8000h |

(1) Excludes the effects of noise, INL, offset, and gain errors.

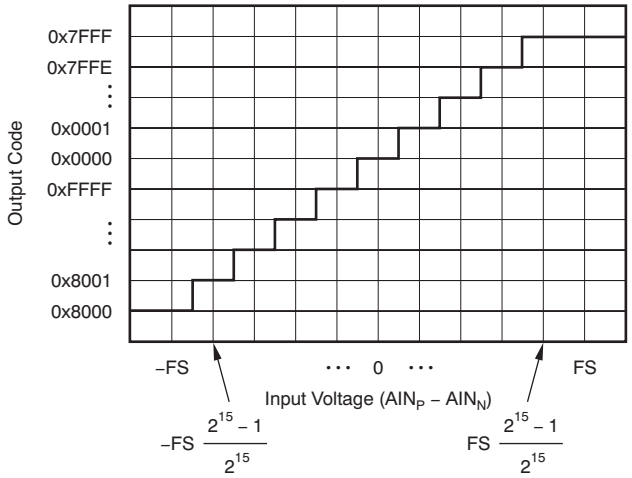



**Figure 36. ADS1118 Code Transition Diagram**

## TEMPERATURE SENSOR

The temperature measurement mode of the ADS1118 is configured as a 14-bit result when enabled. Two bytes must be read to obtain data. The first byte is the most significant byte (MSB), followed by a second byte, the least significant byte (LSB). The first 14 bits are used to indicate temperature. That is, the 14-bit temperature result is left-justified within the 16-bit result register and the last two bits always read back as '0'. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary twos complement format.

**Table 4. 14-bit Temperature Data Format**

| TEMPERATURE (°C) | DIGITAL OUTPUT (BINARY) | HEX |
|---|---|---|
| 128 | 01 0000 0000 0000 | 1000 |
| 127.96875 | 00 1111 1111 1111 | 0FFF |
| 100 | 00 1100 1000 0000 | 0C80 |
| 80 | 00 1010 0000 0000 | 0A00 |
| 75 | 00 1001 0110 0000 | 0960 |
| 50 | 00 0110 0100 0000 | 0640 |
| 25 | 00 0011 0010 0000 | 0320 |
| 0.25 | 00 0000 0000 1000 | 0008 |
| 0 | 00 0000 0000 0000 | 0000 |
| –0.25 | 11 1111 1111 1000 | 3FF8 |
| –25 | 11 1100 1110 0000 | 3CE0 |
| –55 | 11 1001 0010 0000 | 3920 |

### Converting from Temperature to Digital Codes

**For positive temperatures (for example, +50°C):**

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 14-bit left justified format with the MSB = 0 to denote the positive sign.

**Example:** (+50°C)/(0.03125°C/count) = 1600 = 0640h = 00 0110 0100 0000

**For negative temperatures (for example –25°C):**

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then denote the negative sign with the MSB = 1.

**Example:**(|–25°C|)/(0.03125°C/count) = 800 = 0320h = 00 0011 0010 0000

Twos complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

### Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a '0' or a '1'. If the MSB is a '0', simply multiply the decimal code by 0.03125°C to obtain the result. If the MSB = 1, subtract '1' from the result and complement all of the bits. Then multiply the result by –0.03125°C.

**Example:** ADS1118 reads back 0960h: 0960h has an MSB = 0.

(0960h)(0.03125°C) = (2400)(0.03125°C) = +75°C

**Example:** ADS1118 reads back 3CE0h: 3CE0h has an MSB = 1.

Complement the result: 3CE0h → 0320h

(0320h)(–0.03125°C) = (800)(–0.03125°C) = –25°C

## ALIASING

As with any data converter, if the input signal contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, the input signal must be bandlimited. Some signals are inherently bandlimited; for example, the output of a thermocouple has a limited rate of change. Nevertheless, these signals can contain noise and interference components. These components can fold back into the sampling band in the same way as with any other signal.

The ADS1118 digital filter provides some attenuation of high-frequency noise, but the digital sinc filter frequency response cannot completely replace an anti-aliasing filter. For some applications, some external filtering may be needed; in such instances, a simple RC filter is adequate.

When designing an input filter circuit, be sure to take into account the interaction between the filter network and the input impedance of the ADS1118.

## OPERATING MODES

The ADS1118 operates in one of two modes: continuous conversion or single-shot. In continuous conversion mode, the ADS1118 continuously performs conversions. Once a conversion has been completed, the ADS1118 places the result in the Conversion Register and immediately begins another conversion. In single-shot mode, the ADS1118 waits until the OS bit is set high. Once asserted, the bit is set to '0', indicating that a conversion is currently in progress. Once conversion data are ready, the OS bit reasserts and the device powers down. Writing a '1' to the OS bit during a conversion has no effect.

## RESET AND POWER-UP

When the ADS1118 powers up, a reset is performed. As part of the reset process, the ADS1118 sets all of the bits in the Config Register to the respective default settings. By default, the ADS1118 enters into a power-down state at start-up. The device interface and digital are active, but no conversion occurs until the Config Register is written to. The initial power-down state of the ADS1118 is intended to relieve systems with tight power-supply requirements from encountering a surge during power-up.

## DUTY CYCLING FOR LOW POWER

For many applications, improved performance at low data rates may not be required. For these applications, the ADS1118 supports duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADS1118 in power-down mode with a data rate set to 860SPS could be operated by a microcontroller that instructs a single-shot conversion every 125ms (8SPS). Because a conversion at 860SPS only requires about 1.2ms, the ADS1118 enters power-down mode for the remaining 123.8ms. In this configuration, the ADS1118 consumes about 1/100th the power of the ADS1118 operated in continuous conversion mode. The rate of duty cycling is completely arbitrary and is defined by the master controller.

## SERIAL INTERFACE

The SPI-compatible serial interface consists of either four signals: $\overline{CS}$, SCLK, DIN, and DOUT/$\overline{DRDY}$; or three signals, in which case $\overline{CS}$ may be tied low. The interface is used to read conversion data, read and write registers, and control the ADS1118 operation.

## CHIP SELECT ($\overline{CS}$)

The chip select ($\overline{CS}$) selects the ADS1118 for SPI communication. This feature is useful when multiple devices share the serial bus. $\overline{CS}$ must remain low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT/$\overline{DRDY}$ enters a high-impedance state; as such, DOUT/$\overline{DRDY}$ cannot provide indication of data ready. In situations where multiple devices are present and DOUT/$\overline{DRDY}$ must be monitored; by periodically lowering $\overline{CS}$, the DOUT/$\overline{DRDY}$ pin either immediately goes high to indicate that no new data are available, or it immediately goes low, to indicate that new data are present in the Config Register and are available for transfer. New data can be transferred at anytime without concern of data corruption. When a transmission starts, the current result is locked into the output shift register and does not change until the communication is completed. This system avoids any possibility of data corruption.

## SERIAL CLOCK (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT/DRDY pins into and out of the ADS1118. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. If SCLK is held low for 28ms, the serial interface resets and the next SCLK pulse starts a new communication cycle. This timeout feature can be used to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

## DATA INPUT (DIN)

The data input pin (DIN) is used along with SCLK to send data to the ADS1118 (op code commands and register data). The device latches data on DIN on the falling edge of SCLK. The ADS1118 never drives the DIN pin.

## DATA OUTPUT AND DATA READY (DOUT/$\overline{\text{DRDY}}$)

The data output and data ready pin (DOUT/$\overline{\text{DRDY}}$) are used with SCLK to read conversion and register data from the ADS1118. In Read Data Continuous mode, DOUT/$\overline{\text{DRDY}}$ goes low when conversion data are ready and goes high 8µs before the data ready signal. Data on DOUT/$\overline{\text{DRDY}}$ are shifted out on the rising edge of SCLK. By default DOUT/DRDY goes to a high-impedance state when $\overline{\text{CS}}$ is high. Alternatively, the ADS1118 DOUT/$\overline{\text{DRDY}}$ pin can be configured as a weak pull-up if $\overline{\text{CS}}$ is high. This feature is intended to reduce the risk of DOUT/$\overline{\text{DRDY}}$ floating near midsupply and causing leakage current in the master. If the ADS1118 does not share the serial bus with another device, $\overline{\text{CS}}$ may be tied low.

## POWER-DOWN MODE

When the PWDN bit in the Config Register is set to '1', the ADS1118 enters a lower power standby state. This condition is also the default state the ADS1118 enters when power is first supplied. In this mode, the ADS1118 uses no more than 2µA of current. During this time, the device responds to commands, but does not perform any data conversion. To exit this mode, simply write a '0' to the PWDN bit in the Config Register.

## REGISTERS

The ADS1118 has two registers that are accessible via the SPI port. The Conversion Register contains the result of the last conversion. The Config Register allows the modification of the ADS1118 operating modes and the ability to query the status of the device.

### Conversion Register

This 16-bit register contains the result of the last conversion in binary twos complement format. Following power-up, the Conversion Register is cleared to '0', and remains '0' until the first conversion is completed.

The register format is shown in Table 5.

**Table 5. Conversion Register (Read-Only)**

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NAME | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

### Config Register

The 16-bit register can be used to control the ADS1118 operating mode, input selection, data rate, PGA settings, and comparator modes. The register format is shown in Table 6.

**Table 6. Config Register (Read/Write)**

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| NAME | OS | MUX2 | MUX1 | MUX0 | PGA2 | PGA1 | PGA0 | MODE |
| | | | | | | | | |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | DR2 | DR1 | DR0 | TS_MODE | PULL_UP_EN | NOP1 | NOP2 | CNV_RDY_FL |

Default = 8583h.

**Bit 15** **OS: Operational status/single-shot conversion start**

This bit determines the operational status of the device.
This bit can only be written when in power-down mode.

For a write status:
0 : No effect
1 : Begin a single conversion (when in power-down mode)
For a read status:
0 : Device is currently performing a conversion
1 : Device is not currently performing a conversion

**Bits[14:12]** **MUX[2:0]: Input multiplexer configuration**

These bits configure the input multiplexer. No effect when in temperature sensor mode.

000 : $AIN_P$ = AIN0 and $AIN_N$ = AIN1 (default)
001 : $AIN_P$ = AIN0 and $AIN_N$ = AIN3
010 : $AIN_P$ = AIN1 and $AIN_N$ = AIN3
011 : $AIN_P$ = AIN2 and $AIN_N$ = AIN3
100 : $AIN_P$ = AIN0 and $AIN_N$ = GND
101 : $AIN_P$ = AIN1 and $AIN_N$ = GND
110 : $AIN_P$ = AIN2 and $AIN_N$ = GND
111 : $AIN_P$ = AIN3 and $AIN_N$ = GND

**Bits[11:9]** **PGA[2:0]: Programmable gain amplifier configuration**

These bits configure the programmable gain amplifier. No effect when in temperature sensor mode.

000 : FS = ±6.144V(1)
001 : FS = ±4.096V(1)
010 : FS = ±2.048V (default)
011 : FS = ±1.024V
100 : FS = ±0.512V
101 : FS = ±0.256V
110 : FS = ±0.256V
111 : FS = ±0.256V

**Bit 8** **MODE: Device operating mode**

This bit controls the current operational mode of the ADS1118.
0 : Continuous conversion mode
1 : Power-down single-shot mode (default)

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

**Bits[7:5]** **DR[2:0]: Data rate**

These bits control the data rate setting.

| | |
|---|---|
| 000 : 8SPS | 100 : 128SPS (default) |
| 001 : 16SPS | 101 : 250SPS |
| 010 : 32SPS | 110 : 475SPS |
| 011 : 64SPS | 111 : 860SPS |

**Bit 4** **TS_MODE: Temperature sensor mode**

This bit configures the ADC to convert temperature or input signals.
0 : ADC mode (default)
1 : Temperature sensor mode

**Bit 3** **PULL_UP_EN: Pull-up enable**

This bit enables a weak pull-up resistor on the DOUT pin when $\overline{CS}$ is high. When enabled, a 400kΩ resistor connects the bus line to supply when $\overline{CS}$ is high. When disabled, the DOUT pin floats when $\overline{CS}$ is high.
0 : Pull-up resistor disabled on DOUT pin (default)
1 : Pull-up resistor enabled on DOUT pin

**Bits[2:0]** **NOP: No operation**

The NOP bits control whether data are written to the Config Register or not. In order for data to be written to the Config Register, the NOP bits must be written as '01'. Any other value written to the NOP bits results in a NOP command. This means that DIN can be held high or low during SCLK pulses without data being written to the Config Register.
00 : Invalid data, do not update the contents of the Config Register.
01 : Valid data, update the Config Register (default)
10 : Invalid data, do not update the contents of the Config Register.
11: Invalid data, do not update the contents of the Config Register.

**Bit 0** **CNV_RDY_FL: Conversion ready flag**

This bit is active low and indicates when data are ready from the converter. When it is high, a conversion is not yet ready and is in process. The purpose of the conversion ready flag bit is to return the DOUT pin line to a high state to prepare for the falling edge from new data.
0 : Data ready, no conversion in progress
1 : Data not ready, conversion in progress (default)

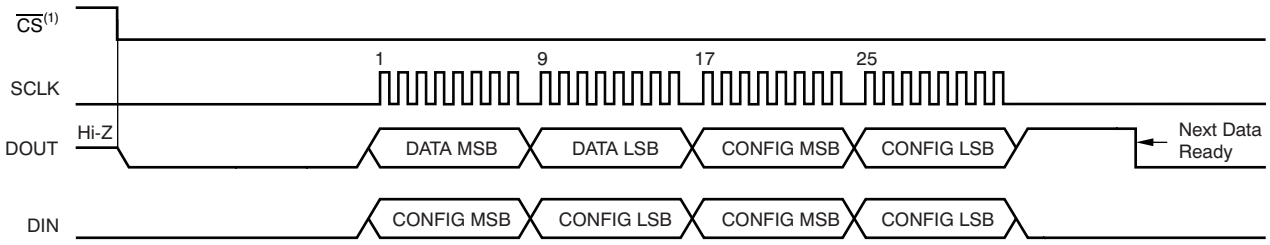
## DATA RETRIEVAL

Data may be read in one of two modes: Single-Shot and Continuous Conversion mode. The mode is selected by writing to the OS bit in the Config Register.

### Continuous Conversion Mode

In Continuous Conversion mode, the conversion data are read from the device without an op code command. When DOUT/$\overline{DRDY}$ asserts low (indicating that new conversion data are ready), the conversion data are read by shifting the data out on DOUT. The MSB of the data (bit 15) on DOUT/$\overline{DRDY}$ is clocked out on the first rising edge of SCLK.

As shown in Figure 37, the data consist of two bytes for the conversion result and an additional two bytes for the Config Register readback. The data read operation must be completed $16/f_{CLK}$ cycles before DOUT asserts again.



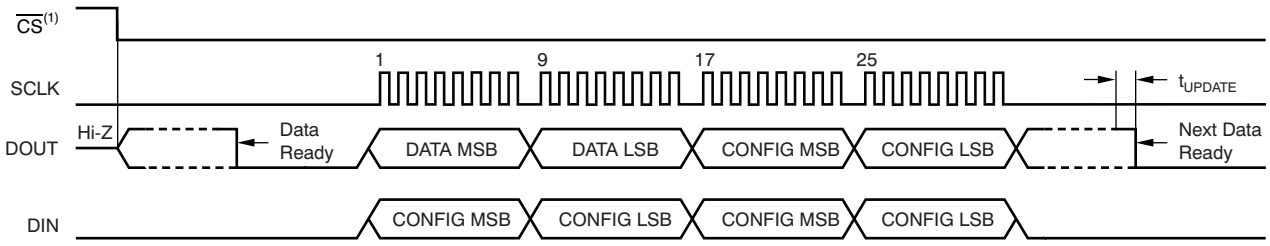

(1) $\overline{CS}$ may be held low. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data.

**Figure 37. Continuous Conversion Mode Timing**

### One-Shot Mode

In One-Shot mode, the conversion data are buffered, holding the current data until new conversion data replace it. The conversion data are read by writing a '1' to the OS bit, followed by shifting the conversion data out.

The data consist of two bytes for the conversion result and two bytes for the Config Register; see Figure 38. In contrast to the Continuous Conversion mode, DOUT does not assert low in one-shot mode.




(1) $\overline{CS}$ may be held low. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data.

**Figure 38. One-Shot Mode Timing**

# APPLICATION INFORMATION

The following sections give example circuits and suggestions for using the ADS1118 in various situations.

## BASIC CONNECTIONS AND LAYOUT CONSIDERATIONS

For many applications, connecting the ADS1118 is simple. A basic connection diagram for the ADS1118 is shown in Figure 39. Most microcontroller SPI peripherals can operate with the ADS1118. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data launch or are changed only on rising edges of SCLK and data are latched or read by the master and slave on falling edges of SCLK. Details of the SPI communication protocol employed by the ADS1118 can be found in the *SPI Timing Characteristics* section. Although it is not required, it is a good practice to place 49.9Ω resistors in series with all of the digital pins. This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection.

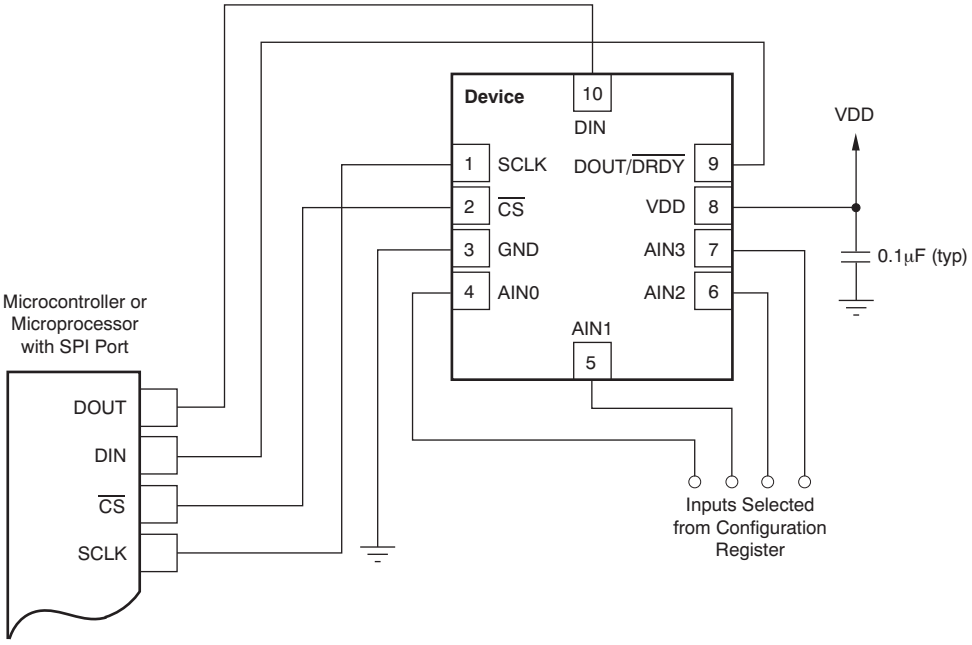



**Figure 39. Typical Connections of the ADS1118**

The fully differential voltage input of the ADS1118 is ideal for connection to differential sources with moderately low source impedance, such as thermocouples and thermistors. Although the ADS1118 can read bipolar differential signals, it cannot accept negative voltages on either input because every pin on the ADS1118 employs the use of ESD protection diodes. In the event that an input exceeds supply or drops below ground, these diodes begin to turn on. Therefore, it may be helpful to think of the ADS1118 positive voltage input as *noninverting*, and of the negative input as *inverting.*

When the ADS1118 is converting data, it draws current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply. This bypass capacitor should be placed as close to the device as possible. For very sensitive systems, or systems in harsh noise environments, avoiding the use of vias for connecting the bypass capacitor may offer superior bypass and noise immunity.

It is recommended to employ best design practices when laying out a printed circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout should separate analog components [such as ADCs, op amps, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) tranceivers, universal serial bus (USB) tranceivers, and switching regulators]. An example of good component placement is shown in Figure 40. While Figure 40 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities being employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog components.

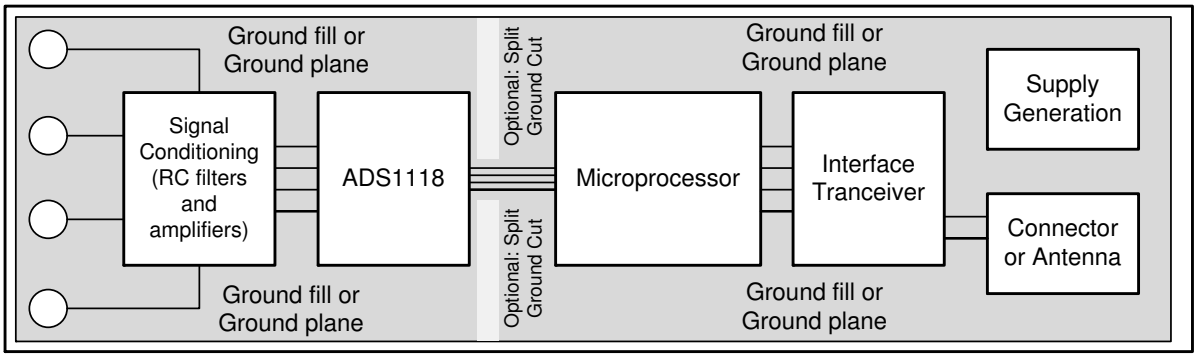
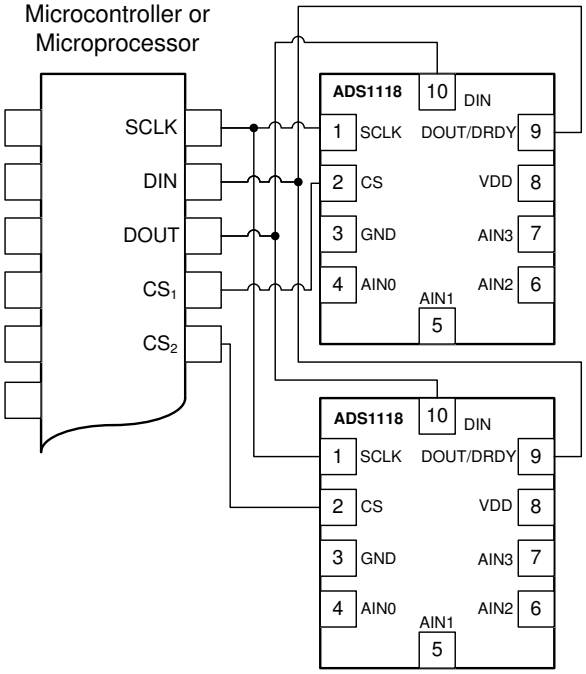



**Figure 40. System Component Placement**

The usage of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation it is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, it is generally recommended that the ground planes be connected as close to the ADS1118 as possible. It is also strongly recommended that digital components, especially RF portions, be kept as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid allowing these traces to be near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature sensing functions are much more significant than they are for the ADC functions. Details on layout considerations for the temperature sensor can be found in the *Thermocouple Measurement with Cold Junction Compensation* section. For a detailed layout example, refer to the *ADS1118EVM User's Guide* (SBAU184).

## CONNECTING MULTIPLE DEVICES

Connecting multiple ADS1118s to a single bus is simple. Using a dedicated chip-select ($\overline{CS}$) for each SPI enabled device, SCLK, DIN, and DOUT/$\overline{DRDY}$ can be safely shared. By default, when $\overline{CS}$ goes high for the ADS1118, DOUT/$\overline{DRDY}$ enters a 3-state mode. If the PULL_UP_EN bit is enabled, the DOUT/$\overline{DRDY}$ pin is pulled up to the supply of the ADS1118 by a weak 400kΩ resistor. This feature is intended to prevent DOUT/$\overline{DRDY}$ from floating near mid-rail and causing excess current leakage on a microcontroller input. The ADS1118 cannot issue a data ready pulse on DOUT/$\overline{DRDY}$ when $\overline{CS}$ is high. In order to evaluate when a new conversion is ready from the ADS1118 when using multiple devices, the master can periodically drop $\overline{CS}$ to the ADS1118. When $\overline{CS}$ lowers, the DOUT/$\overline{DRDY}$ pin immediately drives either high or low. If the DOUT/$\overline{DRDY}$ line drives low on a low $\overline{CS}$, new data are currently available for clocking out at any time. If the DOUT/$\overline{DRDY}$ line drives high, no new data are available and the ADS1118 returns the last read conversion result. Valid data can be retrieved from the ADS1118 at anytime without concern of data corruption. When SCLK rises, the current result is locked into DOUT/$\overline{DRDY}$ the output shift register. If a new conversion becomes available during data transmission, it is not avialable for readback until a new SPI transmission is initiated.




NOTE: Power and input connections omitted for clarity.

**Figure 41. Connecting Multiple ADS1118s**

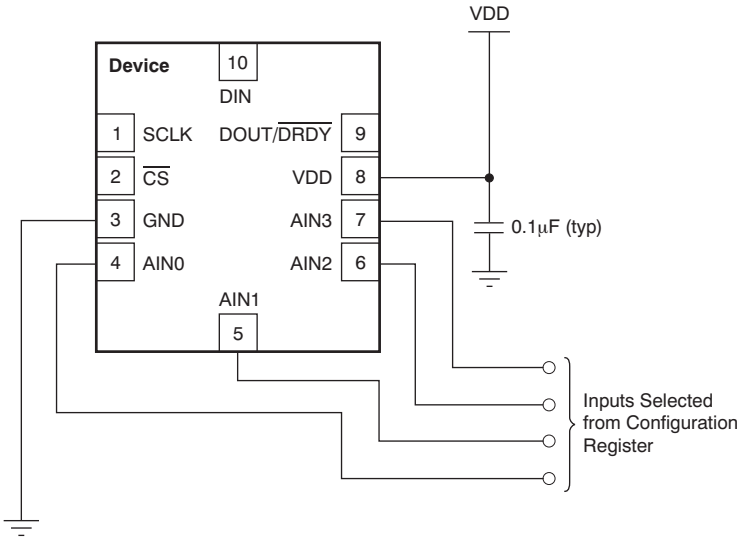
## USING GPIO PORTS FOR COMMUNICATION

Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an SPI controller is not available, the ADS1118 can be connected to GPIO pins and the SPI bus protocol can be simulated. Using GPIO pins to generate the SPI interface only requires that the pins be configured as push/pull inputs or outputs. Furthermore, if the SCLK line is held low for more than 28ms, the communication times out. This condition means that the GPIO ports must be capable of providing SCLK pulses with no more than 28ms between pulses.

## SINGLE-ENDED INPUTS

Although the ADS1118 has two differential inputs, the device can easily measure four single-ended signals. Figure 42 shows a single-ended connection scheme. The ADS1118 is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection in the Config Register. The single-ended signal can range from 0V to supply. The ADS1118 loses no linearity anywhere within the input range. Negative voltages cannot be applied to this circuit because the ADS1118 can only accept positive voltages.

The ADS1118 input range is bipolar differential. The single-ended circuit shown in Figure 42 covers only half the ADS1118 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost. For optimal noise performance, it is recommended to use differential configurations whenever possible. Differential configurations maximize the dynamic range of the ADC and provide strong attenuation of common-mode noise.




NOTE: Digital pin connections omitted for clarity.

**Figure 42. Measuring Single-Ended Inputs**

The ADS1118 is also designed to allow AIN3 to serve as a common point for measurements by adjusting the MUX configuration. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration the ADS1118 can operate with inputs where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because it allows negative voltages; however, it does not offer attenuation of common-mode noise.

## THERMOCOUPLE MEASUREMENT WITH COLD JUNCTION COMPENSATION

For an independent, two-channel thermocouple system, Figure 43 shows the basic connections. This circuit contains a simple low-pass, anti-aliasing filter, mid-point bias, and open detection. While the digital filter of the ADS1118 strongly attenuates high-frequency components of noise, it is generally recommended to provide a first-order passive RC filter to further improve this performance. The differential RC filter formed by the 500Ω resistors ($R_{DIFFA}$ and $R_{DIFFB}$) and the 1µF ($C_{DIFF}$) capacitor offers a cutoff frequency of approximately 320Hz. Additional filtering can be achieved by increasing the differential capacitor or the resistance values. However, avoid increasing the filter resistance beyond 1kΩ because the effects of the interaction with ADCs input impedance begin to affect the linearity and gain error of the ADS1118. Because of the high sampling rates supported by the ADS1118, simple post digital filtering in a microcontroller can alleviate the requirements of the analog filter and can also offer the flexibility to implement filter notches at 50Hz or 60Hz. Two 0.1µF ($C_{CMA}$ and $C_{CMB}$) capacitors are also added to offer attenuation of high-frequency common-mode noise components. Because mismatches in the common-mode capacitors cause differential noise, it is recommended that the differential capacitor be at least an order of magnitude (10x) larger than the common-mode capacitors.

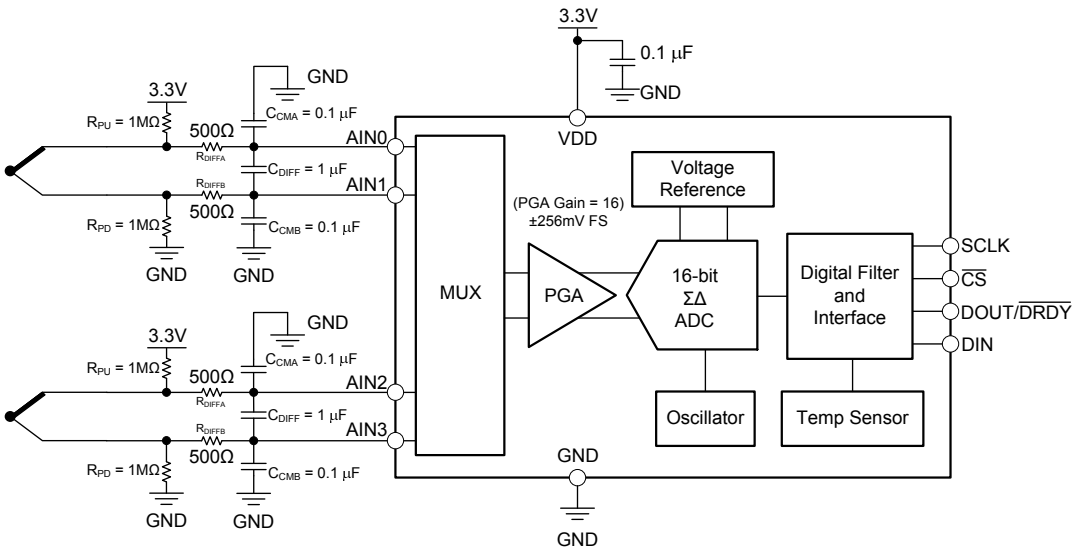



**Figure 43. Two-Channel Thermocouple System**

The two 1MΩ resistors ($R_{PU}$ and $R_{PD}$) serve two purposes. The first purpose is to offer a common-mode bias near midsupply. While the ADS1118 does offer the ability to *float* the common-mode of a signal or connect any of the inputs to a common point such as ground or supply, it is generally recommended to avoid such situations. Connecting one of the inputs to a common point decreases performance by converting common-mode noise into differential signal noise that is not strongly attenuated. The second purpose of the 1MΩ resistors is to offer a weak pull-up and pull-down for sensor open detection. In the event that a sensor is disconnected, the inputs to the ADC extend to supply and ground and yield a full-scale readout, indicating a sensor disconnection.

The procedure to actually achieve cold junction compensation is simple and can be done in several ways. One way is to interleave readings between the thermocouple inputs and the temperature sensor. That is, acquire one on-chip temperature result for every thermocouple ADC voltage measured. If the cold junction is in a very stable environment, more periodic cold junction measurements may be sufficient. These operations yield two results for every thermocouple measurement and cold junction measurement cycle: the thermocouple voltage or $V_{TC}$ and the on-chip temperature or $T_{CJC}$. In order to account for the cold junction, the temperature sensor within the ADS1118 must first be converted to a voltage proportional to the thermocouple currently being used yielding $V_{CJC}$. This conversion is generally accomplished by performing a reverse lookup on the table being used for the thermocouple voltage to temperature conversion. Then, adding the two voltages yields the thermocouple compensated voltage $V_{Actual}$ where $V_{CJC} + V_{TC} = V_{Actual}$. $V_{Actual}$ is then converted to temperature using the same lookup table from before, yielding $T_{Actual}$.

Thermocouple manufacturers usually supply a lookup table with their thermocouples that offer excellent accuracy for linearization of a specific type of thermocouple. The granularity on these lookup tables is generally very precise (at around 1°C for each lookup value). To save microcontroller memory and development time, an interpolation technique applied to these values can be used. By choosing 16 to 32 equally-spaced values from the manufacturer's lookup tables over a desired temperature range, using a simple linear approximation of intervals between is generally very precise.

# PACKAGE OPTION ADDENDUM

25-Jul-2011

## PACKAGING INFORMATION

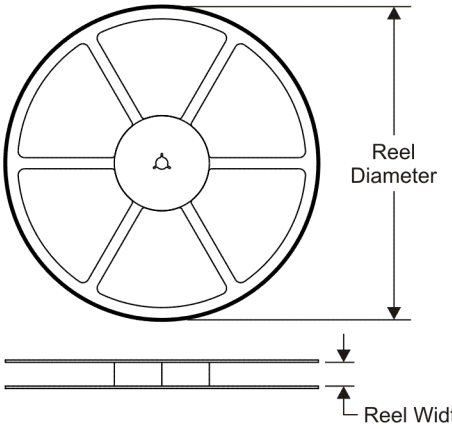
| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/ Ball Finish | MSL Peak Temp [3] | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| ADS1118IDGSR | ACTIVE | MSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| ADS1118IDGST | ACTIVE | MSOP | DGS | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| ADS1118IRUGR | PREVIEW | X2QFN | RUG | 10 | | TBD | Call TI | Call TI | |
| ADS1118IRUGT | PREVIEW | X2QFN | RUG | 10 | | TBD | Call TI | Call TI | |

# PACKAGE MATERIALS INFORMATION

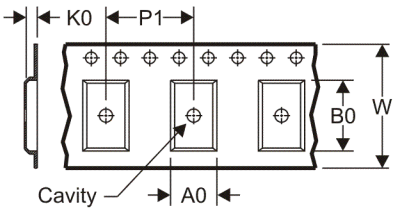
22-Jul-2011

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

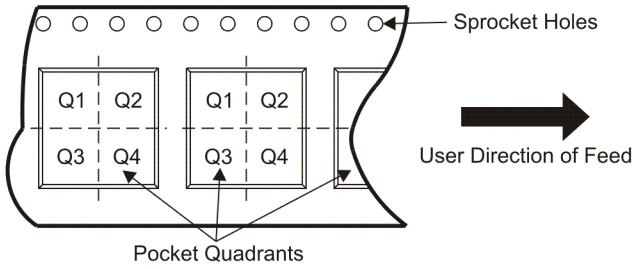



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



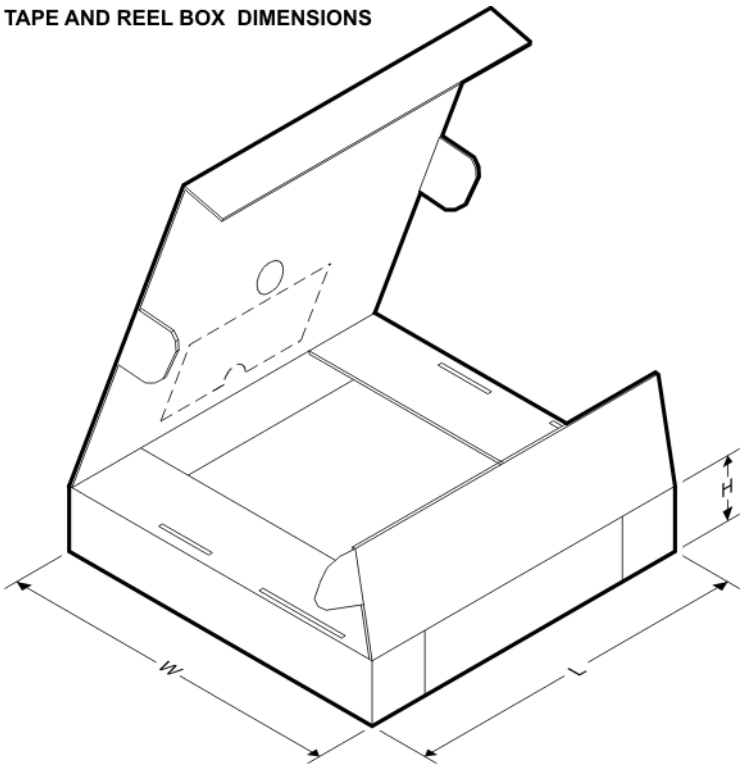

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS1118IDGSR | MSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| ADS1118IDGST | MSOP | DGS | 10 | 250 | 180.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

22-Jul-2011

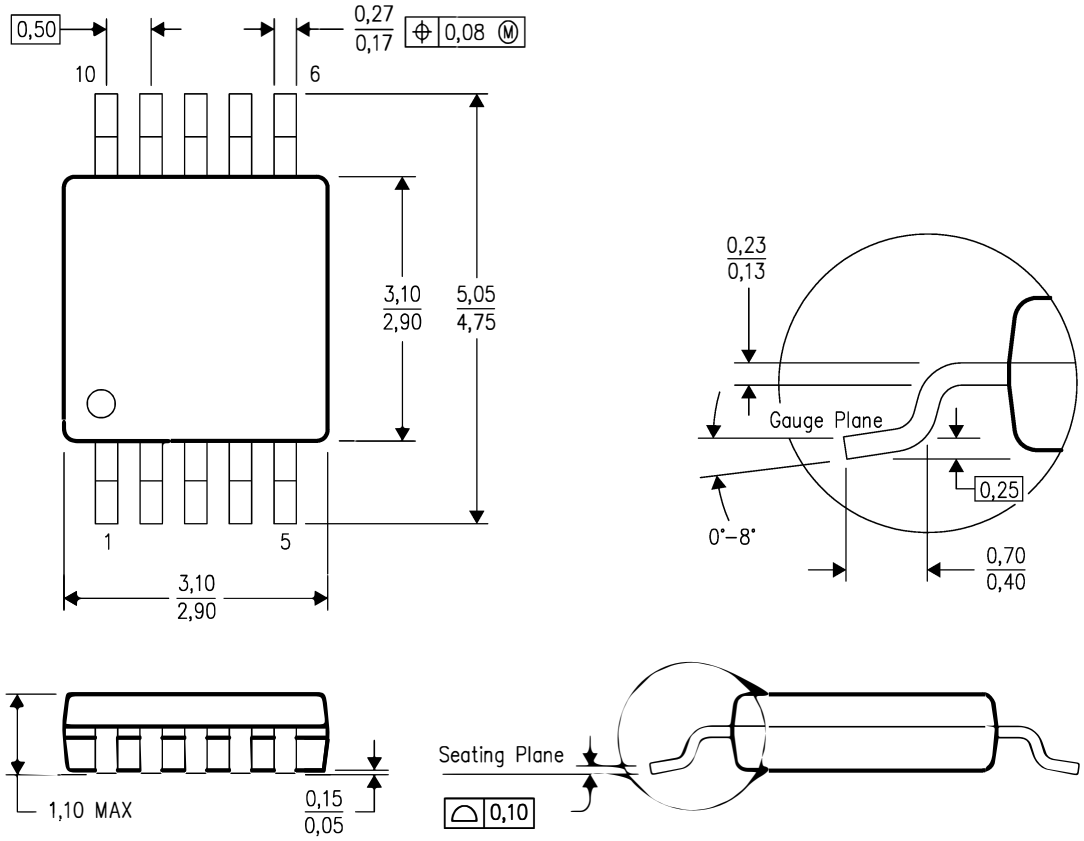
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS1118IDGSR | MSOP | DGS | 10 | 2500 | 370.0 | 355.0 | 55.0 |
| ADS1118IDGST | MSOP | DGS | 10 | 250 | 195.0 | 200.0 | 45.0 |

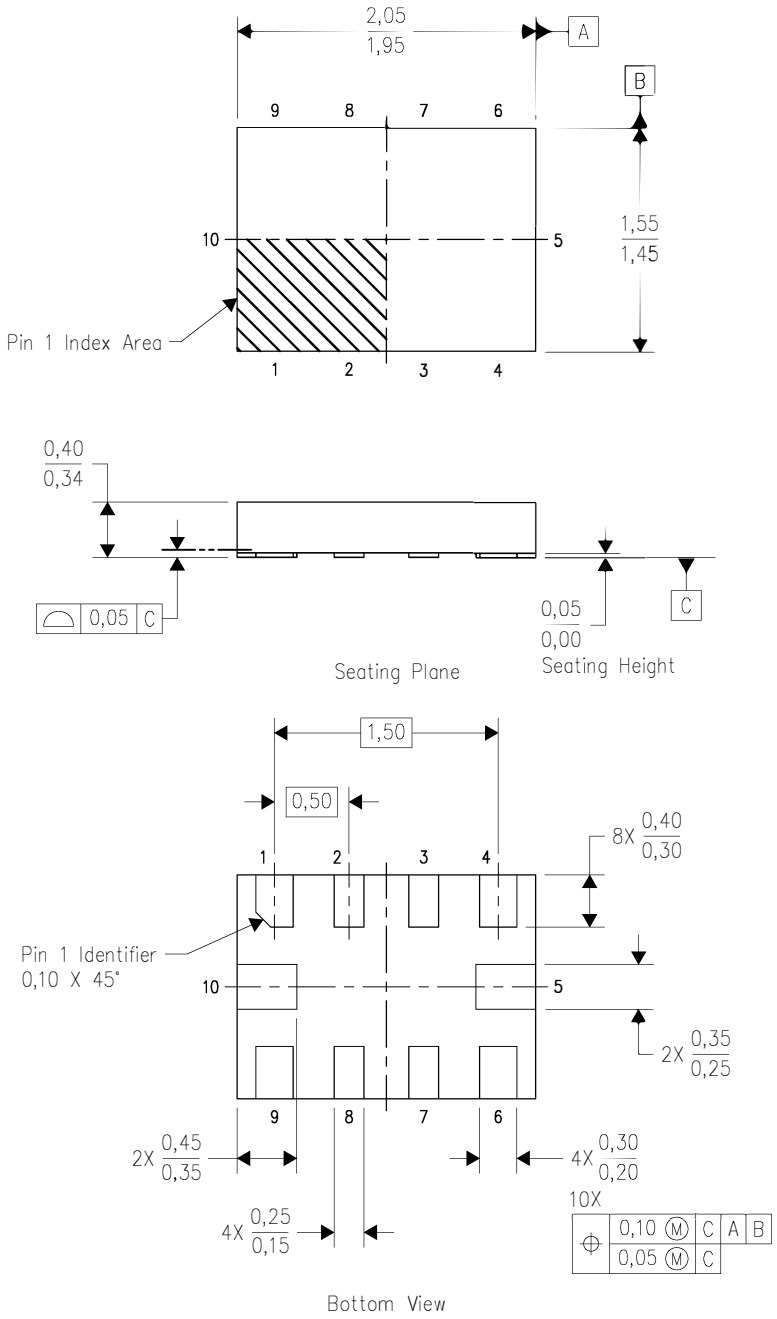
## DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE




4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK




4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.