LMP202x Zero-Drift, Low-Noise, EMI-Hardened Amplifiers

1 Features

(Typical Values, T_A = 25°C, V_S = 5 V)

- Input Offset Voltage (Typical) −0.4 µV
- Input Offset Voltage (Max) ±5 µV
- Input Offset Voltage Drift (Typical) –0.004 µV/°C
- Input Offset Voltage Drift (Max) ±0.02 µV/°C
- Input Voltage Noise, A_V = 1000 11 nV/√Hz
- Open Loop Gain 160 dB
- CMRR 139 dB
- PSRR 130 dB
- Supply Voltage Range 2.2 V to 5.5 V
- Supply Current (per Amplifier) 1.1 mA
- Input Bias Current ±25 pA
- GBW 5 MHz
- Slew Rate 2.6 V/µs
- Operating Temperature Range −40°C to 125°C
- 5-Pin SOT-23, 8-Pin VSSOP and 8-Pin SOIC Packages

2 Applications

- Precision Instrumentation Amplifiers
- Battery Powered Instrumentation
- Thermocouple Amplifiers
- Bridge Amplifiers

3 Description

The LMP2021 and LMP2022 are single and dual precision operational amplifiers offering ultra low input offset voltage, near zero input offset voltage drift, very low input voltage noise and very high open loop gain. They are part of the LMP™ precision family and are ideal for instrumentation and sensor interfaces.

The LMP202x has only 0.004 µV/°C of input offset voltage drift, and 0.4 µV of input offset voltage. These attributes provide great precision in high accuracy applications.

The proprietary continuous auto zero correction circuitry ensures impressive CMRR and PSRR, removes the 1/f noise component, and eliminates the need for calibration in many circuits.

With only 260 nV_{PP} (0.1 Hz to 10 Hz) of input voltage noise and no 1/f noise component, the LMP202x are suitable for low frequency applications such as industrial precision weigh scales. The extremely high open loop gain of 160 dB drastically reduces gain error in high gain applications. With ultra precision DC specifications and very low noise, the LMP202x are ideal for position sensors, bridge sensors, pressure sensors, medical equipment and other high accuracy applications with very low error budgets.

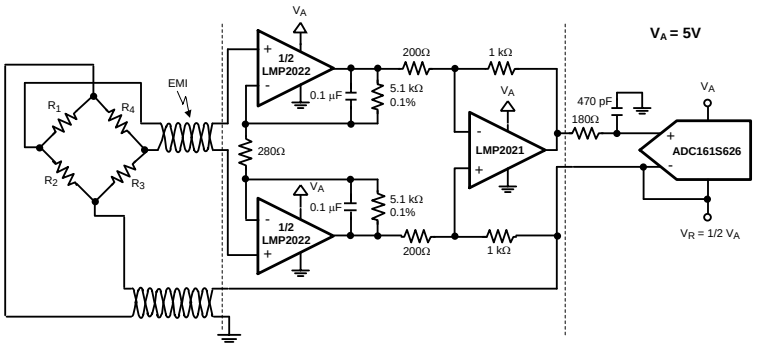
The LMP2021 is offered in 5-Pin SOT-23 and 8-Pin SOIC packages. The LMP2022 is offered in 8-Pin VSSOP and 8-Pin SOIC packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP2021	SOIC (8)	4.90 mm x 3.91 mm
	SOT-23 (5)	2.90 mm x 1.60 mm
LMP2022	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Bridge Amplifier



The LMP202x support systems with up to 24 bits of accuracy.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (December 2014) to Revision G **Page**

- Deleted SC-70 and VSSOP references from LMP2021 pinout descriptions ... 3
- Deleted DCK and DGK packages and corrected SOT-23 pin function table for LMP2021 ... 3

Changes from Revision E (March 2013) to Revision F **Page**

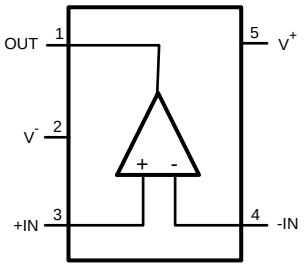
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision D (March 2013) to Revision E **Page**

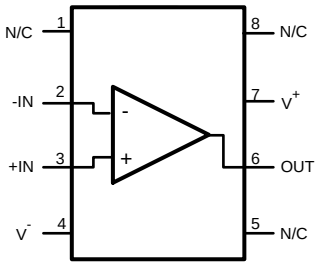
- Changed layout of National Data Sheet to TI format ... 23

5 Pin Configuration and Functions

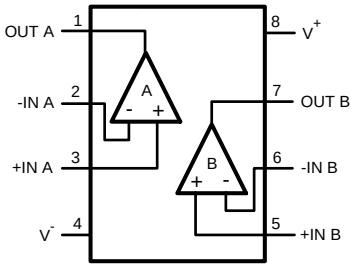
DVB Package: LMP2021
5 Pin SOT-23
TOP VIEW



D Package: LMP2021
8 Pin SOIC
TOP VIEW



D and DGK Packages: LMP2022
8 Pin VSSOP or SOIC
TOP VIEW



Pin Functions: LMP2021

PIN			I/O	DESCRIPTION
NAME	LMP2021			
	DBV	D		
OUT	1	6	I	Output
+IN	3	3	I	Non-Inverting Input
-IN	4	2	O	Inverting Input
V-	2	4	P	Negative Supply
V+	5	7	P	Positive Supply
N/C	-	1	-	No Internal Connection
N/C	-	5	-	No Internal Connection
N/C	-	8	-	No Internal Connection

Pin Functions: LMP2022

PIN		I/O	DESCRIPTION
NAME	LMP2022		
	D, DGK		
+IN A	3	I	Non-Inverting input, channel A
+IN B	5	I	Non-Inverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	P	Positive (highest) power supply
V–	4	P	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

		MIN	MAX	UNIT
V_{IN} Differential		$-V_S$	V_S	
Supply Voltage ($V_S = V^+ - V^-$)			6.0	V
All Other Pins		$V^+ + 0.3$	$V^- - 0.3$	V
Output Short-Circuit Duration to V^+ or V^-[3]			5	seconds
Junction Temperature[4]			150	°C
Soldering Information	Infrared or Convection (20 sec)		235	°C
	Wave Soldering Lead Temperature (10 sec)		260	°C
T_{stg}	Storage temperature range	−65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Package power dissipation should be observed.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta J_A$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Temperature Range	−40	125	°C
Supply Voltage ($V_S = V^+ - V^-$)	2.2	5.5	V

6.4 Thermal Information

THERMAL METRIC[1]		LMP2021, LMP2022	LMP2021	LMP2022	UNIT
		D	DBV	DGK	
		8 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106	164	217	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: 2.5 V(1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 2.5 V, V^- = 0 V, V_{CM} = V^+/2, R_L >10 kΩ to V^+/2.

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage			–5	–0.9	5	µV
		–40°C ≤ T_J ≤ 125°C		–10		10	
TCV_{OS}	Input Offset Voltage Drift(4)			–0.02	0.001	0.02	µV/°C
I_B	Input Bias Current			–100	±23	100	pA
		–40°C ≤ T_J ≤ 125°C		–300		300	
I_{OS}	Input Offset Current			–200	±57	200	pA
		–40°C ≤ T_J ≤ 125°C		–250		250	
CMRR	Common Mode Rejection Ratio	−0.2 V ≤ V_{CM} ≤ 1.7 V, 0 V ≤ V_{CM} ≤ 1.5 V		105	141		dB
		−0.2 V ≤ V_{CM} ≤ 1.7 V, 0 V ≤ V_{CM} ≤ 1.5 V, –40°C ≤ T_J ≤ 125°C		102			
CMVR	Input Common-Mode Voltage Range	Large Signal CMRR ≥ 105 dB		−0.2		1.7	V
		Large Signal CMRR ≥ 102 dB, –40°C ≤ T_J ≤ 125°C		0		1.5	
EMIRR	Electro-Magnetic Interference Rejection Ratio(5)	IN+ and IN−	$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 400 MHz		40		dB
			$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 900 MHz		48		
			$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 1800 MHz		67		
			$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 2400 MHz		79		
PSRR	Power Supply Rejection Ratio	2.5 V ≤ V^+ ≤ 5.5 V, V_{CM} = 0		115	130		dB
		2.5 V ≤ V^+ ≤ 5.5 V, V_{CM} = 0 , –40°C ≤ T_J ≤ 125°C		112			
		2.2 V ≤ V^+ ≤ 5.5 V, V_{CM} = 0		110	130		
A_{VOL}	Large Signal Voltage Gain	R_L = 10 kΩ to V^+/2, V_{OUT} = 0.5 V to 2 V		124	150		dB
		R_L = 10 kΩ to V^+/2, V_{OUT} = 0.5 V to 2 V, –40°C ≤ T_J ≤ 125°C		119			
		R_L = 2 kΩ to V^+/2, V_{OUT} = 0.5 V to 2 V		120	150		
		R_L = 2 kΩ to V^+/2, V_{OUT} = 0.5 V to 2 V, –40°C ≤ T_J ≤ 125°C		115			
V_{OUT}	Output Swing High	R_L = 10 kΩ to V^+/2			38	50	mV from either rail
		R_L = 10 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				70	
		R_L = 2 kΩ to V^+/2			62	85	
		R_L = 2 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				115	
	Output Swing Low	R_L = 10 kΩ to V^+/2			30	45	
		R_L = 10 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				55	
		R_L = 2 kΩ to V^+/2			58	75	
		R_L = 2 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				95	
I_{OUT}	Linear Output Current	Sourcing, V_{OUT} = 2 V		30	50		mA
		Sinking, V_{OUT} = 0.5 V		30	50		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are specified by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) The EMI Rejection Ratio is defined as EMIRR = 20Log ($V_{RF-PEAK}/\Delta V_{OS}$).

Electrical Characteristics: 2.5 V(1) (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 2.5 V, V^- = 0 V, V_{CM} = V^+/2, R_L >10 kΩ to V^+/2.

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
I_S	Supply Current	Per Amplifier		0.95	1.10	mA
		Per Amplifier, –40°C ≤ T_J ≤ 125°C			1.37	
SR	Slew Rate(6)	A_V = +1, C_L = 20 pF, R_L = 10 kΩ V_O = 2 V_{PP}		2.5		V/µs
GBW	Gain Bandwidth Product	C_L = 20 pF, R_L = 10 kΩ		5		MHz
G_M	Gain Margin	C_L = 20 pF, R_L = 10 kΩ		10		dB
Φ_M	Phase Margin	C_L = 20 pF, R_L = 10 kΩ		60		deg
C_{IN}	Input Capacitance	Common Mode		12		pF
		Differential Mode		12		
e_n	Input-Referred Voltage Noise Density	f = 0.1 kHz or 10 kHz, A_V = 1000		11		nV/√Hz
		f = 0.1 kHz or 10 kHz, A_V = 100		15		
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz		260		nV_{PP}
		0.01 Hz to 10 Hz		330		
I_n	Input-Referred Current Noise	f = 1 kHz		350		fA/√Hz
t_r	Recovery time	to 0.1%, R_L = 10 kΩ, A_V = −50, V_{OUT} = 1.25 V_{PP} Step, Duration = 50 µs		50		µs
CT	Cross Talk	LMP2022, f = 1 kHz		150		dB

(6) The number specified is the average of rising and falling slew rates and is measured at 90% to 10%.

6.6 Electrical Characteristics: 5 V[1]

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, R_L > 10 kΩ to V^+/2.

PARAMETER		TEST CONDITIONS		MIN[2]	TYP[3]	MAX[2]	UNIT
V_{OS}	Input Offset Voltage			–5	−0.4	5	µV
		–40°C ≤ T_J ≤ 125°C		–10		10	
TCV_{OS}	Input Offset Voltage Drift[4]			–0.02	−0.004	0.02	µV/°C
I_B	Input Bias Current			–100	±25	100	pA
		–40°C ≤ T_J ≤ 125°C		–300		300	
I_{OS}	Input Offset Current			–200	±48	200	pA
		–40°C ≤ T_J ≤ 125°C		–250		250	
CMRR	Common Mode Rejection Ratio	−0.2 V ≤ V_{CM} ≤ 4.2 V, 0 V ≤ V_{CM} ≤ 4.0 V		120	139		dB
		−0.2 V ≤ V_{CM} ≤ 4.2 V, 0 V ≤ V_{CM} ≤ 4.0 V, –40°C ≤ T_J ≤ 125°C		115			
CMVR	Input Common-Mode Voltage Range	Large Signal CMRR ≥ 120 dB		–0.2		4.2	V
		Large Signal CMRR ≥ 115 dB, –40°C ≤ T_J ≤ 125°C		0		4.0	
EMIRR	Electro-Magnetic Interference Rejection Ratio[5]	IN+ and IN−	$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 400 MHz		58		dB
			$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 900 MHz		64		
			$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 1800 MHz		72		
			$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 2400 MHz		82		
PSRR	Power Supply Rejection Ratio	2.5 V ≤ V^+ ≤ 5.5 V, V_{CM} = 0		115	130		dB
		2.5 V ≤ V^+ ≤ 5.5 V, V_{CM} = 0, –40°C ≤ T_J ≤ 125°C		112			
		2.2 V ≤ V^+ ≤ 5.5 V, V_{CM} = 0		110	130		
A_{VOL}	Large Signal Voltage Gain	R_L = 10 kΩ to V^+/2, V_{OUT} = 0.5 V to 4.5 V		125	160		dB
		R_L = 10 kΩ to V^+/2, V_{OUT} = 0.5 V to 4.5 V, –40°C ≤ T_J ≤ 125°C		120			
		R_L = 2 kΩ to V^+/2, V_{OUT} = 0.5 V to 4.5 V		123	160		
		R_L = 2 kΩ to V^+/2, V_{OUT} = 0.5 V to 4.5 V, –40°C ≤ T_J ≤ 125°C		118			
V_{OUT}	Output Swing High	R_L = 10 kΩ to V^+/2			83	135	mV from either rail
		R_L = 10 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				170	
		R_L = 2 kΩ to V^+/2			120	160	
		R_L = 2 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				204	
	Output Swing Low	R_L = 10 kΩ to V^+/2			65	80	
		R_L = 10 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				105	
		R_L = 2 kΩ to V^+/2			103	125	
		R_L = 2 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				158	
I_{OUT}	Linear Output Current	Sourcing, V_{OUT} = 4.5 V		30	50		mA
		Sinking, V_{OUT} = 0.5 V		30	50		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are specified by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) The EMI Rejection Ratio is defined as EMIRR = 20Log ($V_{RF-PEAK}/\Delta V_{OS}$).

Electrical Characteristics: 5 V[(1)] (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, R_L > 10 kΩ to V^+/2.

PARAMETER		TEST CONDITIONS	MIN[(2)]	TYP[(3)]	MAX[(2)]	UNIT
I_S	Supply Current	Per Amplifier		1.1	1.25	mA
		Per Amplifier, –40°C ≤ T_J ≤ 125°C			1.57	
SR	Slew Rate[(6)]	A_V = +1, C_L = 20 pF, R_L = 10 kΩ V_O = 2 V_{PP}		2.6		V/µs
GBW	Gain Bandwidth Product	C_L = 20 pF, R_L = 10 kΩ		5		MHz
G_M	Gain Margin	C_L = 20 pF, R_L = 10 kΩ		10		dB
Φ_M	Phase Margin	C_L = 20 pF, R_L = 10 kΩ		60		deg
C_{IN}	Input Capacitance	Common Mode		12		pF
		Differential Mode		12		
e_n	Input-Referred Voltage Noise Density	f = 0.1 kHz or 10 kHz, A_V= 1000		11		nV/√Hz
		f = 0.1 kHz or 10 kHz, A_V= 100		15		
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz Noise		260		nV_{PP}
		0.01 Hz to 10 Hz Noise		330		
I_n	Input-Referred Current Noise	f = 1 kHz		350		fA/√Hz
t_r	Input Overload Recovery time	to 0.1%, R_L = 10 kΩ, A_V = −50, V_{OUT} = 2.5 V_{PP} Step, Duration = 50 µs		50		µs
CT	Cross Talk	LMP2022, f = 1 kHz		150		dB

(6) The number specified is the average of rising and falling slew rates and is measured at 90% to 10%.

6.7 Typical Characteristics

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – V^-, V_S= 5 V, V_{CM} = V_S/2.

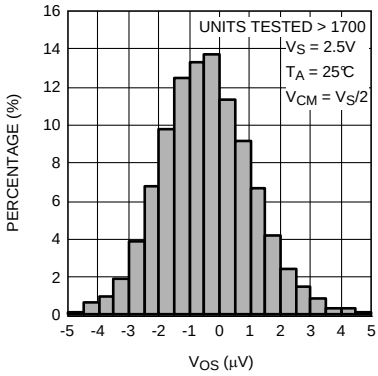


Figure 1. Offset Voltage Distribution

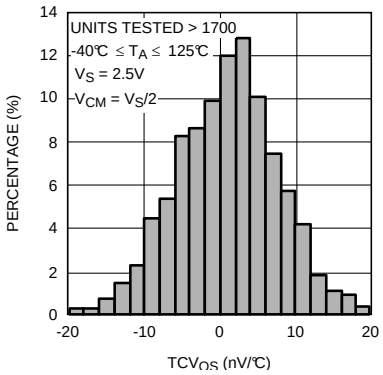


Figure 2. TCV_{OS} Distribution

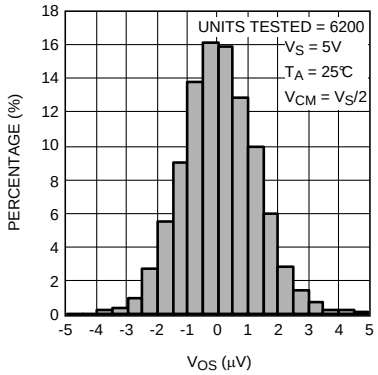


Figure 3. Offset Voltage Distribution

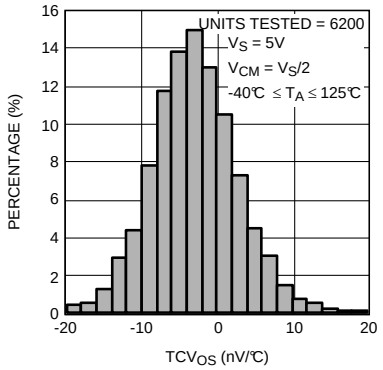


Figure 4. TCV_{OS} Distribution

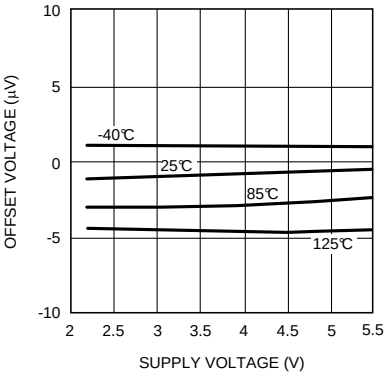


Figure 5. Offset Voltage vs. Supply Voltage

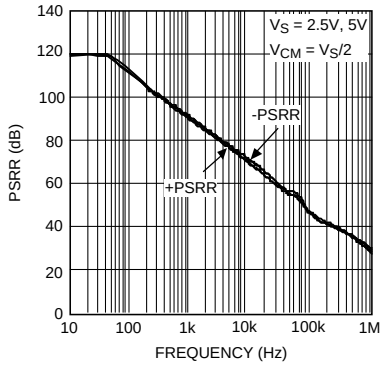


Figure 6. PSRR vs. Frequency

Typical Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – $V^–$, V_S= 5 V, V_{CM} = V_S/2.

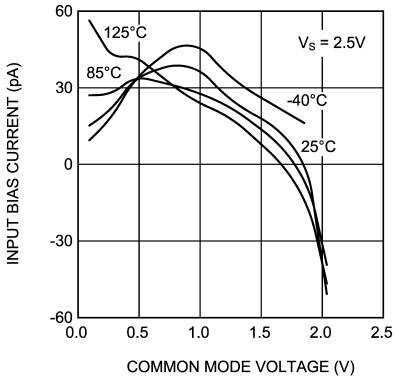


Figure 7. Input Bias Current vs. V_{CM}

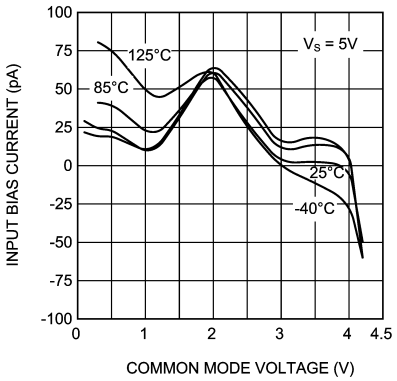


Figure 8. Input Bias Current vs. V_{CM}

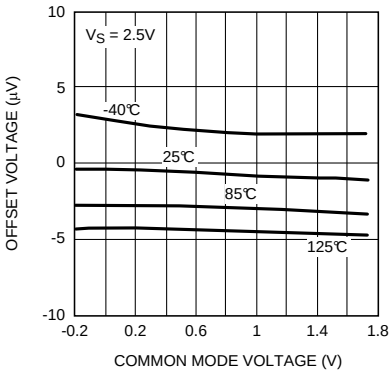


Figure 9. Offset Voltage vs. V_{CM}

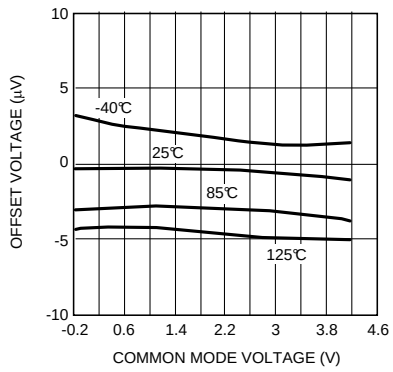


Figure 10. Offset Voltage vs. V_{CM}

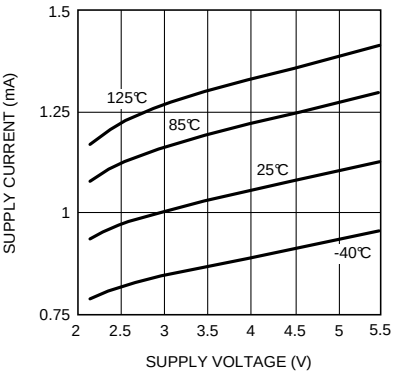


Figure 11. Supply Current vs. Supply Voltage (Per Amplifier)

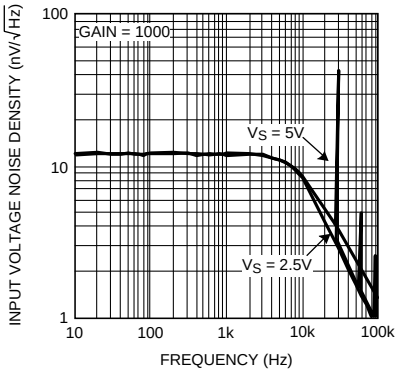


Figure 12. Input Voltage Noise vs. Frequency

Typical Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – $V^–$, V_S= 5 V, V_{CM} = V_S/2.

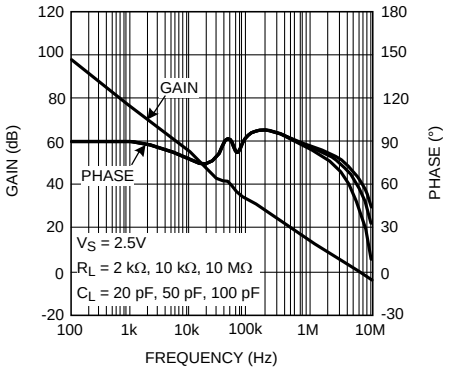


Figure 13. Open Loop Frequency Response

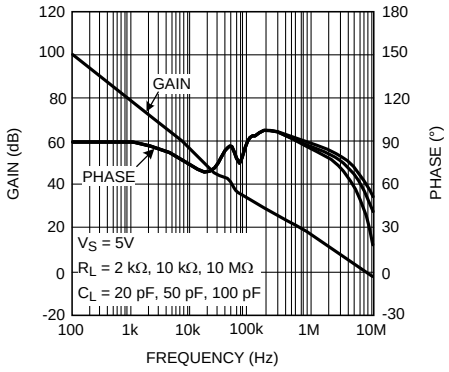


Figure 14. Open Loop Frequency Response

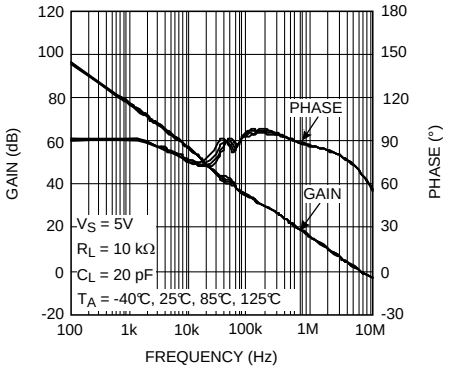


Figure 15. Open Loop Frequency Response Over Temperature

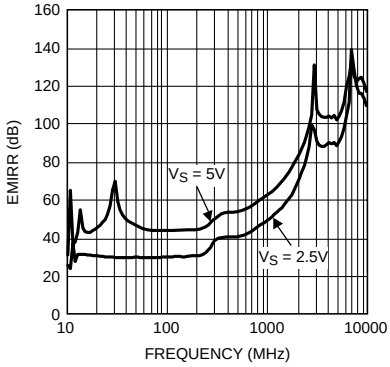


Figure 16. EMIRR vs. Frequency

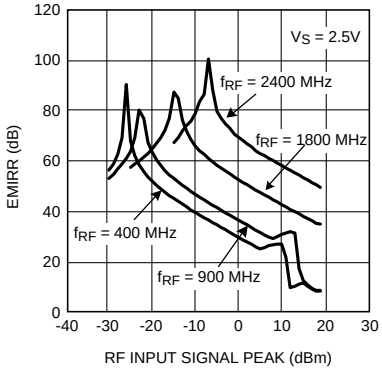


Figure 17. EMIRR vs. Input Power

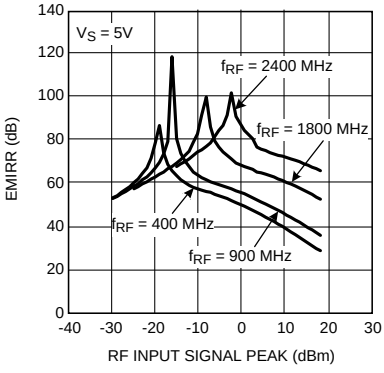


Figure 18. EMIRR vs. Input Power

Typical Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – V^-, V_S= 5 V, V_{CM} = V_S/2.

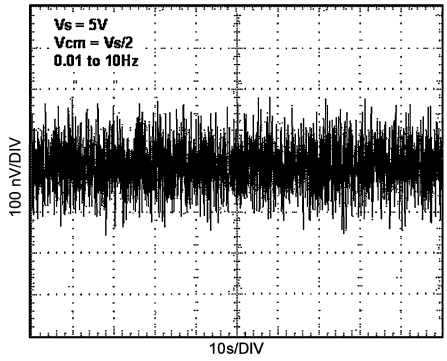


Figure 19. Time Domain Input Voltage Noise

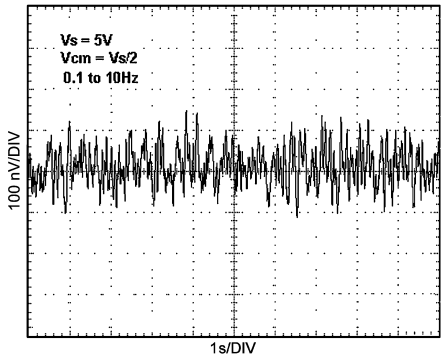


Figure 20. Time Domain Input Voltage Noise

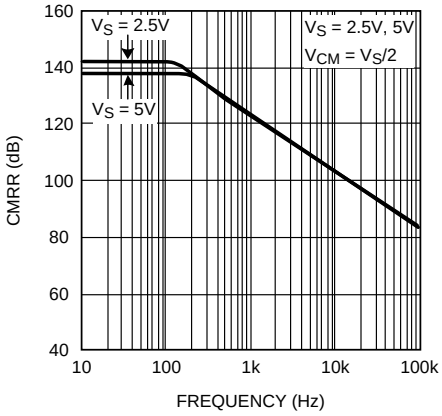


Figure 21. CMRR vs. Frequency

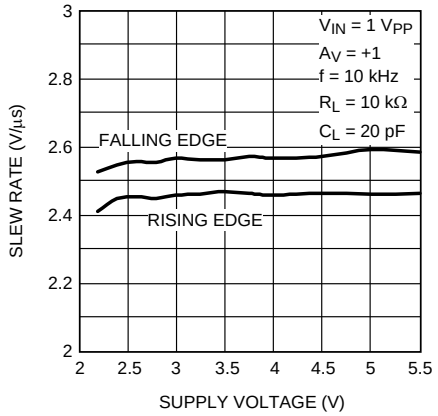


Figure 22. Slew Rate vs. Supply Voltage

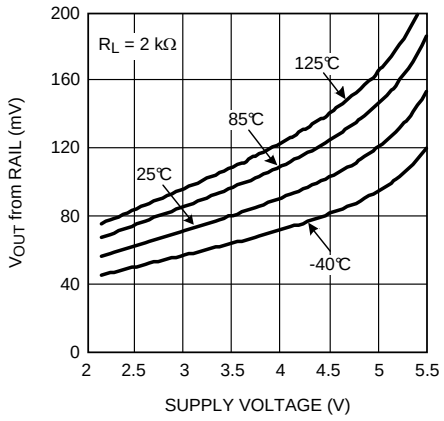


Figure 23. Output Swing High vs. Supply Voltage

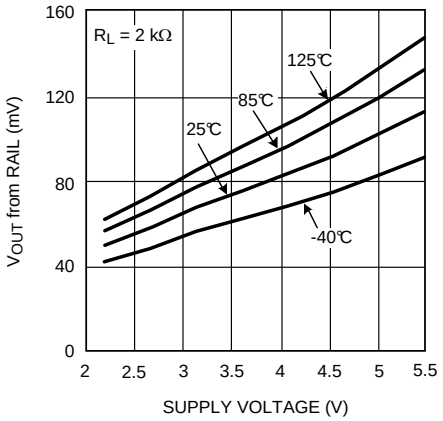


Figure 24. Output Swing Low vs. Supply Voltage

Typical Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – V^-, V_S= 5 V, V_{CM} = V_S/2.

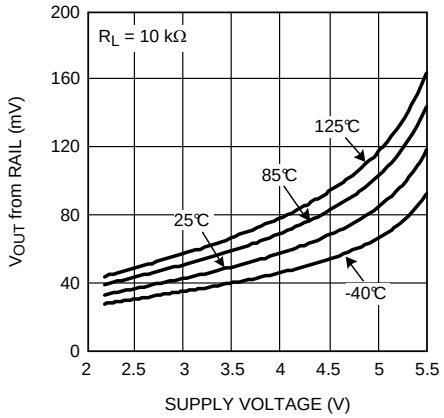


Figure 25. Output Swing High vs. Supply Voltage

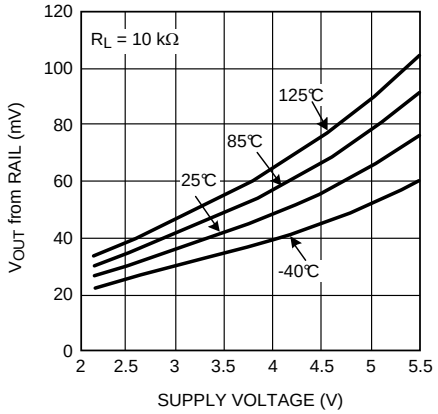


Figure 26. Output Swing Low vs. Supply Voltage

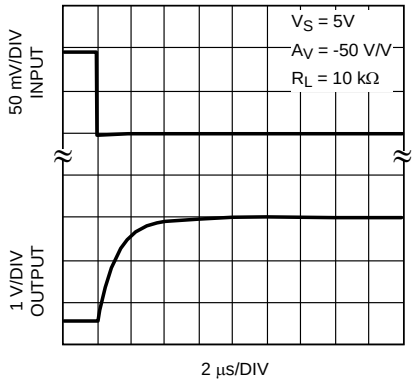


Figure 27. Overload Recovery Time

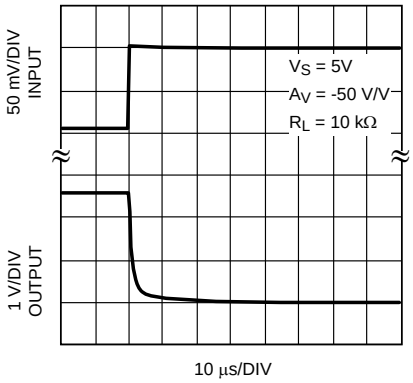


Figure 28. Overload Recovery Time

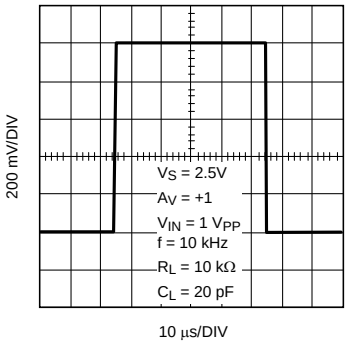


Figure 29. Large Signal Step Response

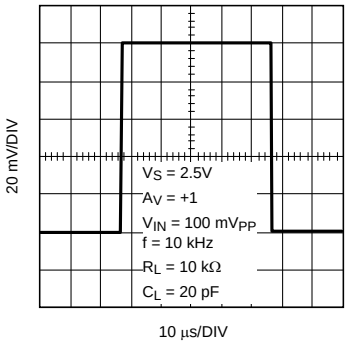


Figure 30. Small Signal Step Response

Typical Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – $V^–$, V_S= 5 V, V_{CM} = V_S/2.

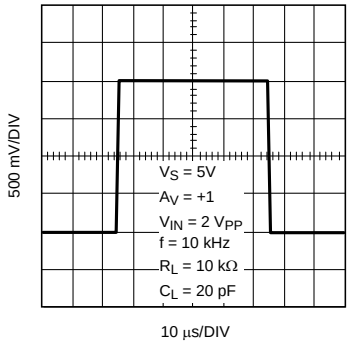


Figure 31. Large Signal Step Response

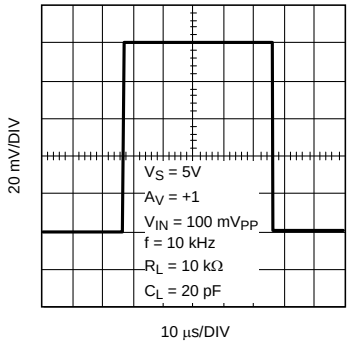


Figure 32. Small Signal Step Response

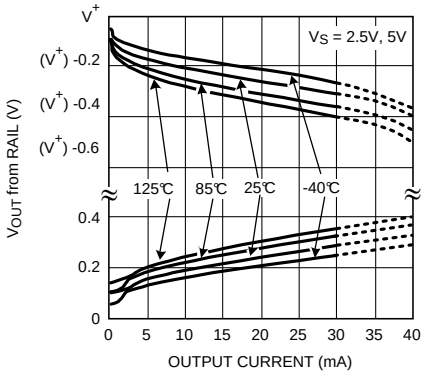


Figure 33. Output Voltage vs. Output Current

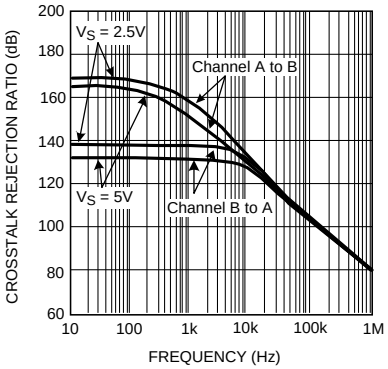


Figure 34. Cross Talk Rejection Ratio vs. Frequency (LMP2022)

7 Detailed Description

7.1 Overview

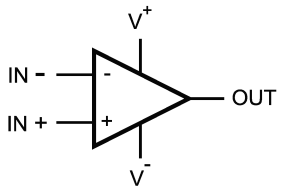
The LMP202x are single and dual precision operational amplifiers with ultra low offset voltage, ultra low offset voltage drift, and very low input voltage noise with no 1/f and extended supply voltage range. The LMP202x offer on chip EMI suppression circuitry which greatly enhances the performance of these precision amplifiers in the presence of radio frequency signals and other high frequency disturbances.

The LMP202x utilize proprietary auto zero techniques to measure and continuously correct the input offset error voltage. The LMP202x have a DC input offset voltage with a maximum value of ±5 µV and an input offset voltage drift maximum value of 0.02 µV/°C. The input voltage noise of the LMP202x is less than 11 nV/$\sqrt{Hz}$ at a voltage gain of 1000 V/V and has no flicker noise component. This makes the LMP202x ideal for high accuracy, low frequency applications where lots of amplification is needed and the input signal has a very small amplitude.

The proprietary input offset correction circuitry enables the LMP202x to have superior CMRR and PSRR performances. The combination of an open loop voltage gain of 160 dB, CMRR of 142 dB, PSRR of 130 dB, along with the ultra low input offset voltage of only −0.4 µV, input offset voltage drift of only −0.004 µV/°C, and input voltage noise of only 260 nV_{PP} at 0.1 Hz to 10 Hz make the LMP202x great choices for high gain transducer amplifiers, ADC buffer amplifiers, DAC I-V conversion, and other applications requiring precision and long-term stability. Other features are rail-to-rail output, low supply current of 1.1 mA per amplifier, and a gain-bandwidth product of 5 MHz.

The LMP202x have an extended supply voltage range of 2.2 V to 5.5 V, making them ideal for battery operated portable applications. The LMP2021 is offered in 5-pin SOT-23 and 8-pin SOIC packages. The LMP2022 is offered in 8-pin VSSOP and 8-Pin SOIC packages.

7.2 Functional Block Diagram



7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (–IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp Vout is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ - IN^-) \quad (1)$$

where A_{OL} is the open-loop gain of the amplifier, typically around 100dB (100,000x, or 10uV per Volt).

7.4 Device Functional Modes

7.4.1 EMI Suppression

The near-ubiquity of cellular, Bluetooth, and Wi-Fi signals and the rapid rise of sensing systems incorporating wireless radios make electromagnetic interference (EMI) an evermore important design consideration for precision signal paths. Though RF signals lie outside the op amp band, RF carrier switching can modulate the DC offset of the op amp. Also some common RF modulation schemes can induce down-converted components. The added DC offset and the induced signals are amplified with the signal of interest and thus corrupt the measurement. The LMP202x use on chip filters to reject these unwanted RF signals at the inputs and power supply pins; thereby preserving the integrity of the precision signal path.

Device Functional Modes (continued)

Twisted pair cabling and the active front-end's common-mode rejection provide immunity against low frequency noise (i.e. 60 Hz or 50 Hz mains) but are ineffective against RF interference. Figure 46 displays this. Even a few centimeters of PCB trace and wiring for sensors located close to the amplifier can pick up significant 1 GHz RF. The integrated EMI filters of LMP202x reduce or eliminate external shielding and filtering requirements, thereby increasing system robustness. A larger EMIRR means more rejection of the RF interference. For more information on EMIRR, please refer to AN-1698 (Literature Number SNOA497).

7.4.2 Input Voltage Noise

The input voltage noise density of the LMP202x has no 1/f corner, and its value depends on the feedback network used. This feature of the LMP202x differentiates this family from other products currently available from other vendors. In particular, the input voltage noise density decreases as the closed loop voltage gain of the LMP202x increases. The input voltage noise of the LMP202x is less than 11 nV/√Hz when the closed loop voltage gain of the op amp is 1000. Higher voltage gains are required for smaller input signals. When the input signal is smaller, a lower input voltage noise is quite advantageous and increases the signal to noise ratio.

Figure 35 shows the input voltage noise of the LMP202x as the closed loop gain increases.

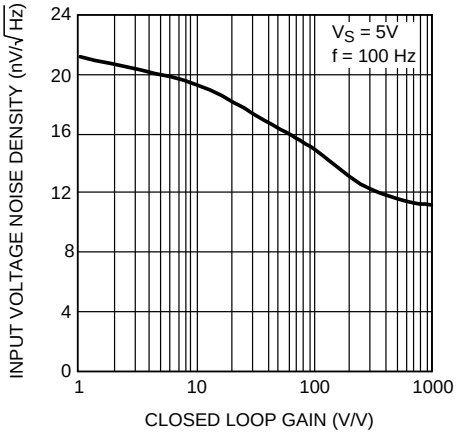


Figure 35. Input Voltage Noise Density decreases with Gain

Figure 36 shows the input voltage noise density does not have the 1/f component.

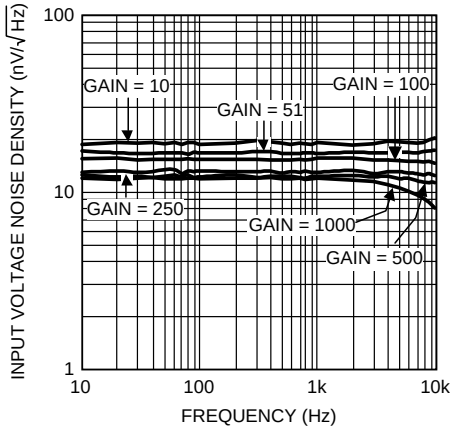


Figure 36. Input Voltage Noise Density with no 1/f

With smaller and smaller input signals and high precision applications with lower error budget, the reduced input voltage noise and no 1/f noise allow more flexibility in circuit design.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Achieving Lower Noise With Filtering

The low input voltage noise of the LMP202x, and no 1/f noise make these suitable for many applications with noise sensitive designs. Simple filtering can be done on the LMP202x to remove high frequency noise. Figure 37 shows a simple circuit that achieves this.

In Figure 37 C_F and the corner frequency of the filter resulting from C_F and R_F will reduce the total noise.

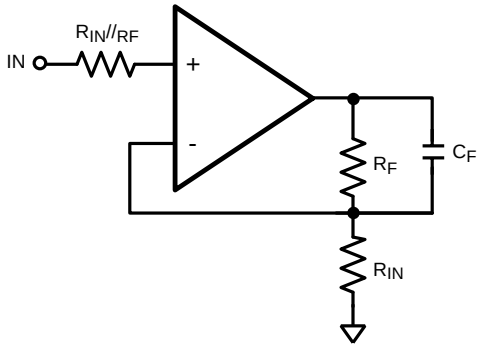


Figure 37. Noise Reducing Filter for Lower Gains

In order to achieve lower noise floors for even more noise stringent applications, a simple filter can be added to the op amp's output after the amplification stage. Figure 38 shows the schematic of a simple circuit which achieves this objective. Low noise amplifiers such as the LMV771 can be used to create a single pole low pass filter on the output of the LMP202x. The noise performance of the filtering amplifier, LMV771 in this circuit, will not be dominant as the input signal on LMP202x has already been significantly gained up and as a result the effect of the input voltage noise of the LMV771 is effectively not noticeable.

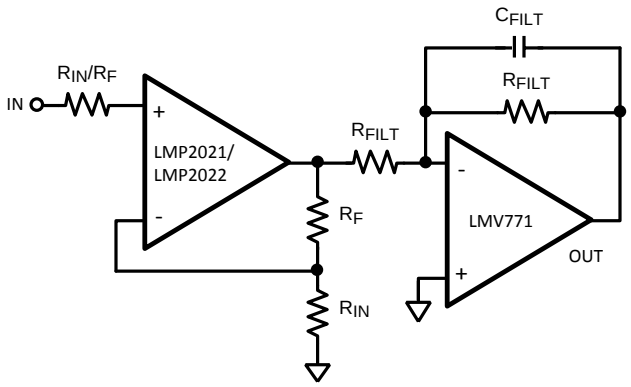


Figure 38. Enhanced Filter to Further Reduce Noise at Higher Gains

Application Information (continued)

Using the circuit in Figure 38 has the advantage of removing the non-linear filter bandwidth dependency which is seen when the circuit in Figure 37 is used. The difference in noise performance of the circuits in Figure 37 and Figure 38 becomes apparent only at higher gains. At voltage gains of 10 V/V or less, there is no difference between the noise performance of the two circuits.

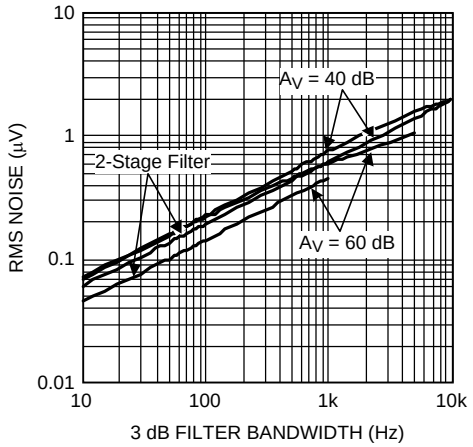


Figure 39. RMS Input Referred Noise vs. Frequency

Figure 39 shows the total input referred noise vs. 3 dB corner of both filters of Figure 37 and Figure 38 at gains of 100V/V and 1000V/V. For these measurements and using Figure 37's circuit, R_F = 49.7 kΩ and R_{IN} = 497Ω. Value of C_F has been changed to achieve the desired 3 dB filter corner frequency. In the case of Figure 38's circuit, R_F = 49.7 kΩ and R_{IN} = 497Ω, R_{FILT} = 49.7 kΩ, and C_{FILT} has been changed to achieve the desired 3 dB filter corner frequency. Figure 39 compares the RMS noise of these two circuits. As Figure 39 shows, the RMS noise measured the circuit in Figure 38 has lower values and also depicts a more linear shape.

8.1.2 Input Bias Current

The bias current of the LMP202x behaves differently than a conventional amplifier due to the dynamic transient currents created on the input of an auto-zero circuit. The input bias current is affected by the charge and discharge current of the input auto-zero circuit. This effectivly creates a repetitive impulse current noise of 100's of pA. For this reason, the LMP202x is *not* recommeded for source impedances of 1 MΩ or greater.

The amount of current sunk or sourced from that stage is dependent on the combination of input impedance (resistance *and* capacitance), as well as the balance and matching of these impedances across the two inputs. This current, integrated by the input capacitence, causes a shift in the apparent "bias current". Because of this, there is an apparent "bias current vs. input impedance" interaction. In the LMP202x for an input resistive impedance of 1 GΩ, the shift in input bias current can be up to 40 pA. This input bias shift is caused by varying the input's capacitive impedance. Since the input bias current is dependent on the input impedance, it is difficult to estimate what the actual bias current is without knowing the end circuit and associated capacitive strays.

Figure 40 shows the input bias current of the LMP202x and that of another commercially available amplifier from a competitor. As it can be seen, the shift in LMP202x bias current is much lower than that of other chopper style or auto zero amplifiers available from other vendors.

Application Information (continued)

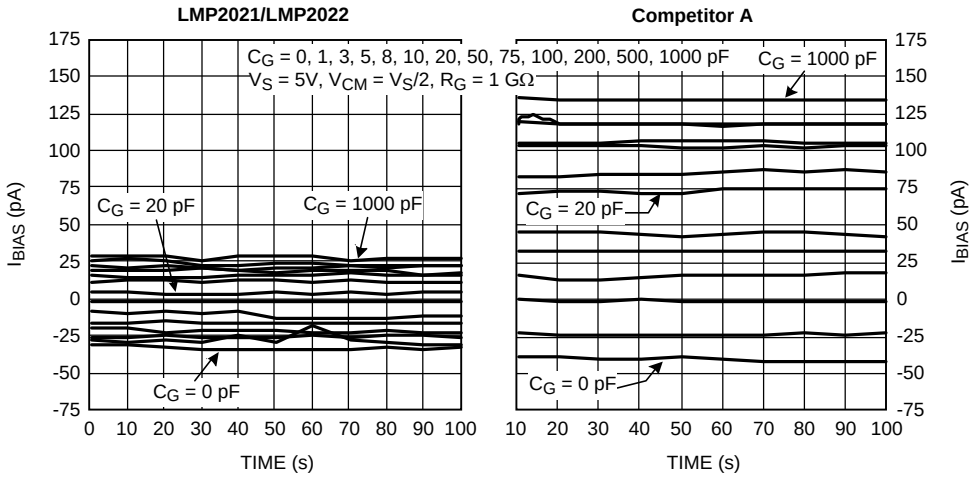


Figure 40. Input Bias Current of LMP202x is lower than Competitor A

8.1.3 Lowering the Input Bias Current

As mentioned in the *Input Bias Current* section, the input bias current of an auto zero amplifier such as the LMP202x varies with input impedance and feedback impedance. Once the value of a certain input resistance, i.e. sensor resistance, is known, it is possible to optimize the input bias current for this fixed input resistance by choosing the capacitance value that minimizes that current. Figure 41 shows the input bias current vs. input impedance of the LMP202x. The value of R_G or input resistance in this test is 1 GΩ. When this value of input resistance is used, and when a parallel capacitance of 22 pF is placed on the circuit, the resulting input bias current is nearly 0 pA. Figure 41 can be used to extrapolate capacitor values for other sensor resistances. For this purpose, the total impedance seen by the input of the LMP202x needs to be calculated based on Figure 41. By knowing the value of R_G, one can calculate the corresponding C_G which minimizes the non-inverting input bias current, positive bias current, value.

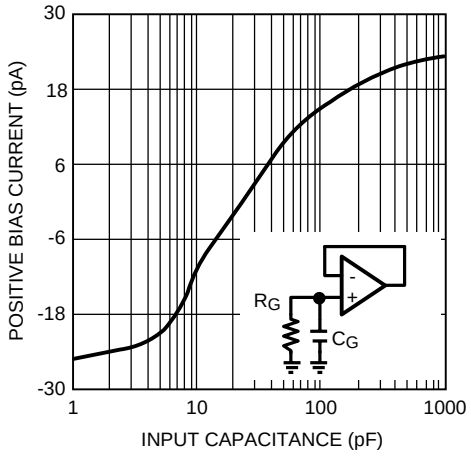


Figure 41. Input Bias Current vs. C_G with R_G = 1 GΩ

In a typical I-V converter, the output voltage will be the sum of DC offset plus bias current and the applied signal through the feedback resistor. In a conventional input stage, the inverting input's capacitance has very little effect on the circuit. This effect is generally on settling time and the dielectric soakage time and can be ignored. In auto zero amplifiers, the input capacitance effect will add another term to the output. This additional term means that the baseline reading on the output will be dependent on the input capacitance. The term input capacitance for this purpose includes circuit strays and any input cable capacitances. There is a slight variation in the capacitive

Application Information (continued)

offset as the duty cycle and amplitude of the pulses vary from part to part, depending on the correction at the time. The lowest input current will be obtained when the impedances, both resistive and capacitive, are matched between the inputs. By balancing the input capacitances, the effect can be minimized. A simple way to balance the input impedance is adding a capacitance in parallel to the feedback resistance. The addition of this feedback capacitance reduces the bias current and increases the stability of the operational amplifier. Figure 42 shows the input bias current of the LMP202x when R_F is set to 1 GΩ. As it can be seen from Figure 42, choosing the optimum value of C_F will help reducing the input bias current.

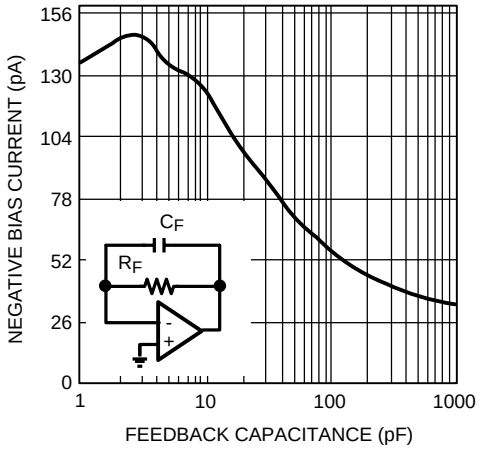


Figure 42. Input Bias Current vs. C_F with R_F = 1 GΩ

The effect of bias current on a circuit can be estimated with the following:

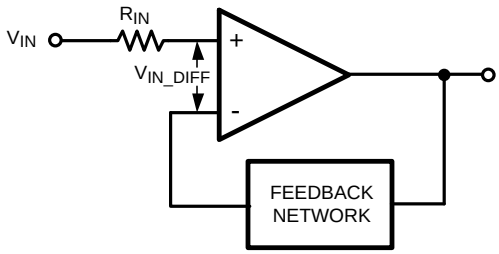
$$A_V*I_{BIAS+}*Z_S - I_{BIAS-}*Z_F \quad (2)$$

Where A_V is the closed loop gain of the system and I_{BIAS+} and I_{BIAS-} denote the positive and negative bias current, respectively. It is common to show the average of these bias currents in product datasheets. If I_{BIAS+} and I_{BIAS-} are not individually specified, use the I_{BIAS} value provided in datasheet graphs or tables for this calculation.

For the application circuit shown in Figure 46, the LMP2022 amplifiers each have a gain of 18. With a sensor impedance of 500Ω for the bridge, and using the above equation, the total error due to the bias current on the outputs of the LMP2022 amplifier will be less than 200 nV.

8.1.4 Sensor Impedance

The sensor resistance, or the resistance connected to the inputs of the LMP202x, contributes to the total impedance seen by the auto correcting input stage.



Application Information (continued)

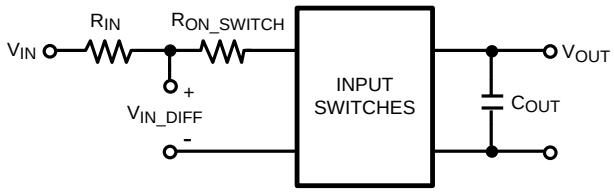


Figure 43. Auto Correcting Input Stage Model

As shown in Figure 43, the sum of R_{IN} and $R_{ON\text{-}SWITCH}$ will form a low pass filter with C_{OUT} during correction cycles. As R_{IN} increases, the time constant of this filter increases, resulting in a slower output signal which could have the effect of reducing the open loop gain, A_{VOL}, of the LMP202x. In order to prevent this reduction in A_{VOL} in presence of high impedance sensors or other high resistances connected to the input of the LMP202x, a capacitor can be placed in parallel to this input resistance. This is shown in Figure 44.

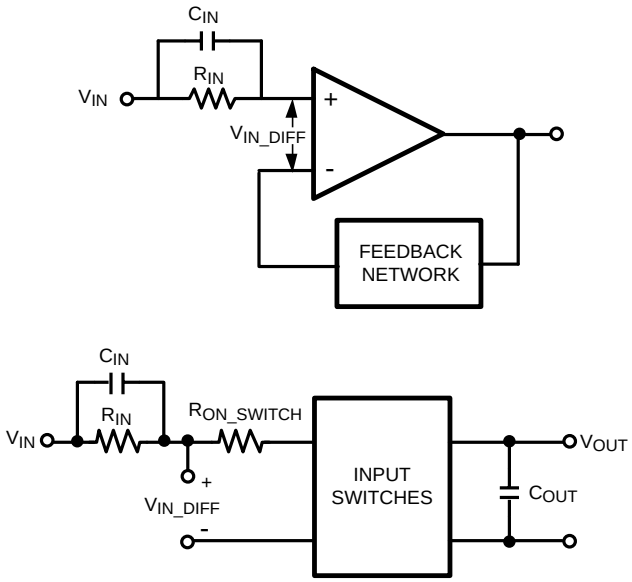


Figure 44. Sensor Impedance with Parallel Capacitance

C_{IN} in Figure 44 adds a zero to the low pass filter and hence eliminating the reduction in A_{VOL} of the LMP202x. An alternative circuit to achieve this is shown in Figure 45.

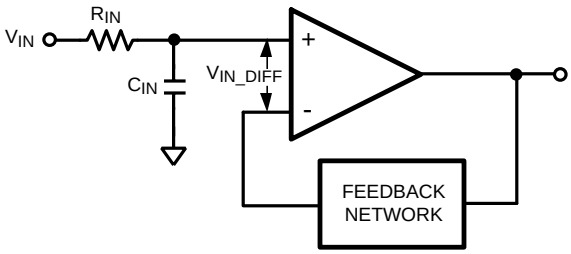


Figure 45. Alternative Sensor Impedance Circuit

Application Information (continued)

8.1.5 Transient Response to Fast Inputs

On chip continuous auto zero correction circuitry eliminates the 1/f noise and significantly reduces the offset voltage and offset voltage drift; all of which are very low frequency events. For slow changing sensor signals this correction is transparent. For excitations which may otherwise cause the output to swing faster than 40 mV/µs, there are additional considerations which can be viewed two perspectives: for sine waves and for steps.

For sinusoidal inputs, when the output is swinging rail-to-rail on ±2.5-V supplies, the auto zero circuitry will introduce distortions above 2.55 kHz. For smaller output swings, higher frequencies can be amplified without the auto zero slew limitation as shown in table below. Signals above 20 kHz, are not affected, though normally, closed loop bandwidth should be kept below 20 kHz so as to avoid aliasing from the auto zero circuit.

$V_{OUT-PEAK}$ (V)	$f_{MAX-SINE\ WAVE}$ (kHz)
0.32	20
1	6.3
2.5	2.5

For step-like inputs, such as those arising from disturbances to a sensing system, the auto zero slew rate limitation manifests itself as an extended ramping and settling time, lasting ~100 µs.

8.1.6 Digital Acquisition Systems

High resolution ADC's with 16-bits to 24-bits of resolution can be limited by the noise of the amplifier driving them. The circuit configuration, the value of the resistors used and the source impedance seen by the amplifier can affect the noise of the amplifier. The total noise at the output of the amplifier can be dominated by one of several sources of noises such as: white noise or broad band noise, 1/f noise, thermal noise, and current noise. In low frequency applications such as medical instrumentation, the source impedance is generally low enough that the current noise coupled into it does not impact the total noise significantly. However, as the 1/f or flicker noise is paramount to many application, the use of an auto correcting stabilized amplifier like the LMP202x reduces the total noise.

Table 1 summarizes the input and output referred RMS noise values for the LMP202x compared to that of Competitor A. As described in previous sections, the outstanding noise performance of the LMP202x can be even further improved by adding a simple low pass filter following the amplification stage.

The use of an additional filter, as shown in Figure 38 benefits applications with higher gain. For this reason, at a gain of 10, only the results of circuit in Figure 37 are shown. The RMS input noise of the LMP202x are compared with Competitor A's input noise performance. Competitor A's RMS input noise behaves the same with or without an additional filter.

Table 1. RMS Input Noise Performance

Amplifier Gain (V/V)	System Bandwidth Requirement (Hz)	RMS Input Noise (nV)		
		LMP202x		Competitor A
		Figure 37 Circuit	Figure 38 Circuit	Figure 37, Figure 38 Circuit
10	100	229	See(1)	300
	1000	763	See(1)	1030
100	100	229	196	300
	1000	763	621	1030
1000	10	71	46	95
	100	158	146	300
	1000	608	462	1030

(1) No significant difference in Noise measurements at A_V = 10V/V

8.2 Typical Application

Figure 46 shows the Bridge Sensor Interface for these devices.

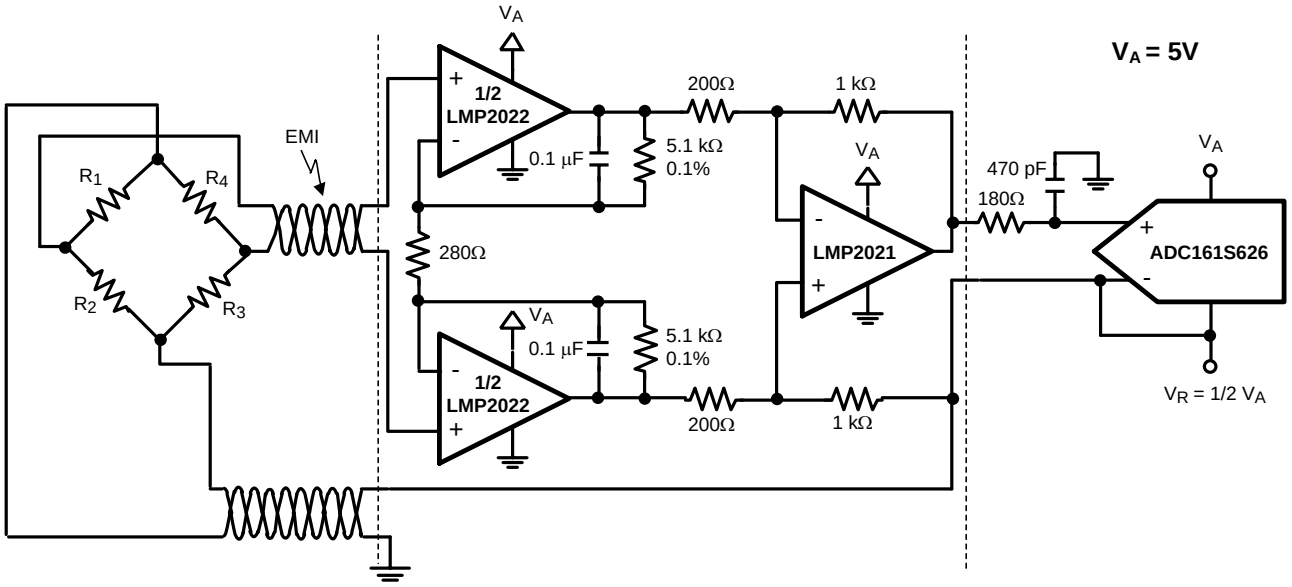


Figure 46. LMP202x Used With ADC161S626

8.2.1 Design Requirements

Bridge sensors are used in a variety of applications such as pressure sensors and weigh scales. Bridge sensors typically have a very small differential output signal. This very small differential signal needs to be accurately amplified before it can be fed into an ADC. As discussed in the previous sections, the accuracy of the op amp used as the ADC driver is essential to maintaining total system accuracy.

The high DC performance of the LMP202x make these amplifiers ideal choices for use with a bridge sensor. The LMP202x have very low input offset voltage and very low input offset voltage drift. The open loop gain of the LMP202x is 160 dB.

The circuit in Figure 46 shows a signal path solution for a typical bridge sensor using the LMP202x. Bridge sensors are created by replacing at least one of the resistors in a typical bridge with a sensor whose resistance varies in response to an external stimulus. For this example, the expected bridge output signal will be in the range of ±12 mV. This signal must be accurately amplified by the amplifier to best match the dynamic input range of the ADC. This is done by using one LMP2022 and one LMP2021 in front of the ADC161S626.

The on chip EMI rejection filters available on the LMP202x help remove the EMI interference introduced to the signal and hence improve the overall system performance.

8.2.2 Detailed Design Procedure

The amplification of this ±12 mV signal is achieved in 2 stages and through a three op-amp instrumentation amplifier. The dual LMP2022 in Figure 46 amplifies each side of the differential output of the bridge sensor by a gain of 18.2. Using the LMP2022 with a gain of 18.2 reduces the input referred voltage noise of the op amps and the system as a result. Also, this gain allows direct filtering of the signal on the LMP2022 without compromising noise performance. The differential output of the two amplifiers in the LMP2022 are then fed into a LMP2021 configured as a difference amplifier. This stage has a gain of 5, with a total system having a gain of (18.2 * 2 +1) * 5 = 187. The LMP2021 has an outstanding CMRR value of 139. This impressive CMRR improves system performance by removing the common mode signal introduced by the bridge. With an overall gain of 187, the ±12 mV differential input signal is gained up to ±2.24V (0.26 V to 4.74V single ended). This utilizes the amplifiers output swing as well as the ADC's input dynamic range, and allows for some overload range.

Typical Application (continued)

Bridge sensor measurements are usually done up to 10s of Hz. Placing a 300 Hz filter on the LMP2022 helps removing the higher frequency noise from this circuit. This filter is created by placing two capacitors in the feedback path of the LMP2022 amplifiers.

This amplified signal is then fed into the ADC161S626. The ADC161S626 is a 16-bit, 50 kSPS to 250 kSPS 5V ADC. In order to utilize the maximum number of bits of the ADC161S626 in this configuration, a 2.5V reference voltage is used. This 2.5V reference is also used to power the bridge sensor and the inverting input of the ADC. Using the same voltage source for these three points helps reducing the total system error by eliminating error due to source variations.

With this system, the output signal of the bridge sensor which can be up to ±13.3 mV and is accurately scaled to the full scale range of the ADC and then digitized for further processing. The LMP202x introduced minimal error to the system and improved the signal quality by removing common mode signals and high frequency noise.

8.2.3 Application Curve

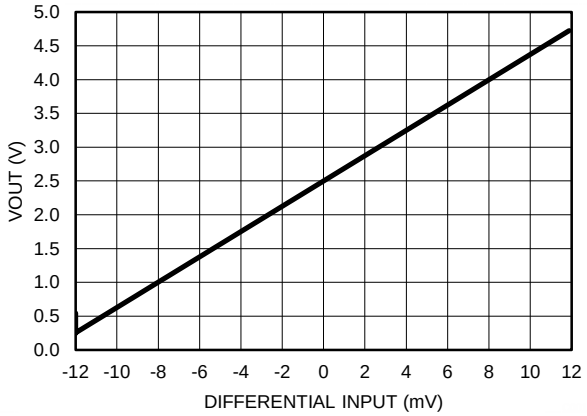


Figure 47. Single Ended Output Results for Bridge Circuit

9 Power Supply Recommendations

The LMP202x is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V) over a –40°C to +125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 6 V can permanently damage the device.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

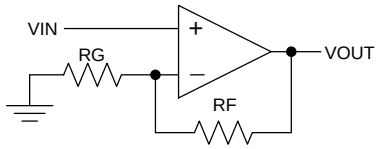
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective

Layout Guidelines (continued)

methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to SLOA089, *Circuit Board Layout Techniques*.

- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *Typical Characteristics*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example



(Schematic Representation)

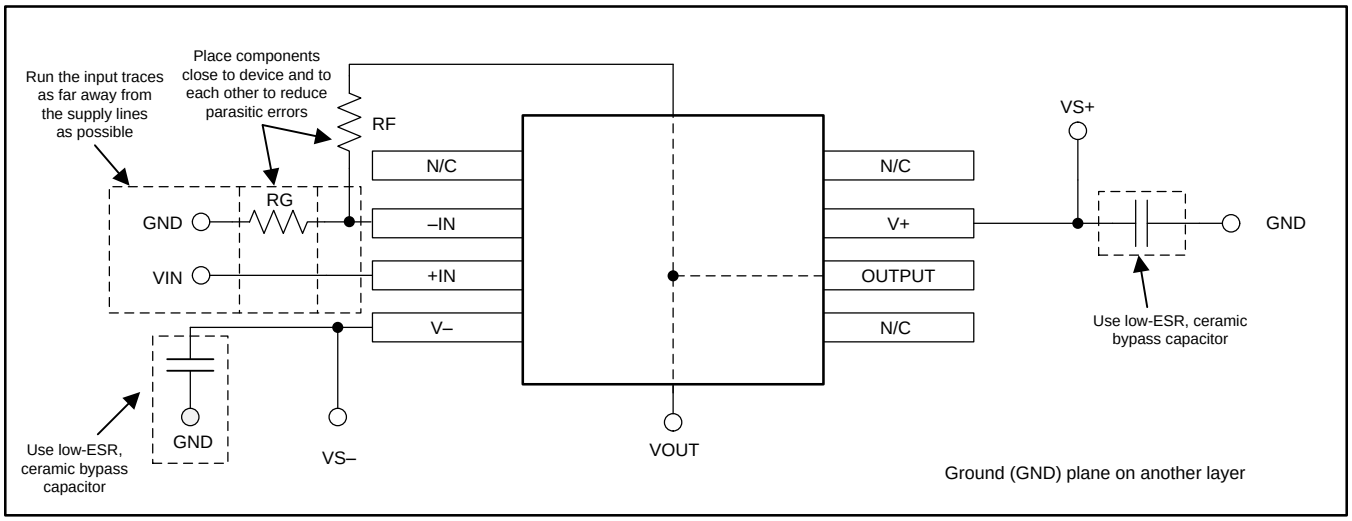


Figure 48. Operational Amplifier Board Layout for Noninverting Configuration

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMP2021	Click here	Click here	Click here	Click here	Click here
LMP2022	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

LMP is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP2021MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP20 21MA	Samples
LMP2021MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP20 21MA	Samples
LMP2021MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AF5A	Samples
LMP2021MFE/NOPB	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AF5A	Samples
LMP2021MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AF5A	Samples
LMP2022MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP20 22MA	Samples
LMP2022MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP20 22MA	Samples
LMP2022MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AV5A	Samples
LMP2022MME/NOPB	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AV5A	Samples
LMP2022MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AV5A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

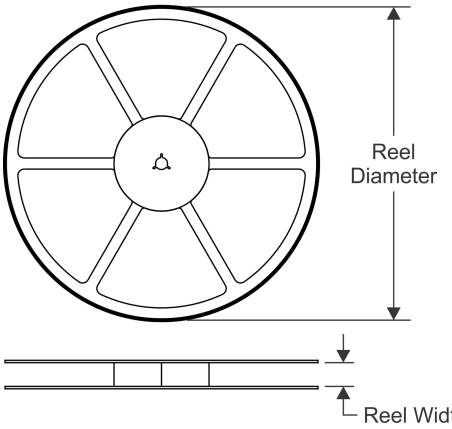
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

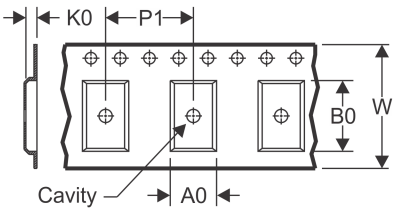
9-Apr-2022

TAPE AND REEL INFORMATION

REEL DIMENSIONS

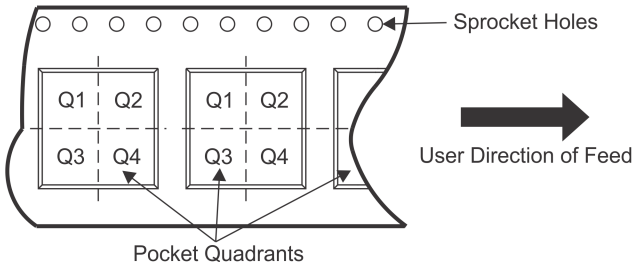


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



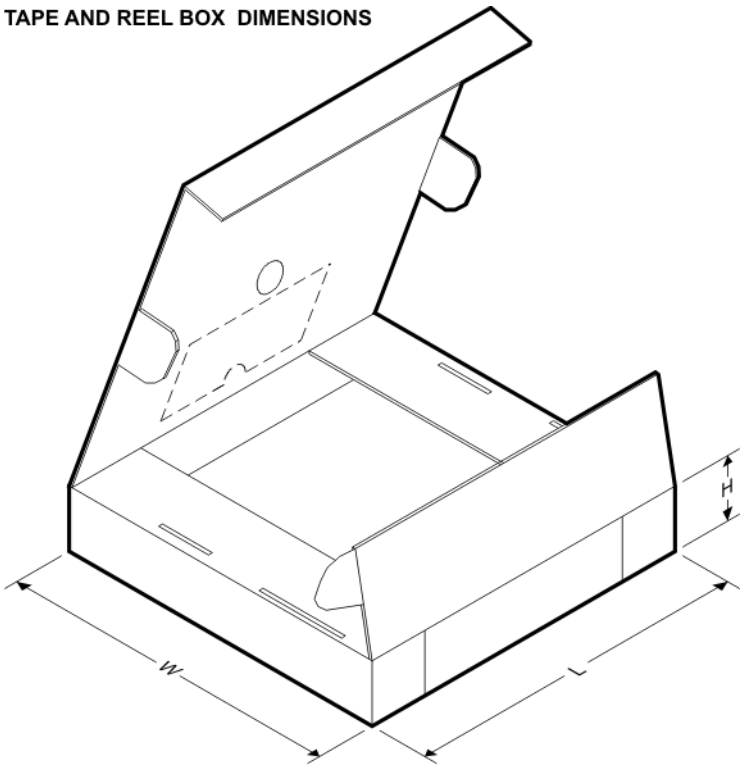
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP2021MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP2021MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2021MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2021MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2022MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP2022MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP2022MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP2022MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

9-Apr-2022

TAPE AND REEL BOX DIMENSIONS



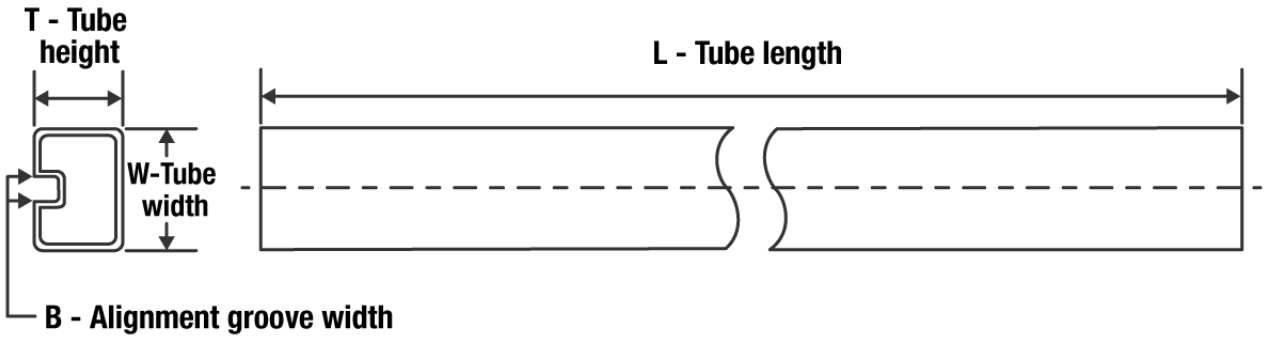
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP2021MAX/NOPB	SOIC	D	8	2500	356.0	356.0	35.0
LMP2021MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMP2021MFE/NOPB	SOT-23	DBV	5	250	208.0	191.0	35.0
LMP2021MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMP2022MAX/NOPB	SOIC	D	8	2500	356.0	356.0	35.0
LMP2022MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMP2022MME/NOPB	VSSOP	DGK	8	250	208.0	191.0	35.0
LMP2022MMX/NOPB	VSSOP	DGK	8	3500	356.0	356.0	35.0

PACKAGE MATERIALS INFORMATION

9-Apr-2022

TUBE



*All dimensions are nominal

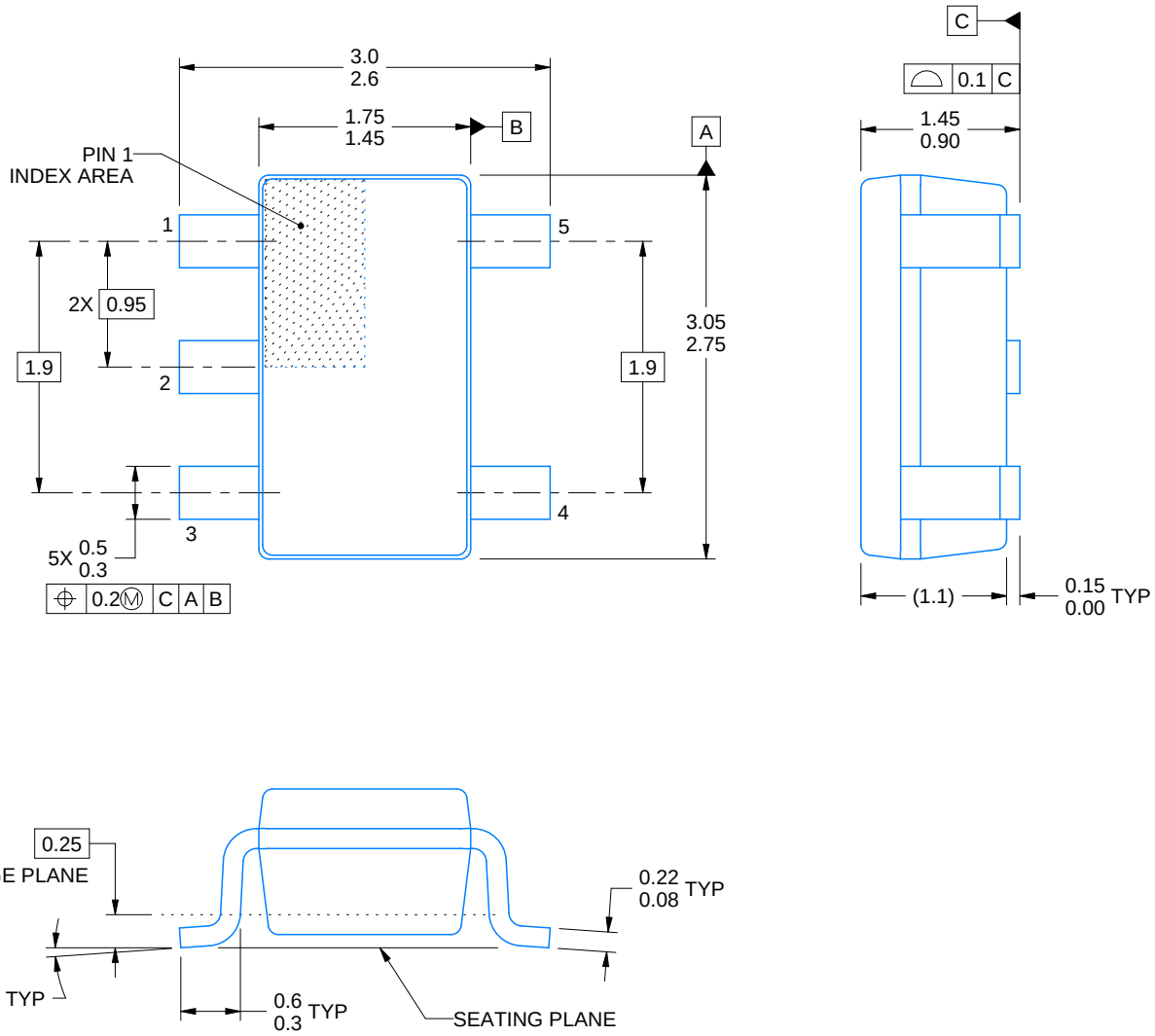
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMP2021MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMP2022MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

NOTES:

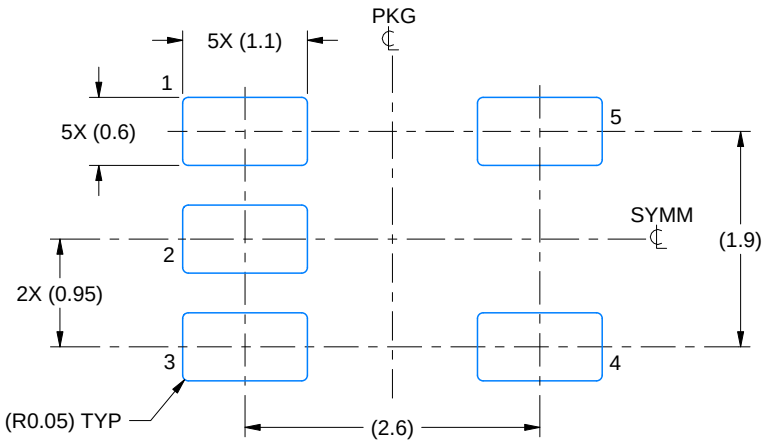
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

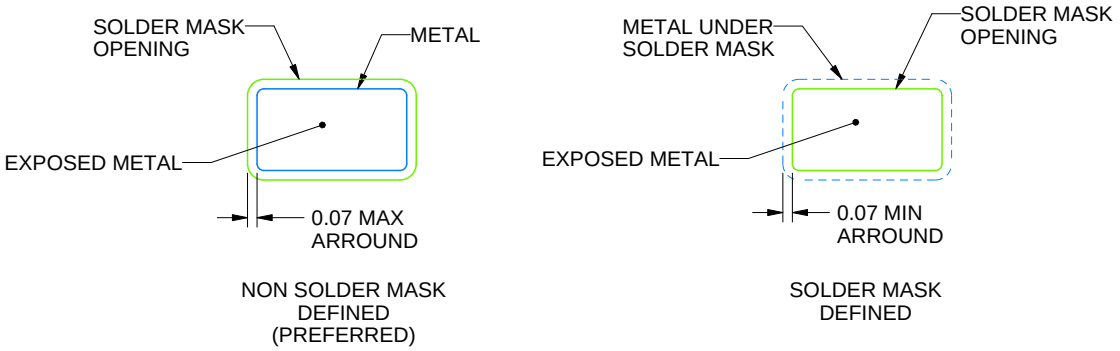
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

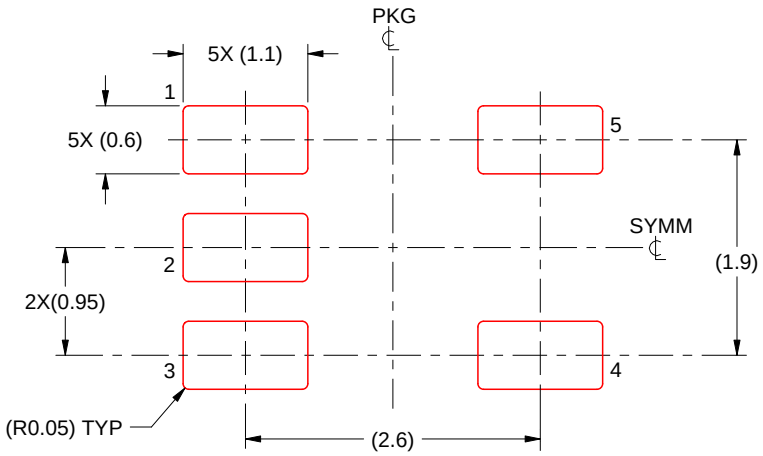
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

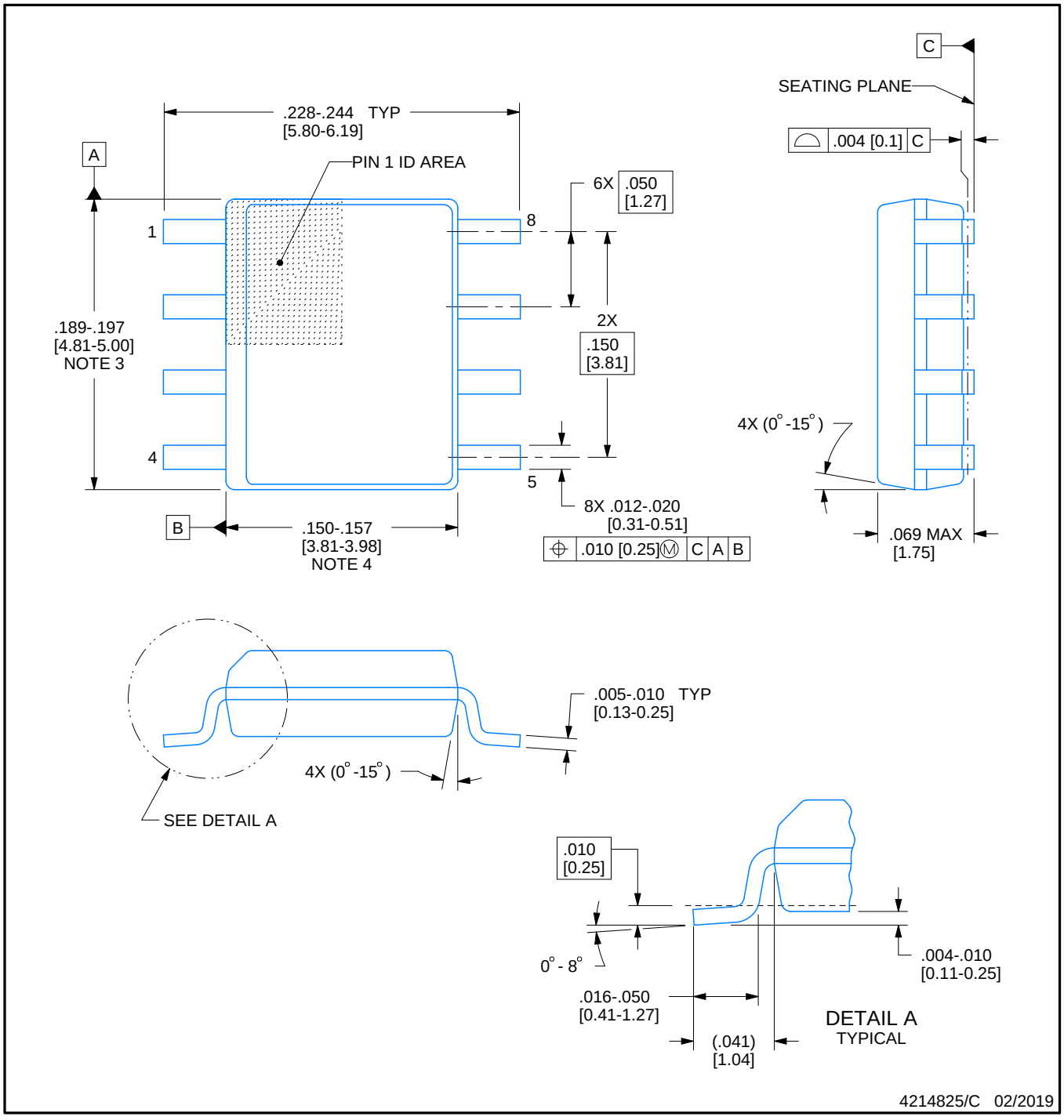
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

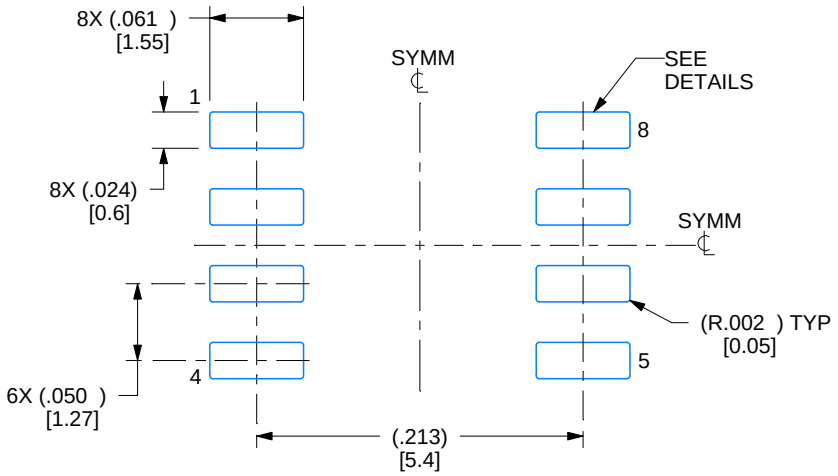
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

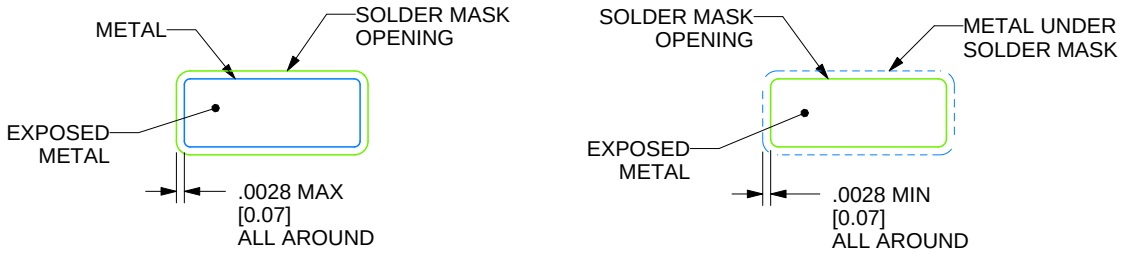
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

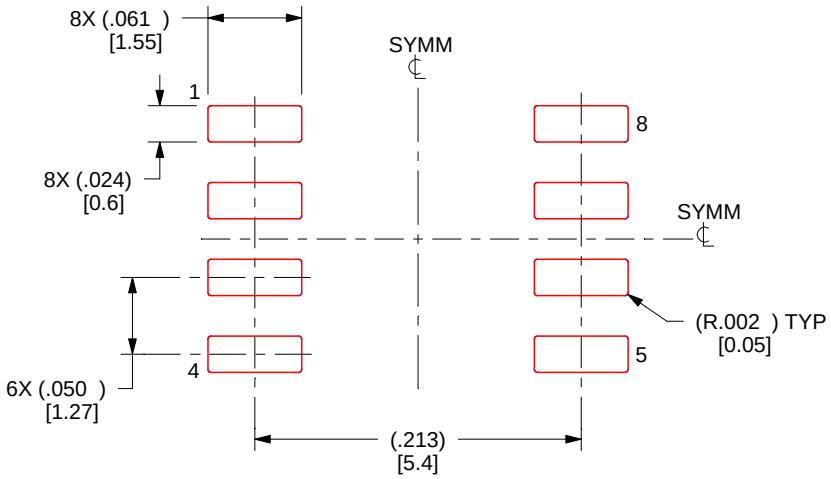
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



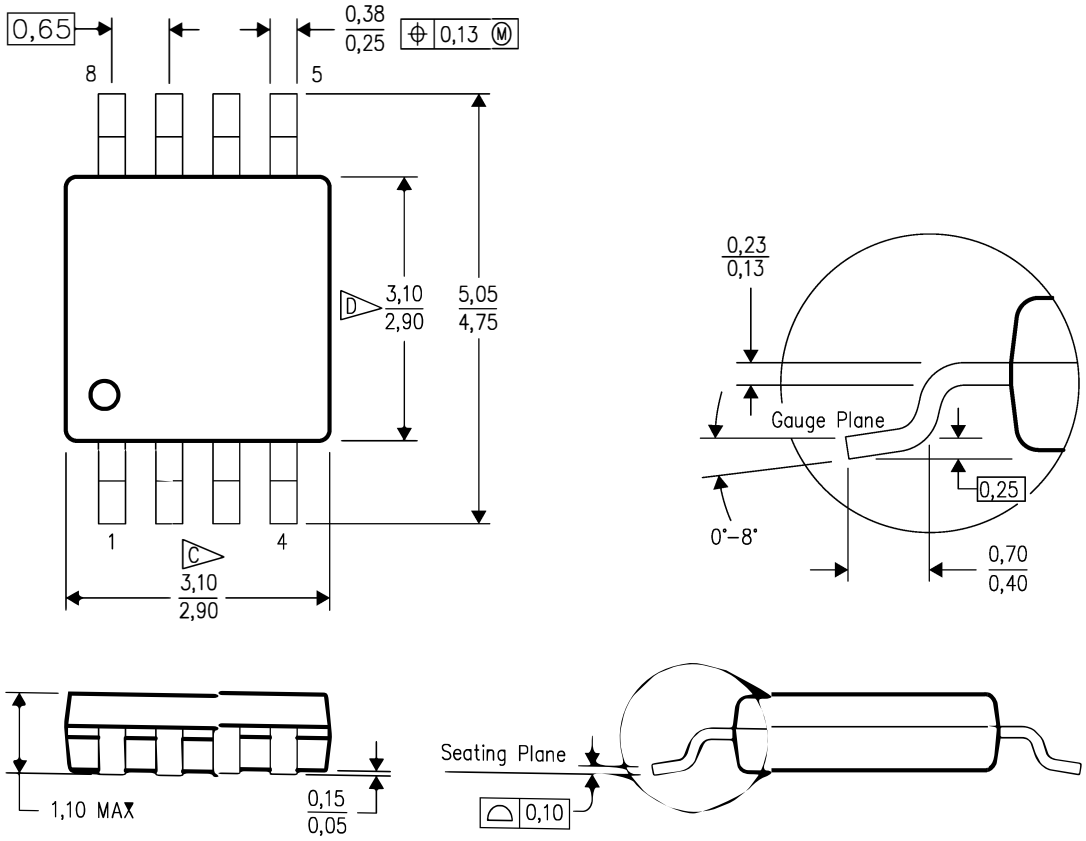
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

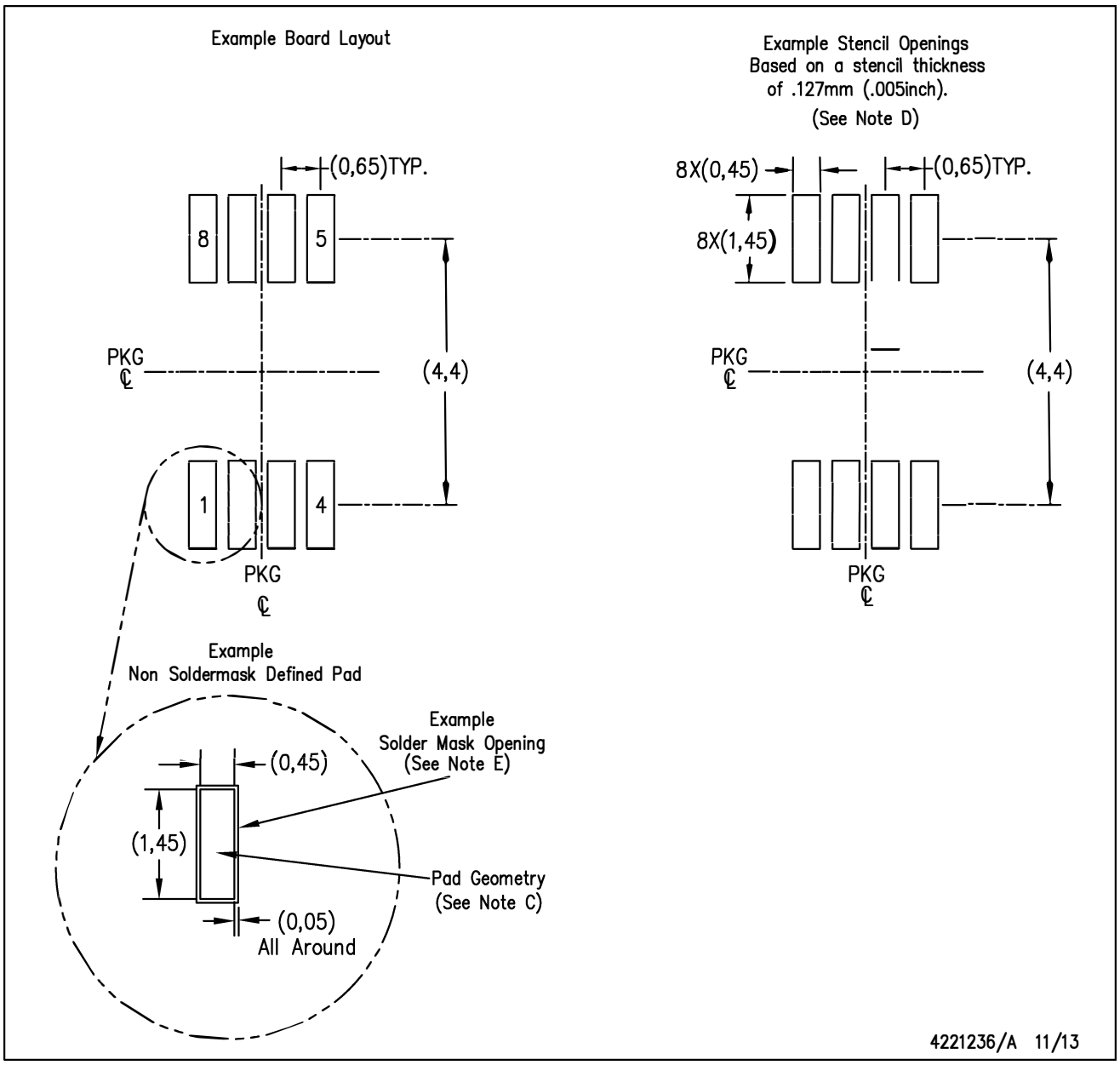
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.