LPV801/LPV802 320 nA Nanopower Operational Amplifiers

1 Features

- Nanopower Supply Current: 320 nA/channel (typ)
- Offset Voltage: 3.5 mV (max)
- Good TcVos: 1.5 µV/°C (typ)
- Unity Gain-Bandwidth: 8 kHz
- Unity-Gain Stable
- Low Input Bias Current : 0.1pA (typ)
- Wide Supply Range: 1.6 V to 5.5 V
- Rail-to-Rail Output
- No Output Reversals
- EMI Protection
- Temperature Range: –40°C to 125°C
- Industry Standard Packages:
  - Single in 5-pin SOT-23
  - Dual in 8-pin VSSOP

2 Applications

- Gas Detectors such as CO and O_2
- Motion Detectors Using PIR Sensors
- Ionization Smoke Alarms
- Thermostats
- Remote Sensors, IoT
- Active RFID Readers and Tags
- Portable Medical Equipment

3 Description

The LPV801 (single) and LPV802 (dual) comprise a family of ultra-low-power operational amplifiers for “Always ON” sensing applications in wireless and low power wired equipment. With 8kHz of bandwidth from 320nA of quiescent current, the LPV80x amplifiers minimize power consumption in equipment such as CO detectors, smoke detectors and motion detecting security systems where operational battery-life is critical.

In addition to being ultra-low-power, the LPV80x amplifiers have CMOS input stages with typically femto-amp bias currents which reduces errors commonly introduced in transimpedance amplifier (TIA) configurations with megaohm feedback resistors and high source impedance sensing applications. The LPV80x amplifiers also feature a negative-rail sensing input stage and a rail-to-rail output stage that is capable of swinging within millivolts of the rails, maintaining the widest dynamic range possible. EMI protection is designed into the LPV80x in order to reduce system sensitivity to unwanted RF signals from mobile phones, WiFi, radio transmitters and tag readers.

The LPV80x amplifiers operate with a total supply voltage as low as 1.6V, ensuring continuous performance in low battery situations over the extended temperature range of –40ºC to 125ºC. The single and dual channel versions are available in industry standard 5-pin SOT-23 and 8-pin VSSOP packages respectively.

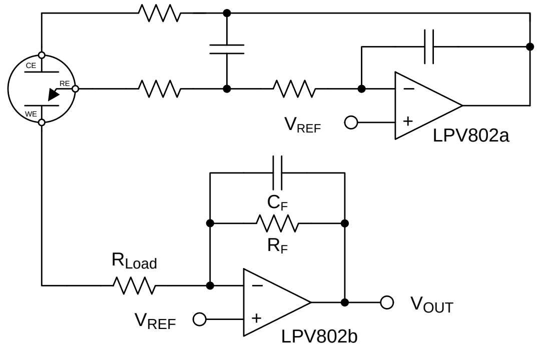
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
LPV801	SOT-23 (5)	2.90 mm x 1.60 mm
LPV802	VSSOP (8)	3.00 mm × 3.00 mm

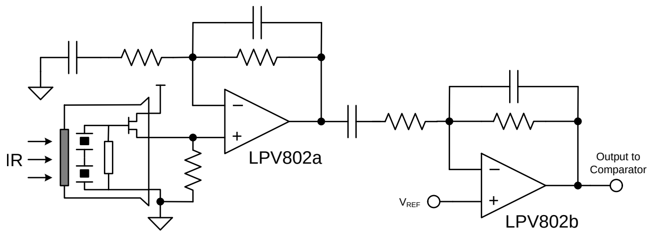
(1) For all available packages, see the orderable addendum at the end of the datasheet.

PRODUCT PREVIEW

Nanopower Electrochemical Sensor Amplifier



Nanopower PIR Motion Sensor Amplifier



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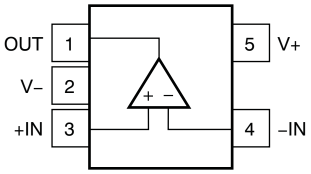
4 Revision History

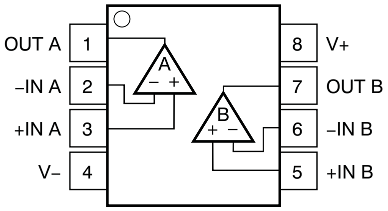
DATE	REVISION	NOTES
June 2016	*	Initial release Product Preview

5 Pin Configuration and Functions

LPV801 5-Pin SOT-23
DBV Package
Top View



LPV802 8-Pin VSSOP
DGK Package
Top View



Pin Functions: LPV801 DBV

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT	1	O	Output
-IN	2	I	Inverting Input
+IN	3	I	Non-Inverting Input
V-	4	P	Negative (lowest) power supply
V+	5	P	Positive (highest) power supply

Pin Functions: LPV802 DGK

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT A	1	O	Channel A Output
-IN A	2	I	Channel A Inverting Input
+IN A	3	I	Channel A Non-Inverting Input
V-	4	P	Negative (lowest) power supply
+IN B	5	I	Channel B Non-Inverting Input
-IN B	6	I	Channel B Inverting Input
OUT B	7	O	Channel B Output
V+	8	P	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) - (V-)			–0.3	6	V
Input pins	Voltage (2) (3)	Common mode	(V-) - 0.3	(V+) + 0.3	V
		Differential	(V-) - 0.3	(V+) + 0.3	V
Input pins	Current		-10	10	mA
Output short current (4)			Continuous	Continuous	
Operating temperature			–40	125	°C
Storage temperature, T_{stg}			–65	150	°C
Junction temperature				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Not to exceed -0.3V or +6.0V on ANY pin, referred to V-
(3) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
(4) Short-circuit to Vs/2, one amplifer per package. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	1.6		5.5	V
Specified temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LPV801 DBV 5 PINS	LPV802 DGK 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	177.4	184.2	ºC/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	133.9	75.3	
θ_{JB}	Junction-to-board thermal resistance	36.3	105.5	
ψ_{JT}	Junction-to-top characterization parameter	23.6	13.5	
ψ_{JB}	Junction-to-board characterization parameter	35.7	103.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

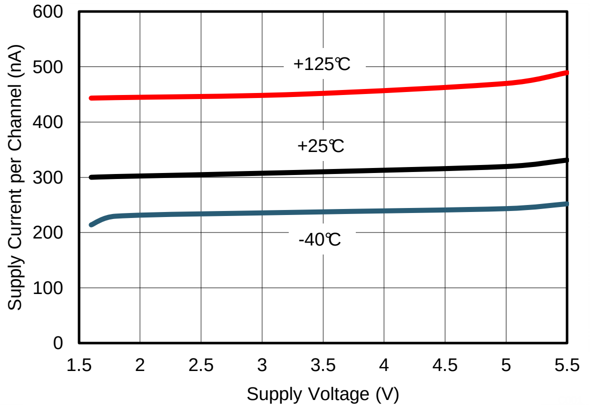
T_A = 25°C, V_S = 1.8V to 5 V, V_{CM} = V_{OUT} = V_S/2, and $R_L \geq$ 10 MΩ to V_S / 2, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 1.8V, 3.3V, and 5V, V_{CM} = V-			0.55	±3.5	mV
		V_S = 1.8V, 3.3V, and 5V, V_{CM} = (V+) – 0.9 V			0.55	±3.5	
$\Delta V_{OS}/\Delta T$	Input offset drift	V_{CM} = V-	T_A = –40°C to 125°C		1.5		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8V to 5V, V_{CM} = V-			1.6	60	µV/V
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	V_S = 5 V		0		4.1	V
CMRR	Common-mode rejection ratio	(V–) ≤ V_{CM} ≤ (V+) – 0.9 V, V_S= 5V		80	98		dB
INPUT BIAS CURRENT							
I_B	Input bias current	V_S = 1.8V			100		fA
I_{OS}	Input offset current	V_S = 1.8V			100		
INPUT IMPEDANCE							
	Differential				8		pF
	Common mode				3.8		
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			25		µVp-p
e_n	Input voltage noise density	f = 100 Hz			340		nV/√Hz
		f = 1 kHz			420		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V ≤ V_O ≤ (V+) – 0.3 V, R_L = 100 kΩ			135		dB
OUTPUT							
V_{OH}	Voltage output swing from positive rail	V_S = 1.8V, R_L = 100 kΩ to V^+/2		10	6		mV
V_{OL}	Voltage output swing from negative rail	V_S = 1.8V, R_L = 100 kΩ to V^+/2			4	10	
I_{SC}	Short-circuit current	Short to V_S/2			4.7		mA
Z_O	Open loop output impedance	f = 1 KHz, I_O = 0 A			94.5		kΩ
FREQUENCY RESPONSE							
GBP	Gain-bandwidth product	C_L = 20 pF, R_L = 10 MΩ, V_S = 5V			8		kHz
SR	Slew rate (10% to 90%)	G = 1, Rising Edge, C_L = 20 pF, V_S = 5V			1.8		V/ms
		G = 1, Falling Edge, C_L = 20 pF, V_S = 5V			1.7		
POWER SUPPLY							
$I_{Q\text{-}LPV801}$	Quiescent Current, Per Channel	V_{CM} = V-, I_O = 0, V_S = 3.3 V			450	550	nA
$I_{Q\text{-}LPV802}$	Quiescent Current, Per Channel	V_{CM} = V-, I_O = 0, V_S = 3.3 V			320	415	nA

(1) LPV801 Specifications are Preliminary until released.

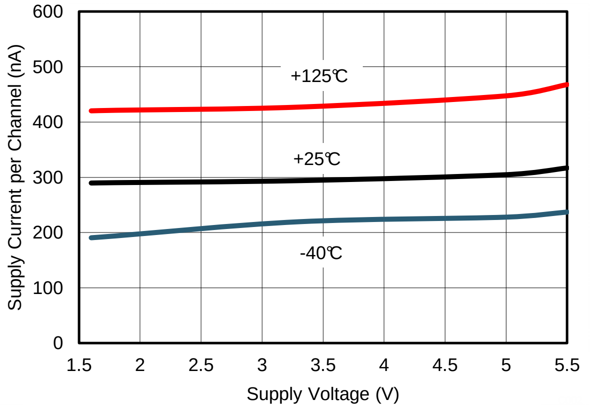
6.6 Typical Characteristics

at T_A = 25°C, V_S = 5V, R_L = 10MΩ to $V_S/2$,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



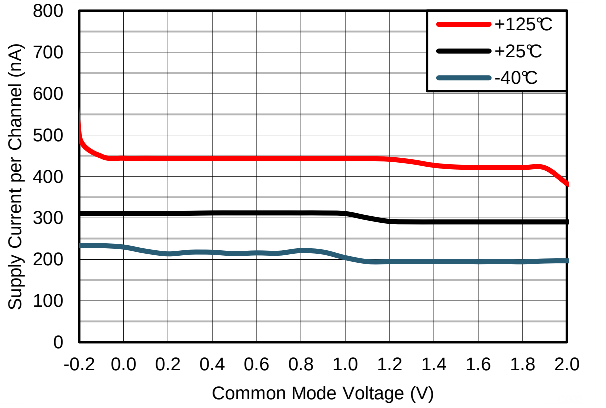
V_{CM} = V- R_L=No Load

Figure 1. Supply Current vs. Supply Voltage, Low VCM



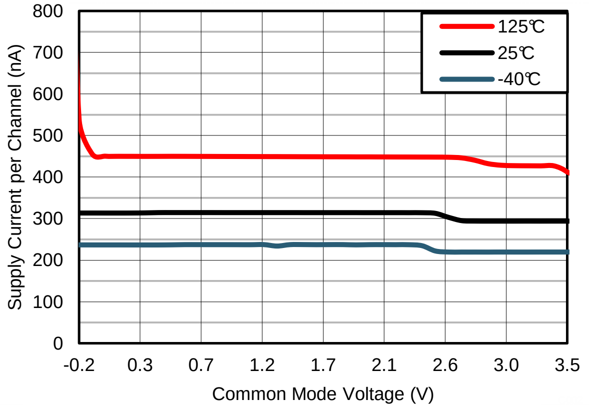
V_{CM} = V+ R_L=No Load

Figure 2. Supply Current vs. Supply Voltage, High VCM



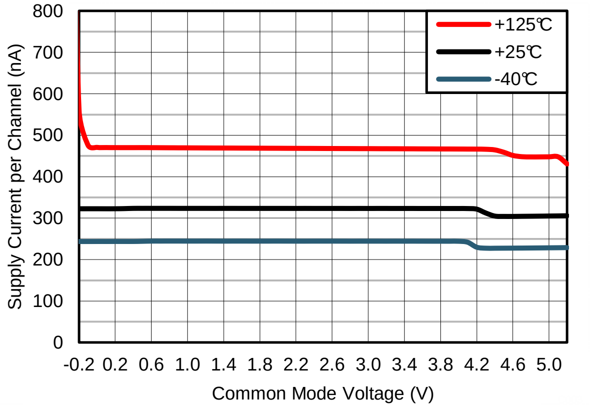
V_S= 1.8V V_{CM} = V+ R_L= No Load

Figure 3. Supply Current vs. Common Mode Voltage, 1.8V



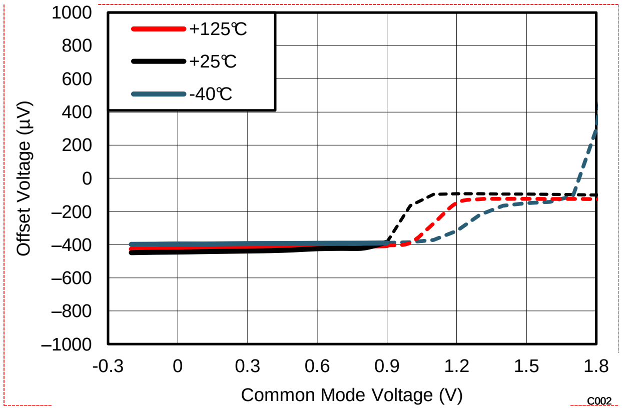
V_S= 3.3V R_L= No Load

Figure 4. Supply Current vs. Common Mode Voltage, 3.3V



V_S= 5V R_L= No Load

Figure 5. Supply Current vs. Common Mode Voltage, 5V

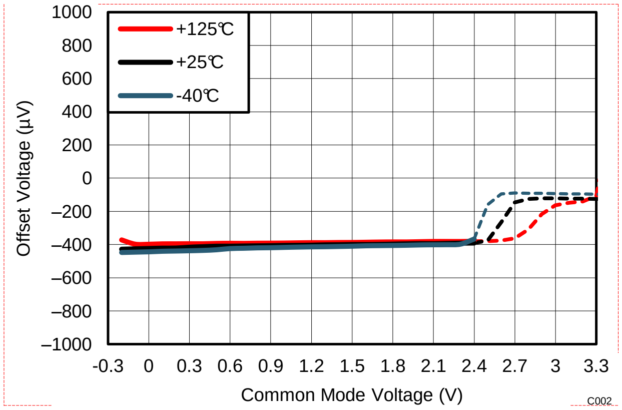


V_S= 1.8V R_L= 10MΩ

Figure 6. Typical Offset Voltage vs. Common Mode Voltage, 1.8V

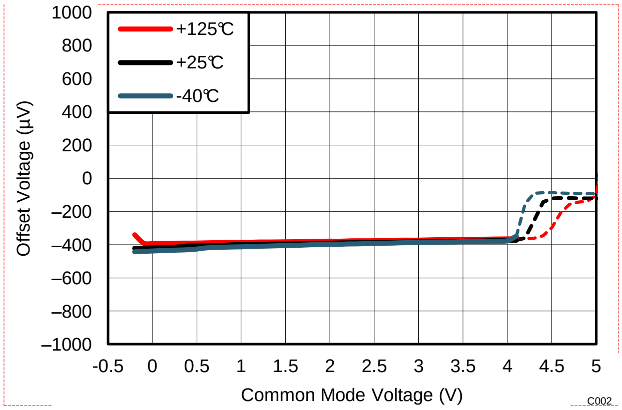
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



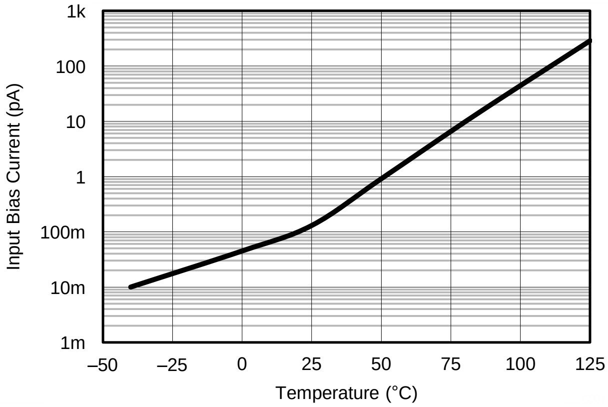
V_S= 3.3V R_L= 10MΩ

Figure 7. Typical Offset Voltage vs. Common Mode Voltage, 3.3V



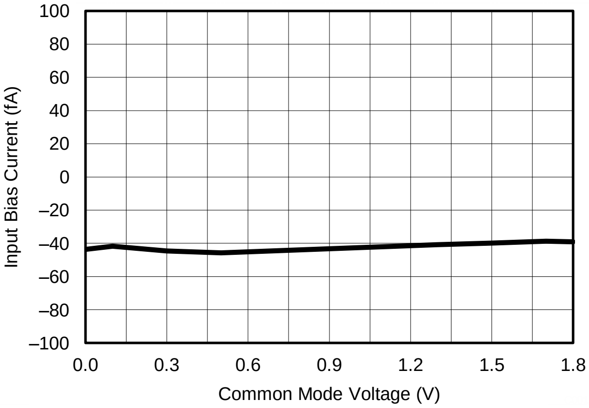
V_S= 5V R_L= 10MΩ

Figure 8. Typical Offset Voltage vs. Common Mode Voltage, 5V



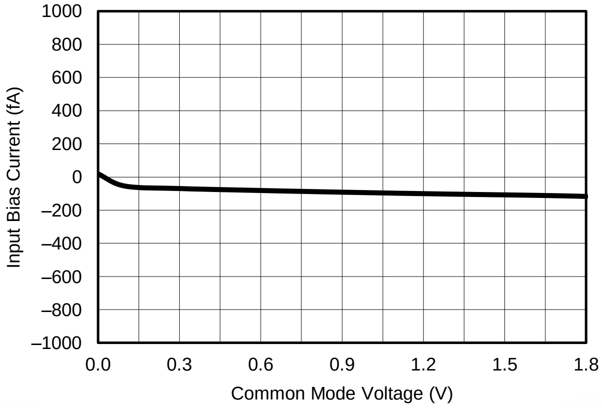
V_S= 5V T_A = -40 to 125 V_{CM} = Vs/2

Figure 9. Input Bias Current vs. Temperature



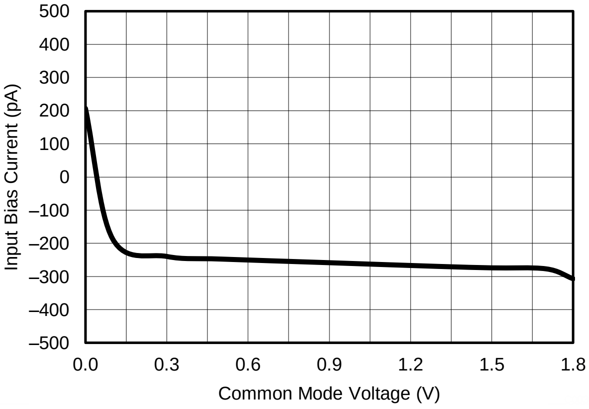
V_S= 1.8V T_A = -40°C

Figure 10. Input Bias Current vs. Common Mode Voltage at -40°C



V_S= 1.8V T_A = 25°C

Figure 11. Input Bias Current vs. Common Mode Voltage at 25°C

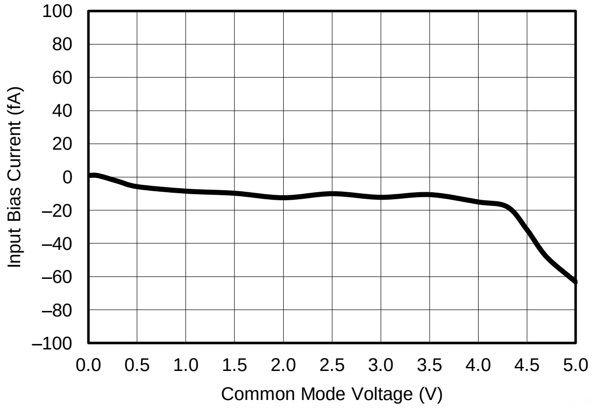


V_S= 1.8V T_A = 125°C

Figure 12. Input Bias Current vs. Common Mode Voltage at 125°C

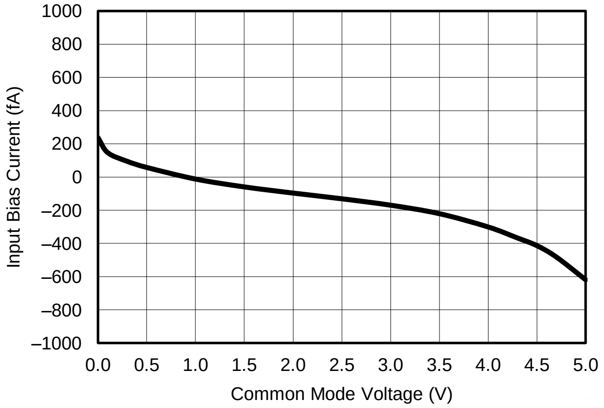
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



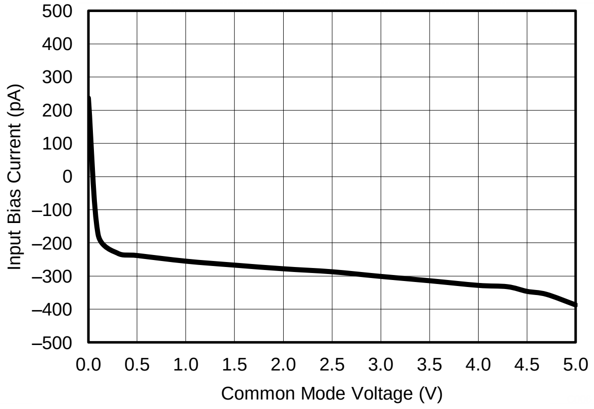
V_S= 5V T_A = -40°C

Figure 13. Input Bias Current vs. Common Mode Voltage at -40°C



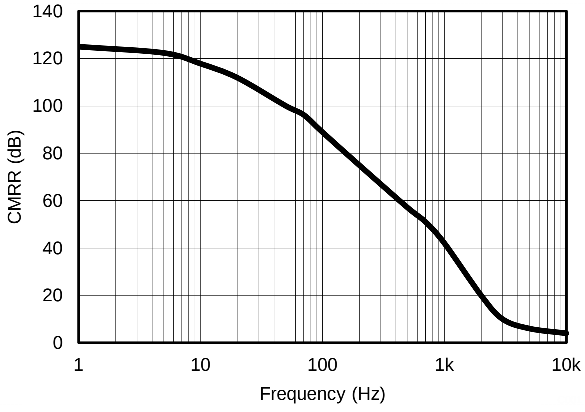
V_S= 5V T_A = 25°C

Figure 14. Input Bias Current vs. Common Mode Voltage at 25°C



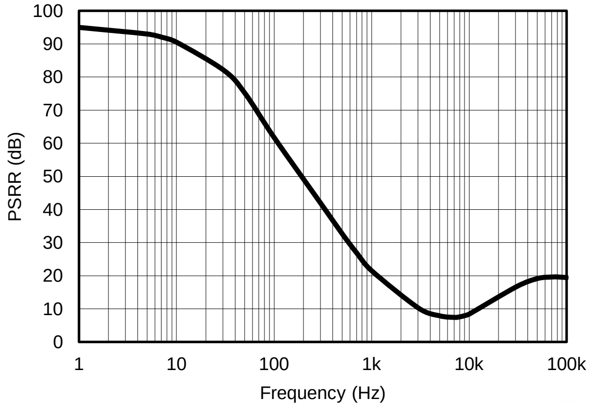
V_S= 5V T_A = 125°C

Figure 15. Input Bias Current vs. Common Mode Voltage at 125°C



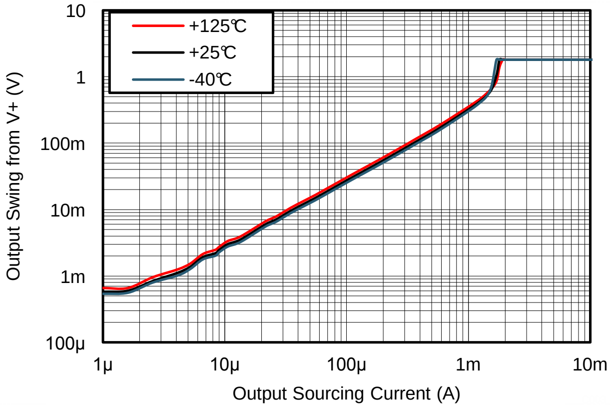
T_A = 25 R_L= 10MΩ ΔV_{CM} = 0.5Vpp
V_S= 5V C_L= 20p
V_{CM} = Vs/2 A_V = +1

Figure 16. CMRR vs Frequency



T_A = 25 R_L= 10MΩ ΔV_{CM} = 0.5Vpp
V_S= 5V C_L= 20p
V_{CM} = Vs/2 A_V = +1

Figure 17. ±PSRR vs Frequency

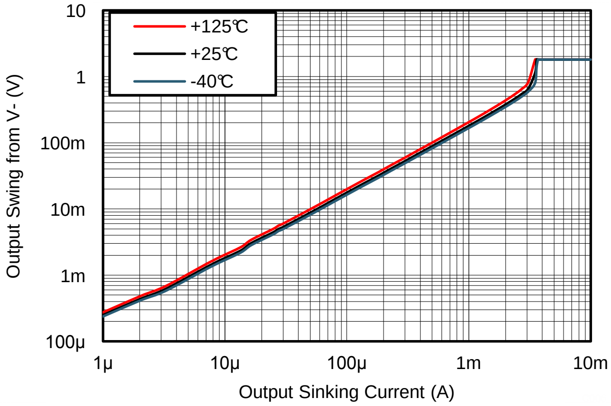


T_A = 25 R_L= 10MΩ ΔV_S = 0.2Vpp
V_S= 5V C_L= 20p
V_{CM} = Vs/2 A_V = +1

Figure 18. Output Swing vs. Sourcing Current, 1.8V

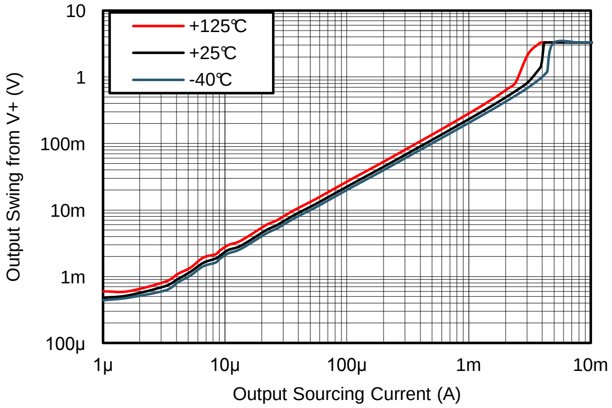
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



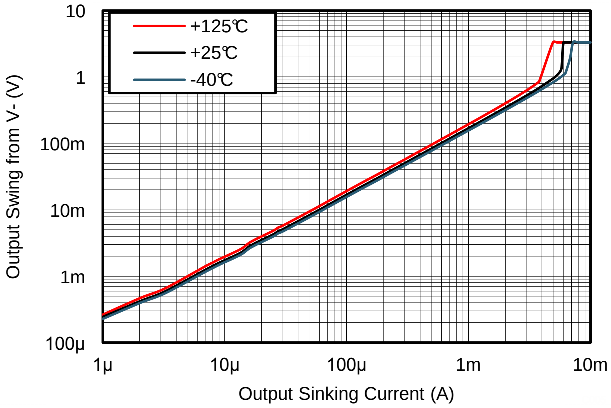
V_S= 1.8V
R_L= No Load

Figure 19. Output Swing vs. Sinking Current, 1.8V



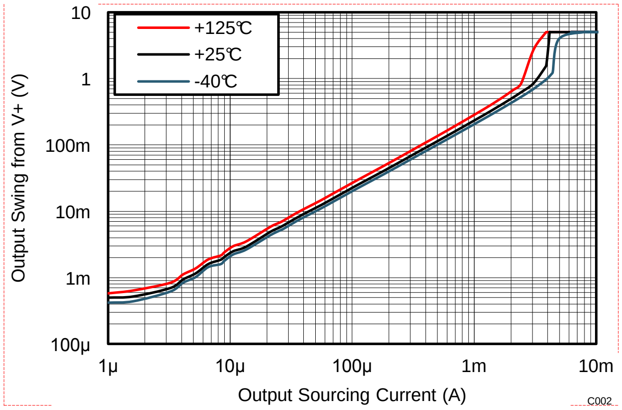
V_S= 3.3V
R_L= No Load

Figure 20. Output Swing vs. Sourcing Current, 3.3V



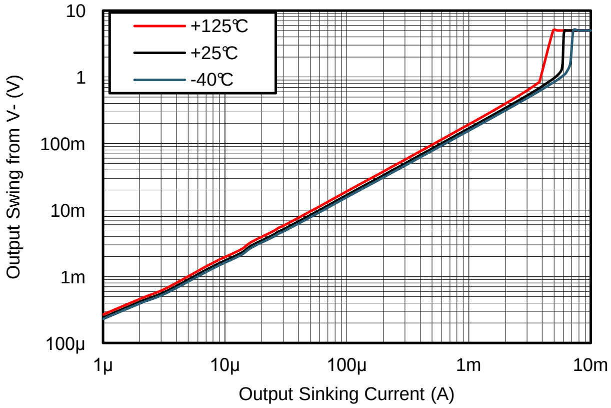
V_S= 3.3V
R_L= No Load

Figure 21. Output Swing vs. Sinking Current, 3.3V



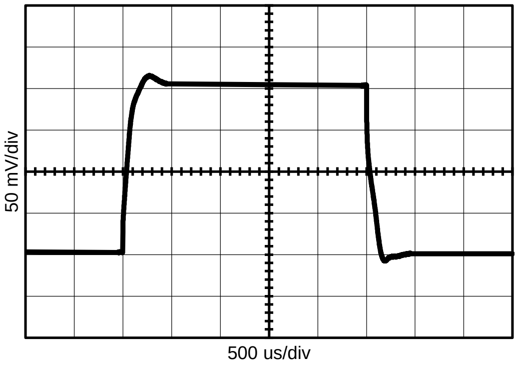
V_S= 5V
R_L= No Load

Figure 22. Output Swing vs. Sourcing Current, 5V



V_S= 5V
R_L= No Load

Figure 23. Output Swing vs. Sinking Current, 5V

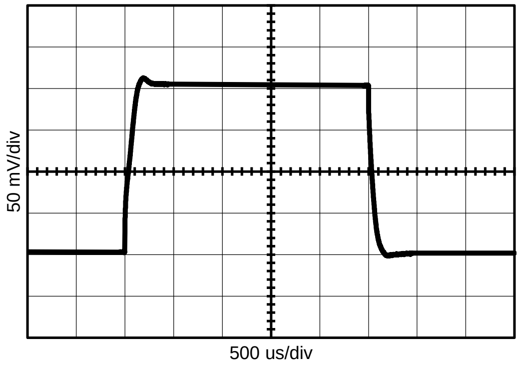


T_A = 25
R_L= 10MΩ
Vout = 200mVpp
V_S= ±0.9V
C_L= 20pF
A_V = +1

Figure 24. Small Signal Pulse Response, 1.8V

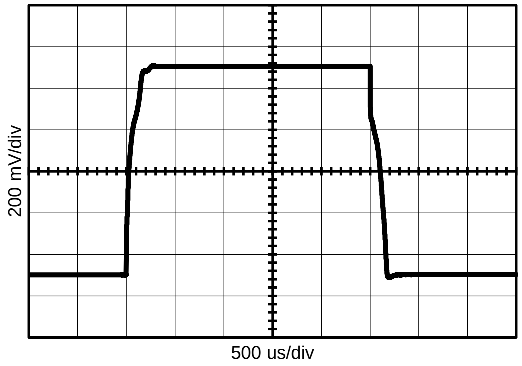
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



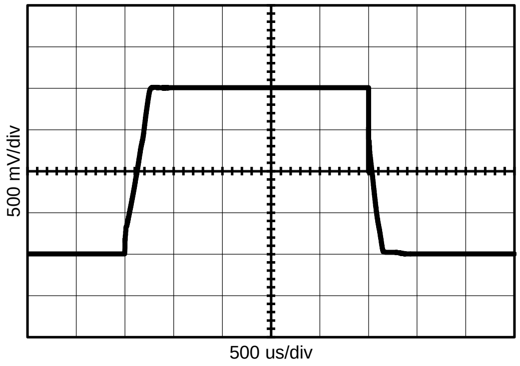
T_A = 25 R_L= 10MΩ Vout = 200mVpp
V_S= ±2.5V C_L= 20pF A_V = +1

Figure 25. Small Signal Pulse Response, 5V



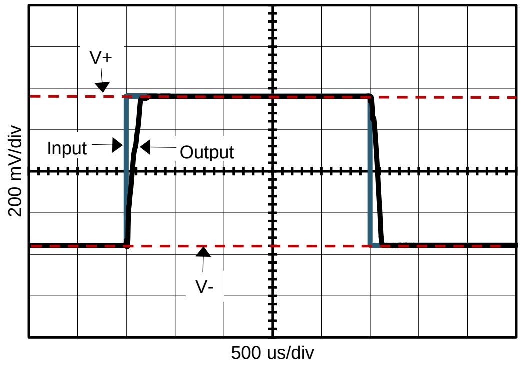
T_A = 25 R_L= 10MΩ Vout = 1Vpp
V_S= ±0.9V C_L= 20pF A_V = +1

Figure 26. Large Signal Pulse Response, 1.8V



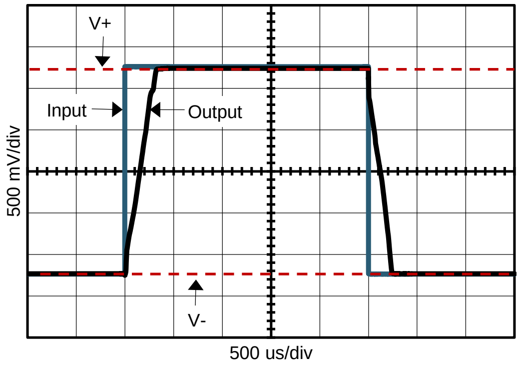
T_A = 25 R_L= 10MΩ Vout = 2Vpp
V_S= ±2.5V C_L= 20pF A_V = +1

Figure 27. Large Signal Pulse Response, 5V



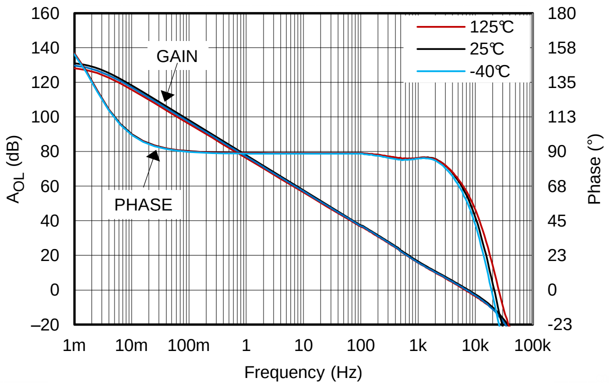
T_A = 25 R_L= 10MΩ Vout = ±0.9Vpp
V_S= ±0.9V C_L= 20pF A_V = +1

Figure 28. Rail to Rail Input Response, 1.8V



T_A = 25 R_L= 10MΩ Vout = ±2.5Vpp
V_S= ±2.5V C_L= 20pF A_V = +1

Figure 29. Rail to Rail Input Response, 5V

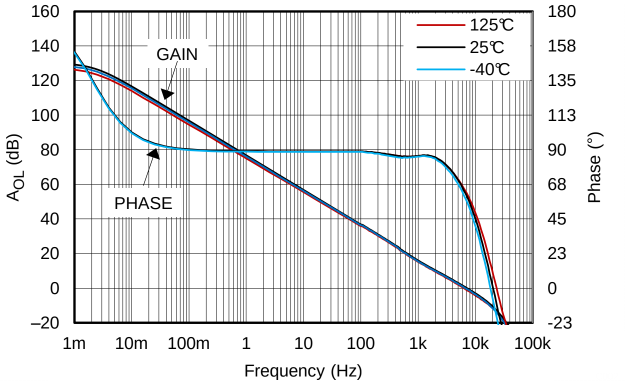


T_A = -40, 25, 125°C R_L= 10MΩ V_{OUT} = 200mV_{PP}
V_S= 5V C_L= 20pF V_{CM} = Vs/2

Figure 30. Open Loop Gain and Phase, 5V, 10 MΩ Load

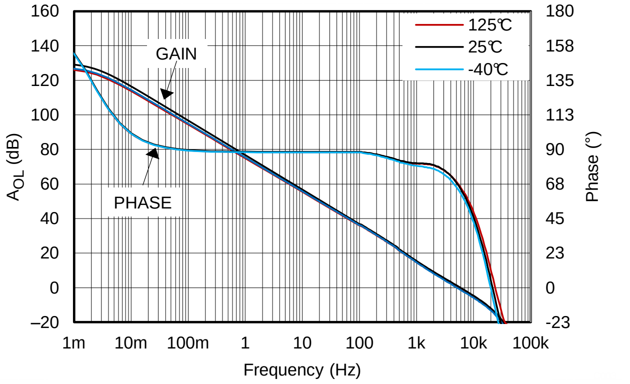
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



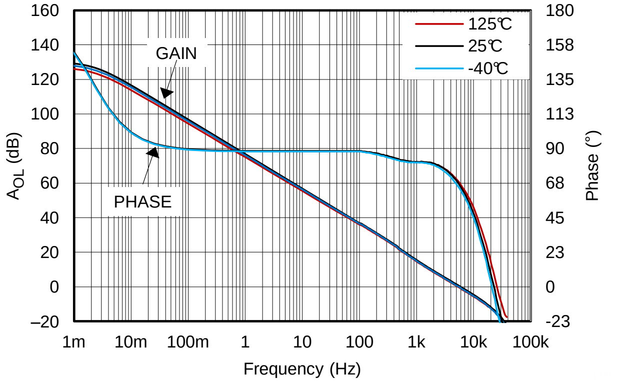
T_A = -40, 25, 125°C R_L= 10MΩ V_{OUT} = 200mV_{PP}
V_S= 3.3V C_L= 20pF V_{CM} = Vs/2

Figure 31. Open Loop Gain and Phase, 3.3V, 10 MΩ Load



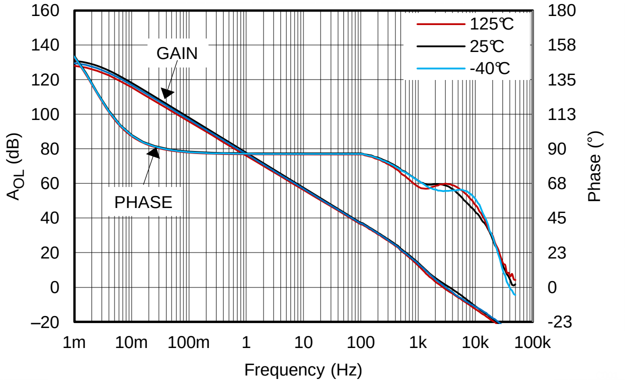
T_A = -40, 25, 125°C R_L= 1MΩ V_{OUT} = 200mV_{PP}
V_S= 5V C_L= 20pF V_{CM} = Vs/2

Figure 32. Open Loop Gain and Phase, 5V, 1 MΩ Load



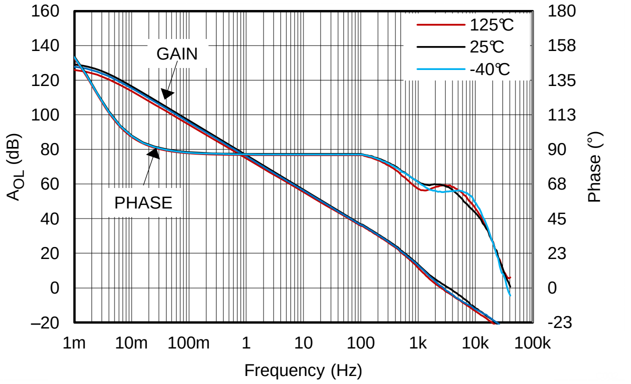
T_A = -40, 25, 125°C R_L= 1MΩ V_{OUT} = 200mV_{PP}
V_S= 3.3V C_L= 20pF V_{CM} = Vs/2

Figure 33. Open Loop Gain and Phase, 3.3V, 1 MΩ Load



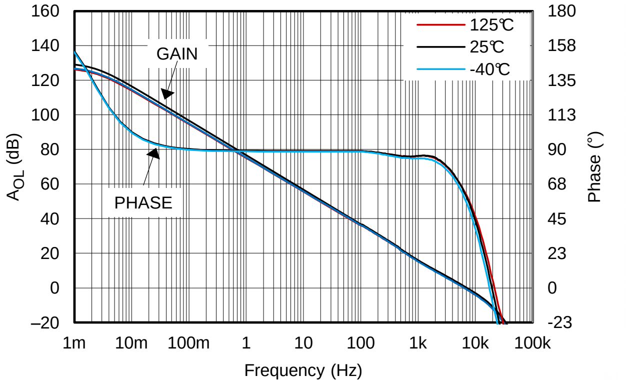
T_A = -40, 25, 125°C R_L= 100kΩ V_{OUT} = 200mV_{PP}
V_S= 5V C_L= 20pF V_{CM} = Vs/2

Figure 34. Open Loop Gain and Phase, 5V, 100kΩ Load



T_A = -40, 25, 125°C R_L= 100kΩ V_{OUT} = 200mV_{PP}
V_S= 3.3V C_L= 20pF V_{CM} = Vs/2

Figure 35. Open Loop Gain and Phase, 3.3V, 100kΩ Load

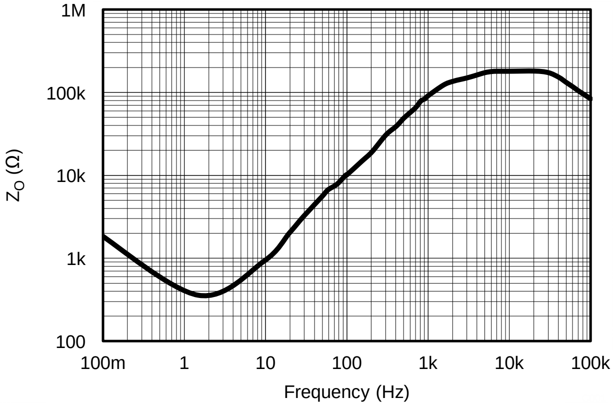


T_A = -40, 25, 125°C R_L= 10MΩ V_{OUT} = 200mV_{PP}
V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

Figure 36. Open Loop Gain and Phase, 1.8V, 10 MΩ Load

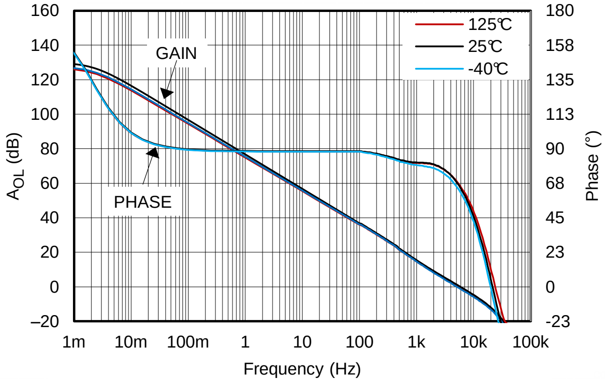
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



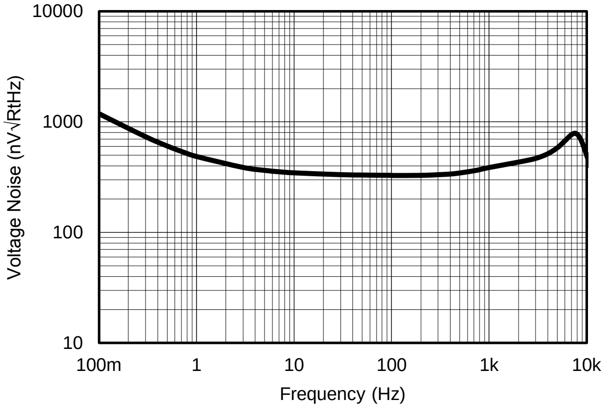
T_A = 25°C V_S= 5 V R_L= 10MΩ

Figure 37. Open Loop Output Impedance



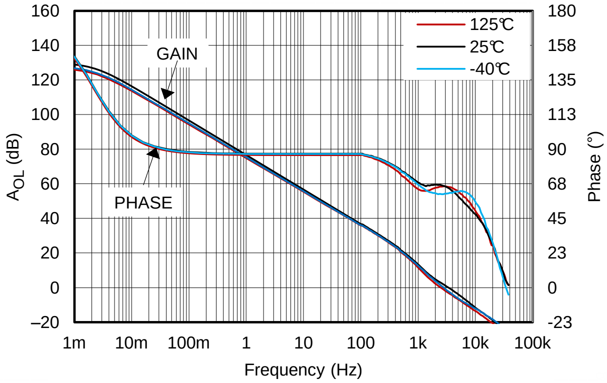
T_A = -40, 25, 125°C R_L= 1MΩ V_{OUT} = 200mV_{PP}
V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

Figure 38. Open Loop Gain and Phase, 1.8V, 1 MΩ Load



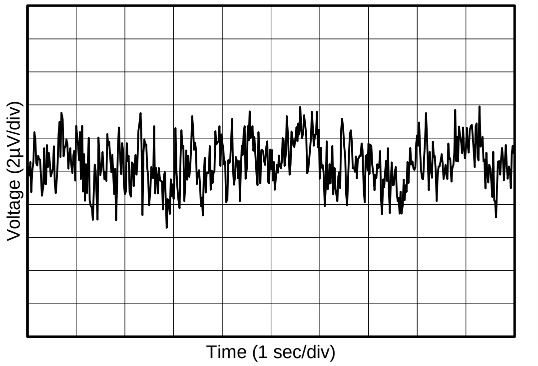
T_A = 25 R_L= 1MΩ V_{CM} = Vs/2
V_S= 5V C_L= 20pF A_V = +1

Figure 39. Voltage Noise vs Frequency



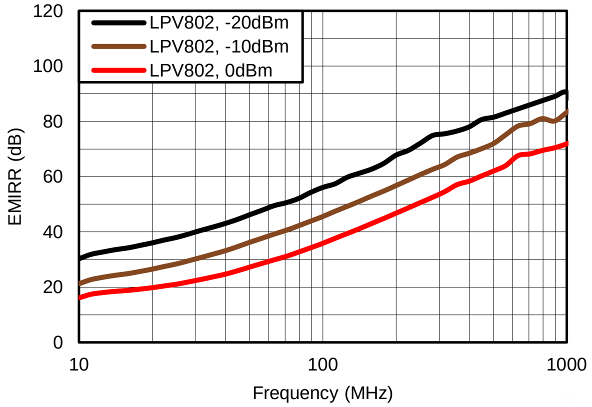
T_A = -40, 25, 125°C R_L= 100kΩ V_{OUT} = 200mV_{PP}
V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

Figure 40. Open Loop Gain and Phase, 1.8V, 100kΩ Load



T_A = 25 R_L= 1MΩ V_{CM} = Vs/2
V_S= 5V C_L= 20pF A_V = +1

Figure 41. 0.1 to 10Hz Peak to Peak Noise



T_A = 25 R_L= 1MΩ V_{CM} = Vs/2
V_S= 3.3V C_L= 20pF A_V = +1

Figure 42. EMIRR Performance

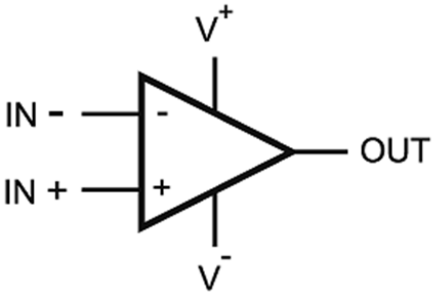
7 Detailed Description

7.1 Overview

The LPV80x is unity-gain stable and can operate on a single supply, making it highly versatile and easy to use.

Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* curves.

7.2 Functional Block Diagram



7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (–IN). The amplifer amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} \left(IN^{+} - IN^{-}\right) \tag{1}$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 100 dB (100,000x, or 100,000 Volts per microvolt).

7.4 Device Functional Modes

7.4.1 Negative-Rail Sensing Input

The input common-mode voltage range of the LPV80x extends from (V-) to (V+) – 0.9 V. In this range, low offset can be expected with a minimum of 80dB CMRR. Operation of the LPV80x beyond (V+) - 0.9V is possible, however, the offset voltage is not specified. Because of this, the LPV80x is protected from output "inversions" or "reversals" as long as the input common mode voltage range stays within the input pin Absolute Maximum Ratings range.

7.4.2 Rail to Rail Output Stage

The LPV80x output voltage swings 3 mV from rails at 3.3 V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV80x Maximum Output Voltage Swing graph defines the maximum swing possible under a particular output load.

7.4.3 Design Optimization for Nanopower Operation

When designing for ultralow power, choose system feedback components carefully. To minimize quiecent current consumption, select large-value feedback resistors. Any large resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors since large electolytics may have large static leakage currents in the nanoamps.

Device Functional Modes (continued)

7.4.4 Driving Capacitive Load

The LPV80x is internally compensated for stable unity gain operation, with a 8 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the amplifier’s output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy (>50pF) capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 43. By using this isolation resistor, the capacitive load is isolated from the amplifier’s output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive. The recommended value for R_{ISO} is 30-50kΩ.

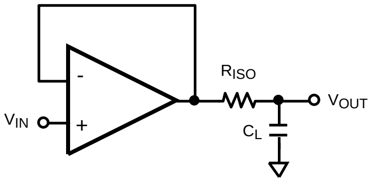


Figure 43. Resistive Isolation Of Capacitive Load

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LPV80x is a ultra-low power operational amplifier that provides 8 kHz bandwidth with only 320nA typical quiescent current, and near precision drift specifications at a low cost. These rail-to-rail input and output amplifiers are specifically designed for battery-powered applications. The input common-mode voltage range extends to the negative supply rail and the output swings to within millivolts of the rails, maintaining a wide dynamic range.

8.2 Typical Application: Three Terminal CO Gas Sensor Amplifier

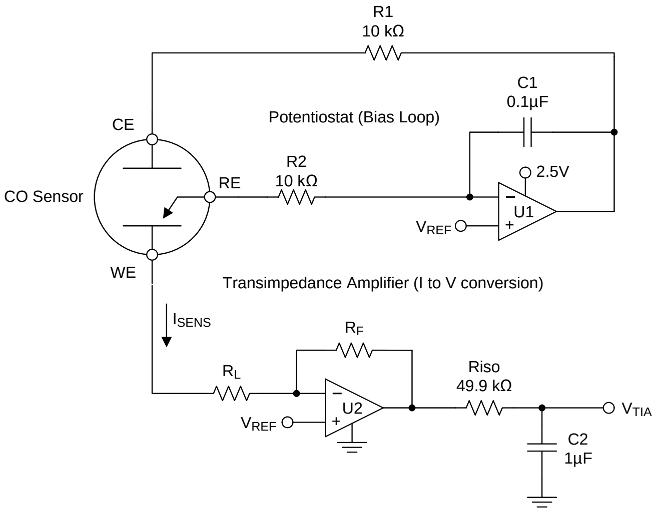


Figure 44. Three Terminal Gas Sensor Amplifer Schematic

8.2.1 Design Requirements

Figure 44 shows a simple micropower potentiostat circuit for use with three terminal unbiased CO sensors, though it is applicable to many other type three terminal gas sensors or electrochemical cells.

The basic sensor has three electrodes; The Sense or Working Electrode ("WE"), Counter Electrode ("CE") and Reference Electrode ("RE"). A current flows between the CE and WE proportional to the detected concentration.

The RE monitors the potential of the internal reference point. For an unbiased sensor, the WE and RE electrodes must be maintained at the same potential by adjusting the bias on CE. Through the Potentiostat circuit formed by U1, the servo feedback action will maintain the RE pin at a potential set by V_{REF}.

R1 is to maintain stability due to the large capacitence of the sensor. C1 and R2 form the Potentiostat integrator and set the feedback time constant.

U2 forms a transimpedance amplifer ("TIA") to convert the resulting sensor current into a proportional voltage. The transimpedance gain, and resulting snesitivity, is set by R_F according to Equation 2 .

$$V_{TIA} = (-I * R_F) + V_{REF} \tag{2}$$

R_L is a load resistor of which the value is normally specified by the sensor manufacturer (typically 10 ohms). The potential at WE is set by the applied $V_{REF.}$ Riso provides capacitive isolation and, combined with C2, form the output filter and ADC reservoir capacitor to drive the ADC.

Typical Application: Three Terminal CO Gas Sensor Amplifier (continued)

8.2.2 Detailed Design Procedure

For this example, we will be using a CO sensor with a sensitivity of 69nA/ppm. The supply votlage and maximum ADC input voltage is 2.5V, and the maximum concentration is 300ppm.

First the V_{REF} voltage must be determined. This voltage is a compromise between maximum headroom and resolution, as well as allowance for "footroom" for the minimum swing on the CE terminal, since the CE terminal generally goes negative in relation to the RE potential as the concentration (sensor current) increases. Bench measuements found the difference between CE and RE to be 180mV at 300ppm for this particular sensor.

To allow for negative CE swing "footroom" and voltage drop across the 10k resistor, 300mV was chosen for V_{REF}.

Therefore +300mV will be used as the minimum V_{ZERO} to add some headroom.

$V_{ZERO} = V_{REF} = +300mV$

where

- V_{ZERO} is the zero concentration voltage
- V_{REF} is the reference voltage (300mV) (3)

Next we calculate the maximum sensor current at highest expected concentration:

$I_{SENSMAX} = I_{PERPPM} * ppmMAX = 69nA * 300ppm = 20.7uA$

where

- $I_{SENSMAX}$ is the maximum expected sensor current
- I_{PERPPM} is the manufacturer specified sensor current in Amps per ppm
- ppmMAX is the maximum required ppm reading (4)

Now find the available output swing range above the reference voltage available for the measurement:

$V_{SWING} = V_{OUTMAX} – V_{ZERO} = 2.5V – 0.3V = 2.2V$

where

- V_{SWING} is the expected change in output voltage
- V_{OUTMAX} is the maximum amplifer output swing (usually near V+) (5)

Now we calculate the transimpedance resistor (R_F) value using the maximum swing and the maximum sensor current:

$R_F = V_{SWING} / I_{SENSMAX} = 2.2V / 20.7\mu A = 106.28\ k\Omega$ (we will use 110 kΩ for a common value) (6)

Typical Application: Three Terminal CO Gas Sensor Amplifier (continued)

8.2.3 Application Curve

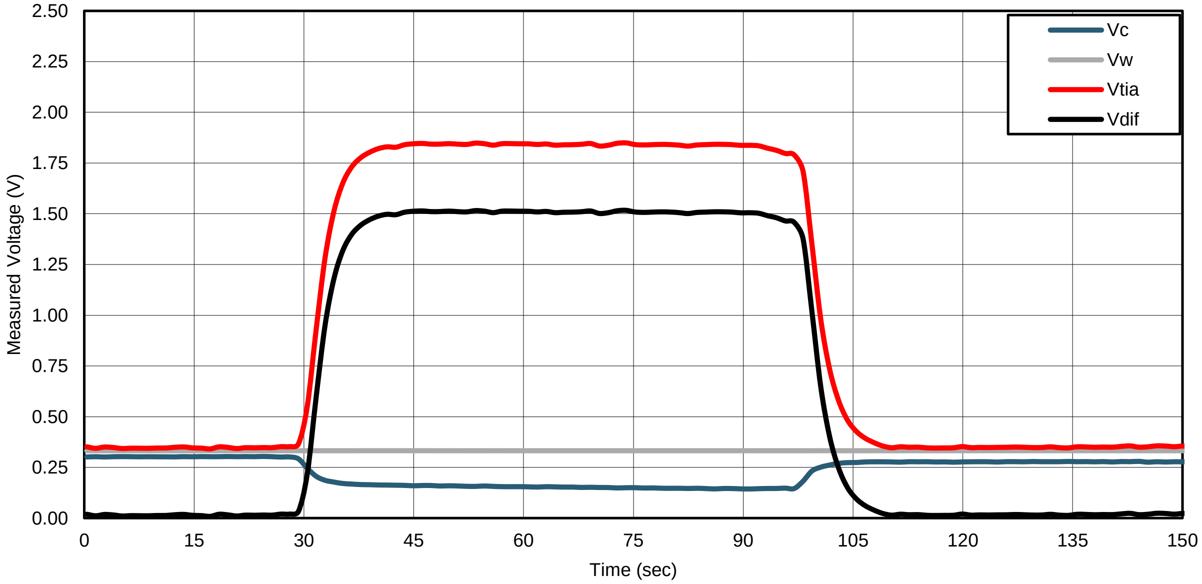


Figure 45. Monitored Voltages when exposed to 200ppm CO

Figure 45 shows the resulting circuit voltages when the sensor was exposed to 200ppm step of carbon monoxide gas. V_C is the monitored CE pin voltage and clearly shows the expected CE voltage dropping below the WE voltage, V_W, as the concentration increases.

V_{TIA} is the output of the transimpedance amplifer U2. V_{DIFF} is the calculated difference between V_{REF} and V_{TIA}, which will be used for the ppm calculation.

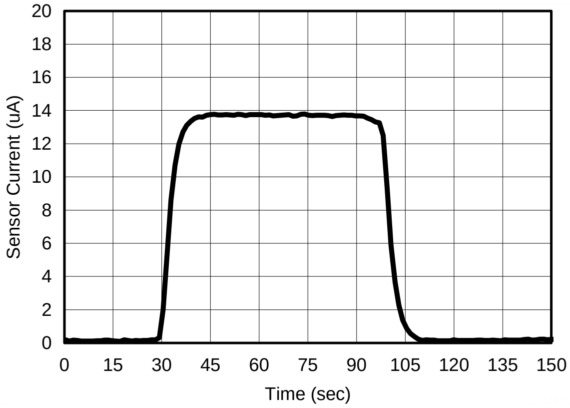


Figure 46. Calculated Sensor Current

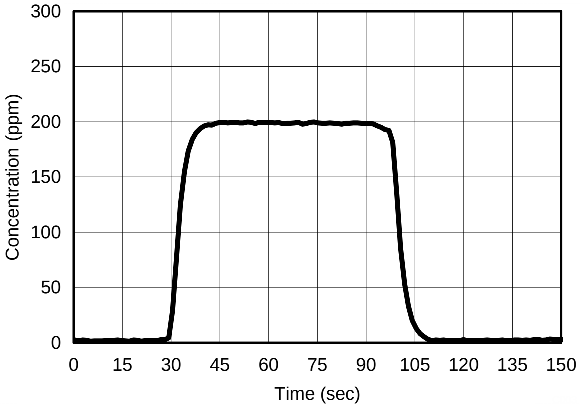


Figure 47. Calculated ppm

Figure 46 shows the calculated sensor current using the formula in Equation 7 :

$$I_{SENSOR} = V_{DIFF} / R_F = 1.52V / 110\ k\Omega = 13.8uA \quad (7)$$

Equation 8 shows the resulting conversion of the sensor current into ppm.

$$ppm = I_{SENSOR} / I_{PERPPM} = 13.8\mu A / 69nA = 200 \quad (8)$$

Total supply current for the amplifier section is less than 700 nA, minus sensor current. Note that the sensor current is sourced from the amplifier output, which in turn comes from the amplifier supply voltage. Therefore, any continuous sensor current must also be included in supply current budget calculations.

8.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1mA or less (1KΩ per volt).

9 Power Supply Recommendations

The LPV80x is specified for operation from 1.6 V to 5.5 V (±0.8 V to ±2.75 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 6 V can permanently damage the device.

For proper operation, the power supplies bust be properly decoupled. For decoupling the supply lines it is suggested that 100 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

The V+ pin should be bypassed to ground with a low ESR capacitor.

The optimum placement is closest to the V+ and ground pins.

Care should be taken to minimize the loop area formed by the bypass capacitor connection between V+ and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible to minimize strays.

10.2 Layout Example

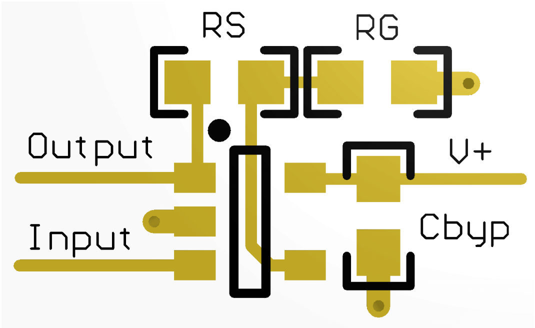


Figure 48. SOT-23 Layout Example (Top View)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

TI FilterPro Filter Design software, http://www.ti.com/tool/filterpro

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LPV801	Click here	Click here	Click here	Click here	Click here
LPV802	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

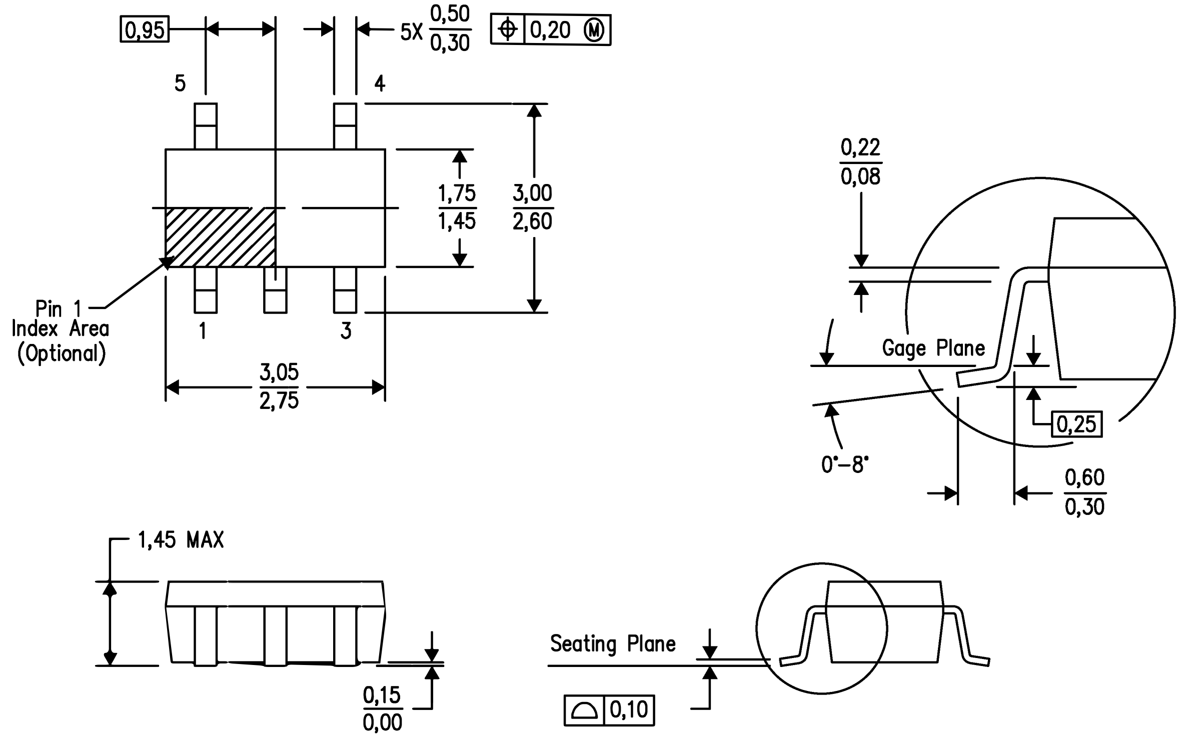
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV801DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
LPV801DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 125		
LPV802DGKR	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		
LPV802DGKT	PREVIEW	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		
PLPV801DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 125		

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE

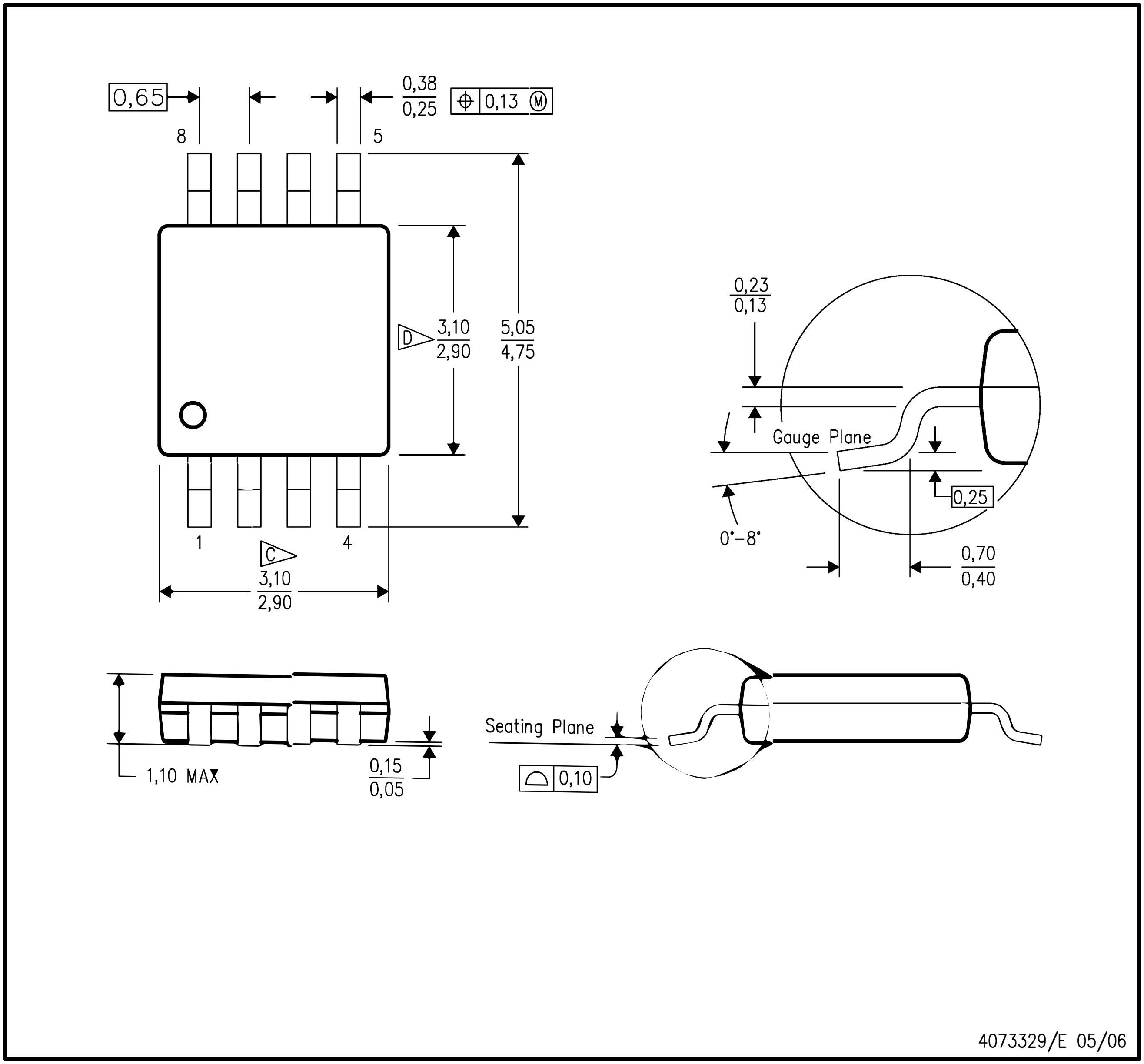


4073253-4/N 12/14

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.