MP2359

1.2A, 24V, 1.4MHz Step-Down Converter in a TSOT23-6

DESCRIPTION

The MP2359 is a monolithic step-down switch mode converter with a built-in power MOSFET. It achieves 1.2A peak output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP2359 requires a minimum number of readily available standard external components. The MP2359 is available in TSOT23-6 and SOT23-6 packages.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV2359DJ-00B	2.1"X x 1.9"Y x 0.4"Z

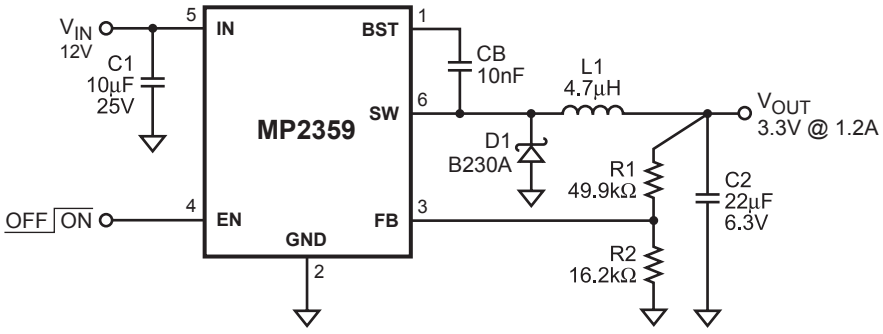
FEATURES

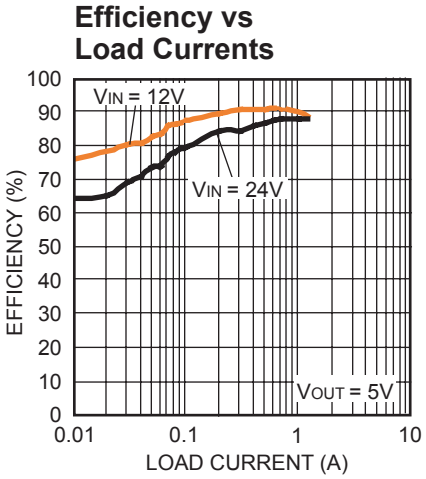
- 1.2A Peak Output Current
- 0.35Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 92% Efficiency
- 0.1μA Shutdown Mode
- Fixed 1.4MHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.5V to 24V Operating Input Range
- Output Adjustable from 0.81V to 15V
- Available in TSOT23-6 and SOT23-6 Packages

APPLICATIONS

- Distributed Power Systems
- Battery Charger
- Pre-Regulator for Linear Regulators
- WLED Drivers

TYPICAL APPLICATION



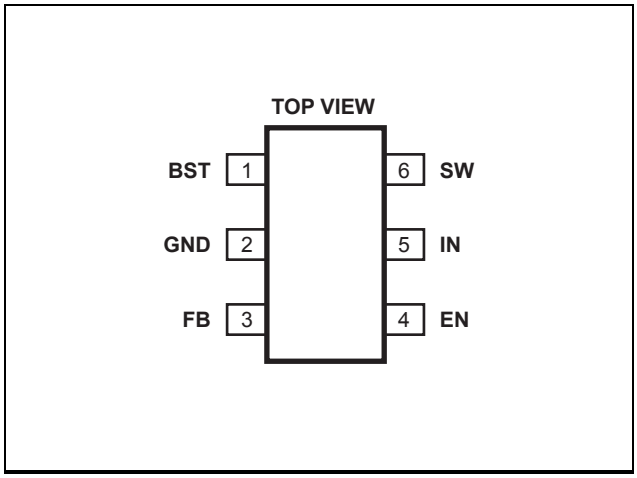


ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP2359DJ*	TSOT23-6	F8	-40°C to +85°C
MP2359DT**	SOT23-6	J6	-40°C to +85°C

*For Tape & Reel, add suffix –Z (eg. M2359DJ–Z);
For RoHS compliant packaging, add suffix –LF (eg. MP2359DJ–LF–Z)
**For Tape & Reel, add suffix –Z (eg. M2359DT–Z);
For RoHS compliant packaging, add suffix –LF (eg. MP2359DT–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 26V
V_{SW} 27V
V_{BS} ..... V_{SW} + 6V
All Other Pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
TSOT23-6 ..... 0.568W
SOT23-6 ..... 0.568W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 24V
Output Voltage V_{OUT} ..... 0.81V to 15V
Ambient Temperature ..... -40°C to +85°C
Max input current into the EN pin 300µA

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 ..... 220 .... 110.. °C/W
SOT23-6 ..... 220 .... 110.. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device function is not guaranteed outside of the recommended operating conditions.
4) Measured on JESD51-7, 4-layer PCB..

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 24V	0.790	0.810	0.830	V
Feedback Current	I_{FB}	V_{FB} = 0.8V		0.1		µA
Switch-On Resistance (5)	$R_{DS(ON)}$			0.35		Ω
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V			10	µA
Current Limit (5)				1.8		A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V	1.2	1.4	1.7	MHz
Fold-back Frequency		V_{FB} = 0V		460		kHz
Maximum Duty Cycle		V_{FB} = 0.6V		87		%
Minimum On-Time (5)	t_{ON}			100		ns
Under Voltage Lockout Threshold Rising			2.5	2.8	3.1	V
Under Voltage Lockout Threshold Hysteresis				150		mV
EN Input Low Voltage					0.4	V
EN Input High Voltage			1.2			V
EN Input Current		V_{EN} = 2V		2.1		µA
		V_{EN} = 0V		0.1		
Supply Current (Shutdown)	I_S	V_{EN} = 0V		0.1	1.0	µA
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V		0.8	1.0	mA
Thermal Shutdown (5)				150		°C

Note:
5) Guaranteed by design.

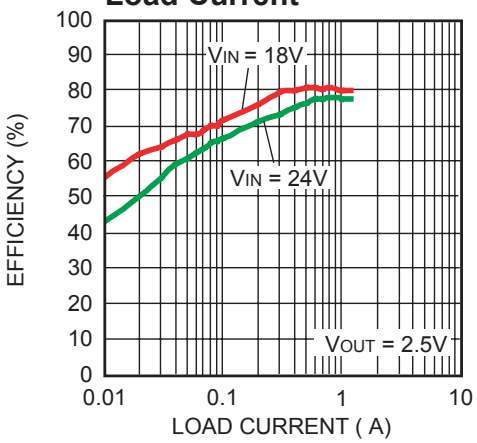
PIN FUNCTIONS

Pin #	Name	Description
1	BST	Bootstrap. A capacitor is connected between SW and BS pins to form a floating supply across the power switch driver. This capacitor is needed to drive the power switch's gate above the supply voltage.
2	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part.
3	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 250mV.
4	EN	On/Off Control Input. Pull EN above 1.2V to turn the device on. For automatic enable, connect a 100kΩ resistor between this pin and Vin pin.
5	IN	Supply Voltage. The MP2359 operates from a +4.5V to +24V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
6	SW	Switch Output.

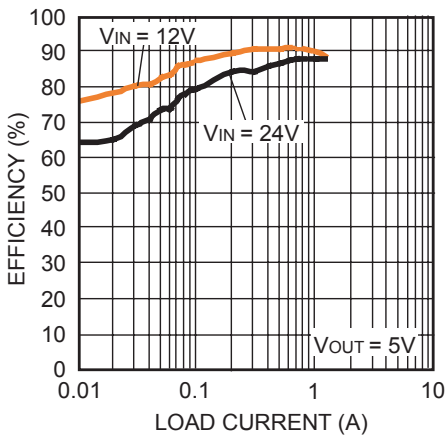
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, C1 = 10µF, C2 = 22µF, T_A = +25ºC, unless otherwise noted.

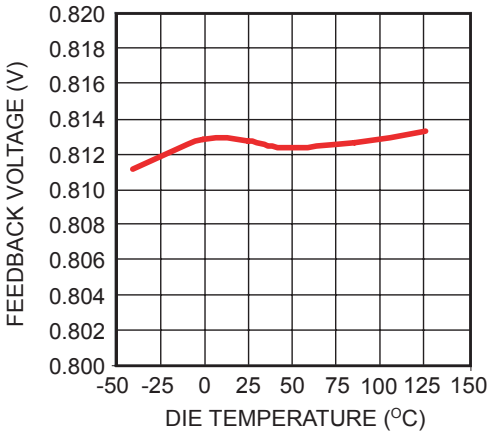
Efficiency vs Load Current



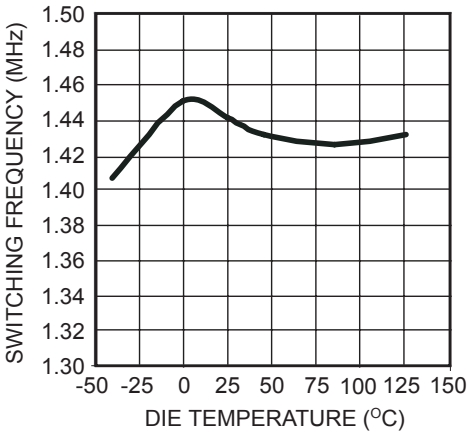
Efficiency vs Load Current



Feedback Voltage vs Die Temperature



Switching Frequency vs Die Temperature



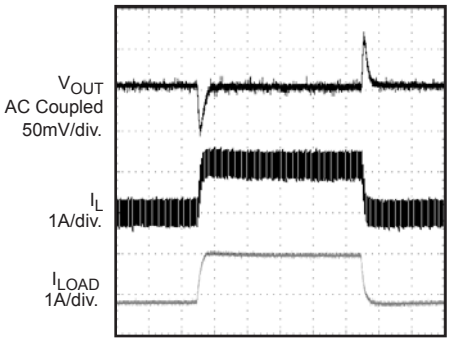
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, C1 = 10µF, C2 = 22µF, T_A = +25ºC, unless otherwise noted.

Current Limit vs Duty Cycle

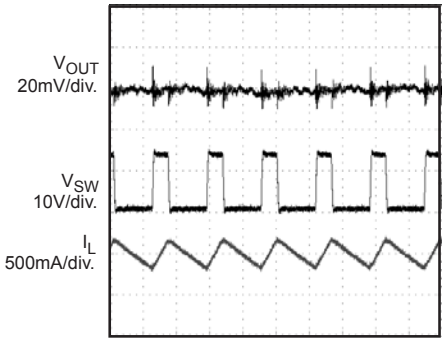
Load Transient Test

I_{OUT} = 0.2A to 0.8A step at 0.8A/µs

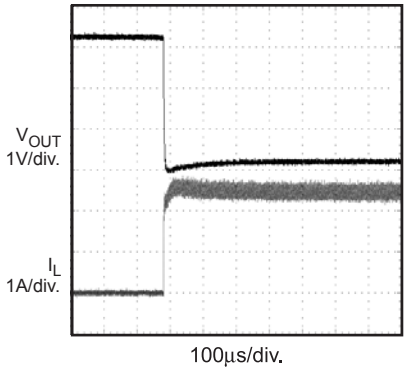


Steady State Test

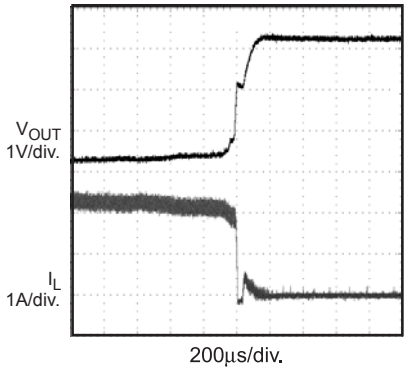
I_{OUT} = 0.5A



Short Circuit Entry

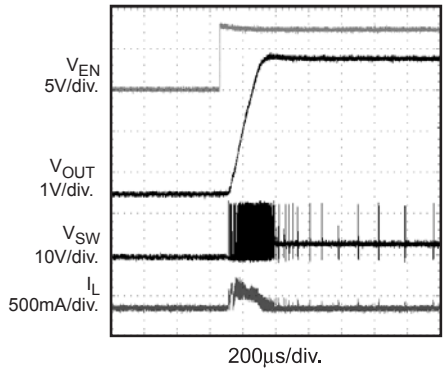


Short Circuit Recovery



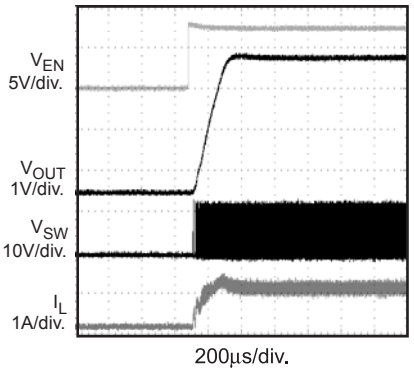
Start-up through Enable

No Load



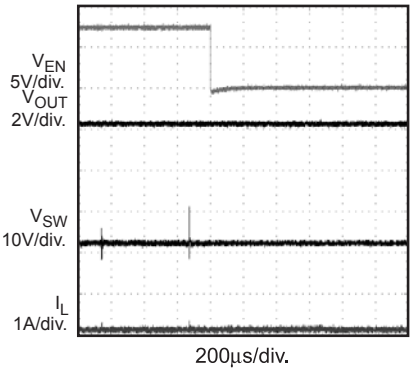
Start-up through Enable

I_{OUT} = 1A Resistive Load



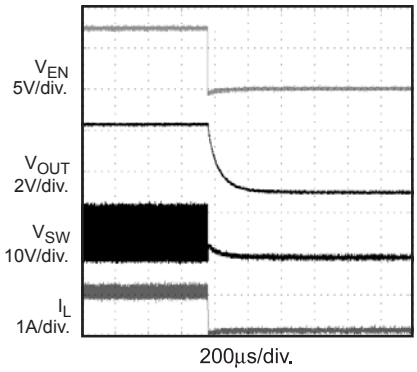
Shut-down through Enable

No Load



Shut-down through Enable

I_{OUT} = 1A Resistive Load



OPERATION

The MP2359 is a current mode buck regulator. That is, the EA output voltage is proportional to the peak inductor current.

At the beginning of a cycle, M1 is off. The EA output voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the 1.4MHz CLK signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to the Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the sum of the Current Sense Amplifier output and the Slope Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and M1 is turned off. The external Schottky rectifier diode (D1) conducts the inductor current.

If the sum of the Current Sense Amplifier output and the Slope Compensation signal does not exceed the EA output for a whole cycle, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.81V bandgap reference. The polarity is such that a FB pin voltage lower than 0.81V increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage also increases current delivered to the output.

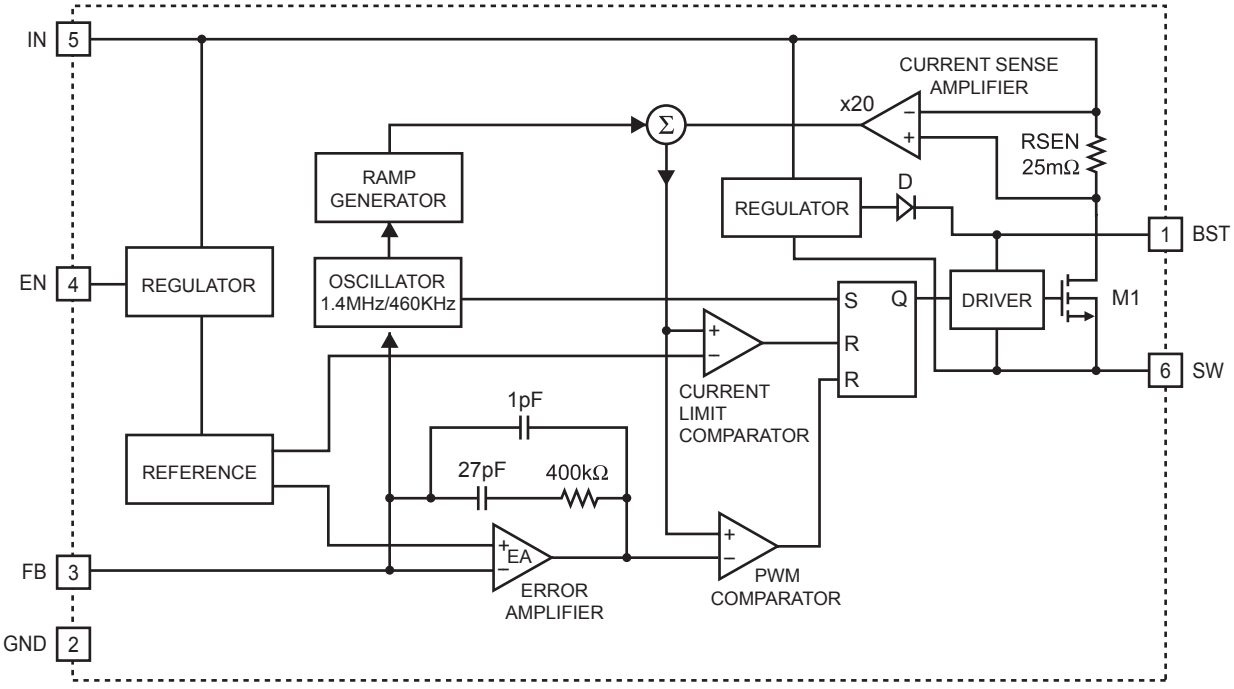


Figure 1—Functional Block Diagram

APPLICATION INFORMATION

Setting Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). Table 1 shows a list of resistor selection for common output voltages. The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). R2 can be determined by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.81V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	80.6 (1%)	64.9 (1%)
2.5	49.9 (1%)	23.7 (1%)
3.3	49.9 (1%)	16.2 (1%)
5	49.9 (1%)	9.53 (1%)

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor's DC resistance should be less than 200mΩ. Refer to Table 2 for suggested surface mount inductors. For most designs, the required inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, a larger inductance is recommended for improved efficiency. See Table 2 for suggested inductors.

Also note that the maximum recommended load current is 1A if the duty cycle exceeds 35%.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from passing through the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7μF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 22μF ceramic capacitor will be sufficient.

PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure2 for references.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and schottky diode.
2) Keep the connection of schottky diode between SW pin and input power ground as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability. For single layer PCB, exposed pad should not be soldered.

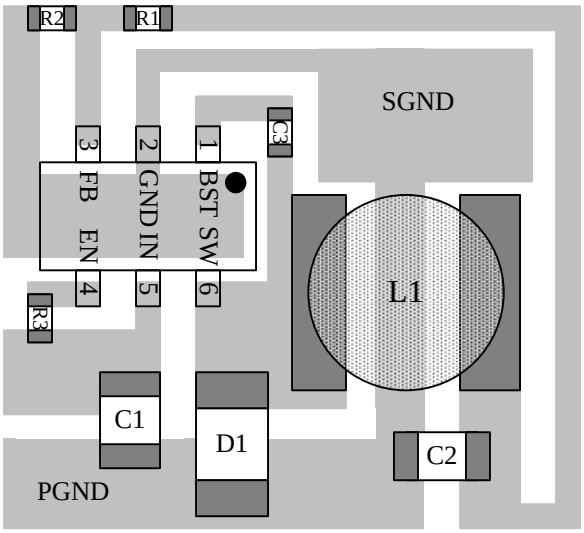


Figure 2—PCB Layout

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Fig.3

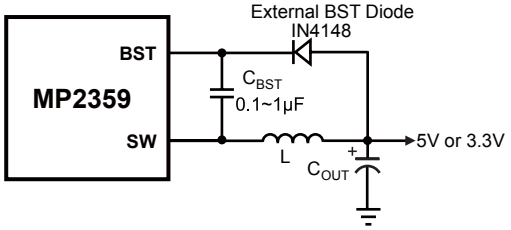


Figure 3—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

Table 2—Suggested Surface Mount Inductors

Manufacturer	Part Number	Inductance(μH)	Max DCR(Ω)	Current Rating (A)	Dimensions L x W x H (mm^3)
Toko	A921CY-4R7M	4.7	0.027	1.66	6 x 6.3 x 3
Sumida	CDRH4D28C/LD	4.7	0.036	1.5	5.1 x 5.1 x 3
Wurth Electronics	7440530047	4.7	0.038	2.0	5.8 x 5.8 x 2.8

TYPICAL APPLICATION CIRCUITS

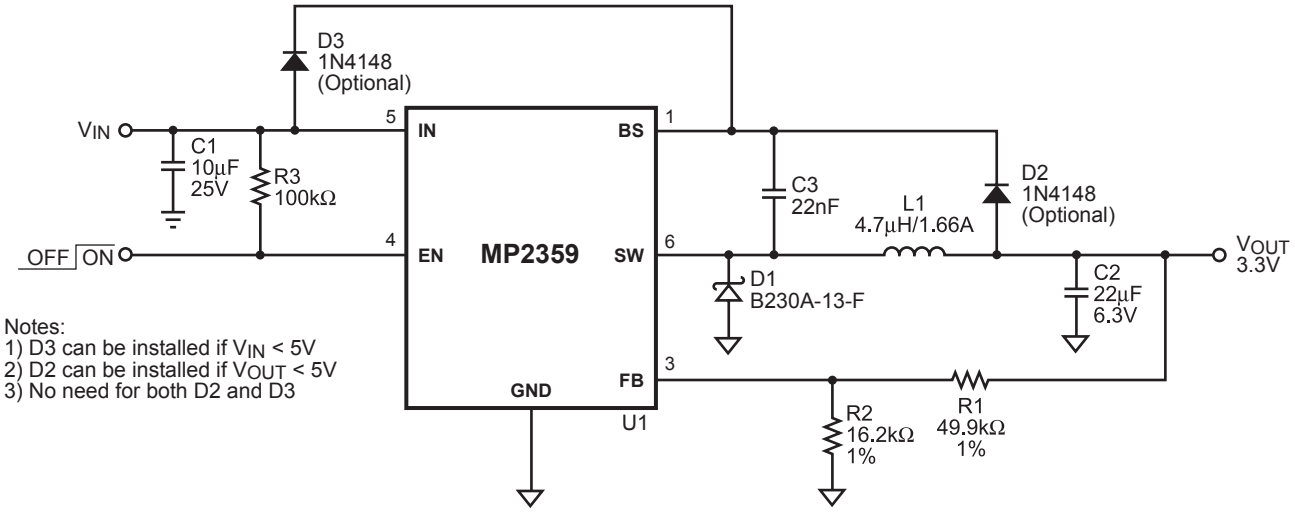


Figure 4—1.4MHz, 3.3V Output at 1A Step-Down Converter

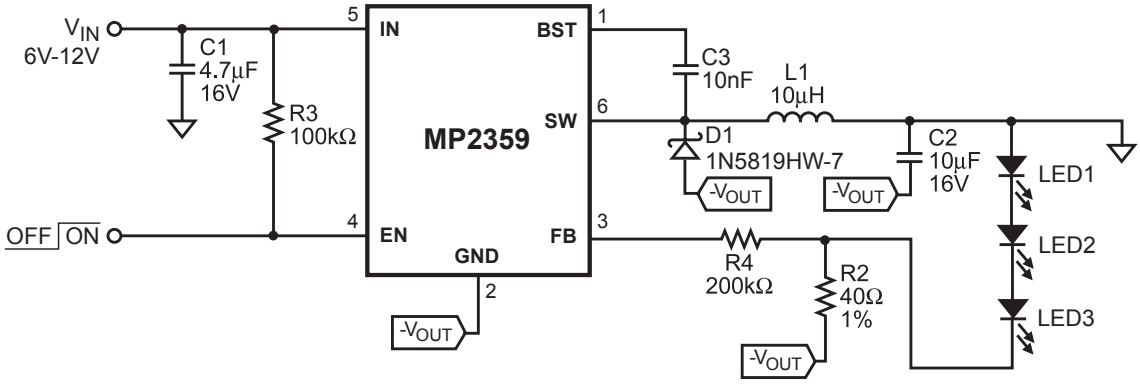
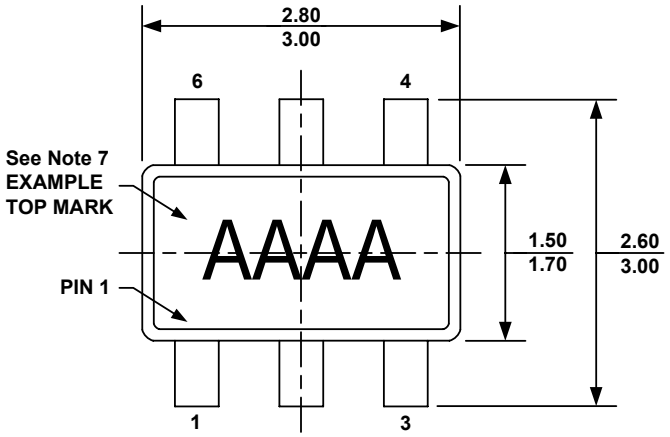


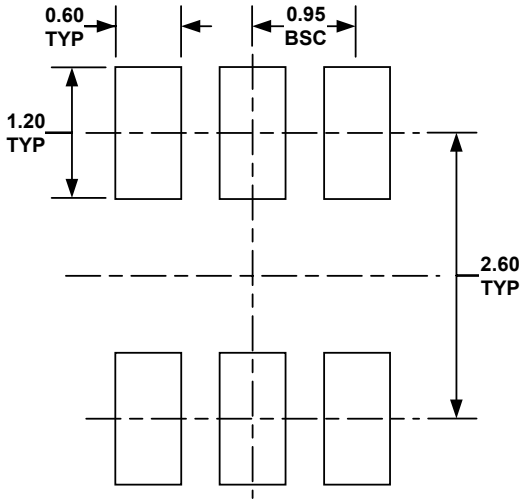
Figure 5—White LED Driver Application

PACKAGE INFORMATION

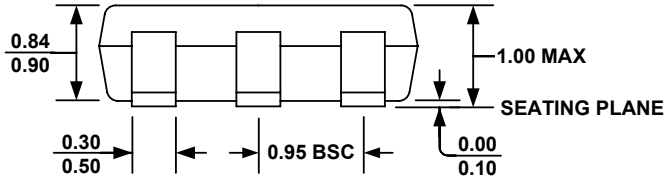
TSOT23-6



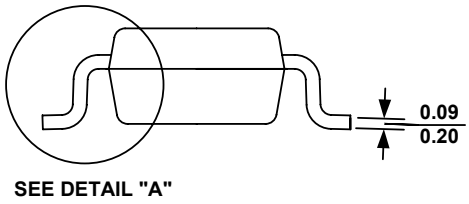
TOP VIEW



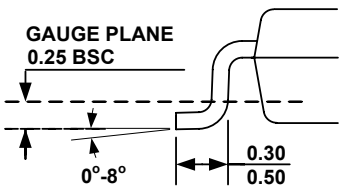
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

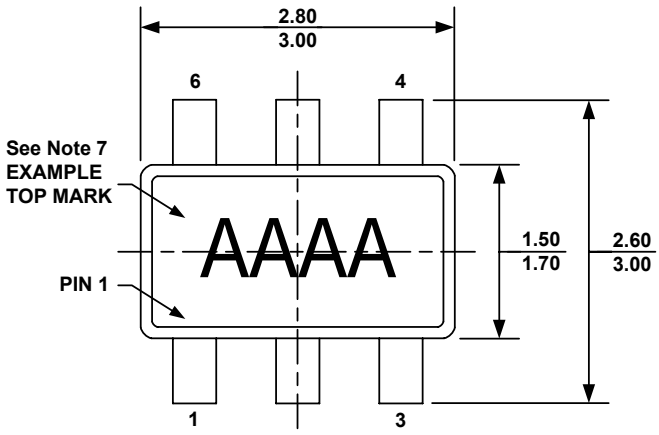


DETAIL “A”

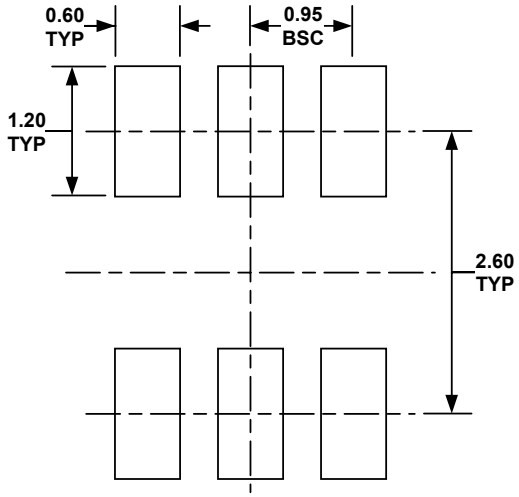
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

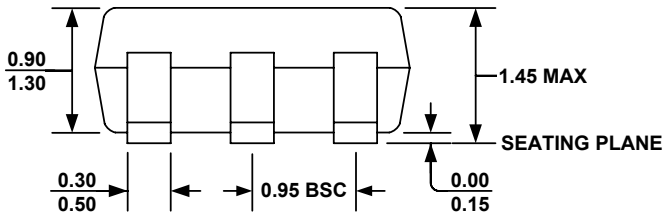
SOT23-6



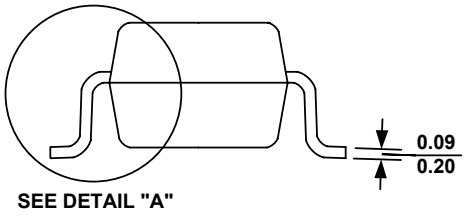
TOP VIEW



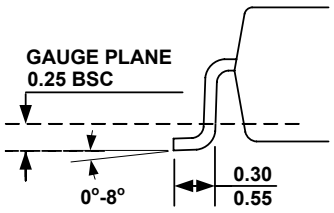
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)