0.03-μV/°C Drift, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift OPERATIONAL AMPLIFIERS

Check for Samples: OPA188, OPA2188, OPA4188

FEATURES

- **Low Offset Voltage: 25 μV (max)**
- **Zero-Drift: 0.03 μV/°C**
- **Low Noise: 8.8 nV/√Hz**
  0.1-Hz to 10-Hz Noise: 0.25 μV_{PP}
- **Excellent DC Precision:**
  PSRR: 142 dB
  CMRR: 146 dB
  Open-Loop Gain: 136 dB
- **Gain Bandwidth: 2 MHz**
- **Quiescent Current: 475 μA (max)**
- **Wide Supply Range: ±2 V to ±18 V**
- **Rail-to-Rail Output:**
  Input Includes Negative Rail
- **RFI Filtered Inputs**
- ***Micro*SIZE Packages**

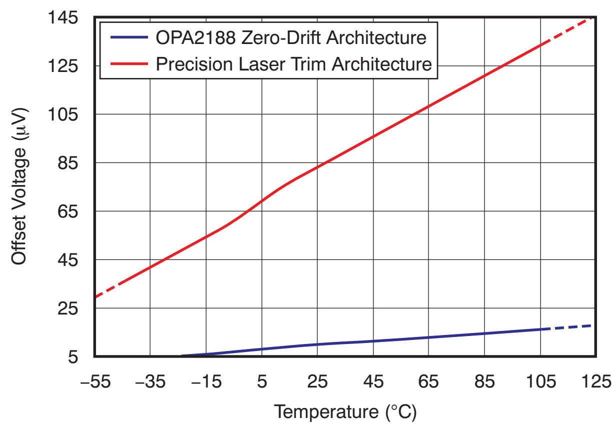
APPLICATIONS

- **Bridge Amplifiers**
- **Strain Gauges**
- **Test Equipment**
- **Transducer Applications**
- **Temperature Measurement**
- **Electronic Scales**
- **Medical Instrumentation**
- **Resister Thermal Detectors**
- **Precision Active Filters**

DESCRIPTION

The OPAx188 series operational amplifiers use TI proprietary auto-zeroing techniques to provide low offset voltage (25 μV, max), and near zero-drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 15 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of +4.0 V to +36 V (±2 V to ±18 V).

The single version is available in the *Micro*SIZE SOT23-5, MSOP-8, and SO-8 packages; the dual is offered in MSOP-8 and SO-8 packages; the quad is offered in SO-14 and TSSOP-14 packages. All versions are specified for operation from –40°C to +105°C.



Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (μV)	OFFSET VOLTAGE DRIFT (μV/°C)	BANDWIDTH (MHz)
Single	OPA188 (4 V to 36 V)	25	0.085	2
Single	OPA333 (5 V)	10	0.05	0.35
	OPA378 (5 V)	50	0.25	0.9
	OPA735 (12 V)	5	0.05	1.6
Dual	OPA2188 (4 V to 36 V)	25	0.085	2
	OPA2333 (5 V)	10	0.05	0.35
	OPA2378 (5 V)	50	0.25	0.9
	OPA2735 (12 V)	5	0.05	1.6
Quad	OPA4188 (4 V to 36 V)	25	0.085	2
Quad	OPA4330 (5 V)	50	0.25	0.35

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
SINGLE						
OPA188(2)	SOT23-5	DBV	–40°C to +105°C	TBD	OPA188AIDBVT	Tape and Reel, 250
					OPA188AIDBVR	Tape and Reel, 3000
	SO-8	D	–40°C to +105°C	OPA188A	OPA188AID	Rails, 100
					OPA188AIDR	Tape and Reel, 2500
	MSOP-8	DGK	–40°C to +105°C	TBD	OPA188AIDGKT	Tape and Reel, 250
					OPA188AIDGKR	Tape and Reel, 2500
DUAL						
OPA2188	SO-8	D	–40°C to +105°C	2188	OPA2188AID	Rails, 100
					OPA2188AIDR	Tape and Reel, 2500
	MSOP-8	DGK	–40°C to +105°C	2188	OPA2188AIDGKT	Tape and Reel, 250
					OPA2188AIDGKR	Tape and Reel, 2500
QUAD						
OPA4188(2)	SO-14	D	–40°C to +105°C	OPA4188A	OPA4188AID	Rails, 90
					OPA4188AIDR	Tape and Reel, 2000
	TSSOP-14	PW	–40°C to +105°C	OPA4188A	OPA4188AIPW	Rails, 90
					OPA4188AIPWR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Product preview device.

ABSOLUTE MAXIMUM RATINGS

		OPAx188	UNIT
Supply voltage		±20, 40 (single supply)	V
Signal input terminals	Voltage	(V–) – 0.5 to (V+) + 0.5	V
	Current(1)	±10	mA
Output short-circuit(2)		Continuous	
Operating temperature		–55 to +125	°C
Storage temperature		–65 to +150	°C
Junction temperature		+150	°C
ESD ratings	Human body model (HBM)	1.5	kV
	Charged device model (CDM)	1	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: High-Voltage Operation

V_S = ±4 V to ±18 V (V_S = +8 V to +36 V)
Boldface limits apply over the specified temperature range, **T_A = –40°C to +105°C.**
At T_A = +25°C, R_L = 10 kΩ connected to $V_S/2$, and $V_{COM} = V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER		CONDITIONS	OPA188, OPA2188, OPA4188 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			6	25	μV
dV_{OS}/dT	**vs Temperature**			**0.03**	**0.085**	**μV/°C**
PSRR	vs power supply	V_S = 4 V to 36 V, $V_{CM} = V_S/2$		0.075	0.3	μV/V
	vs temperature	**V_S = 4 V to 36 V, $V_{CM} = V_S/2$**			**0.3**	**μV/V**
	Long-term stability			See note(1)		μV
	Channel separation, dc			1		μV/V
INPUT BIAS CURRENT						
I_B	Input bias current	$V_{CM} = V_S/2$		±160	±850	pA
	over temperature	**–40°C to +105°C**			**±4**	**nA**
I_{OS}	Input offset current			±320	±1700	pA
	over temperature	**–40°C to +105°C**			**±2**	**nA**
NOISE						
e_n	Input voltage noise, f = 0.1 Hz to 10 Hz			0.25		μV_{PP}
e_n	Input voltage noise density, f = 1 kHz			8.8		$nV/\sqrt{Hz}$
i_n	Input current noise density, f = 1 kHz			7		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	**Common-mode voltage range**		**V–**		**(V+) – 1.5**	**V**
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	120	134		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V	130	146		dB
	over temperature	**(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V**	**120**	**126**		**dB**
INPUT IMPEDANCE						
	Differential			100/6		MΩ/pF
	Common-mode			6/9.5		10^{12} Ω/pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	130	136		dB
	Open-loop voltage gain	**(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ**	**120**	**126**		**dB**
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	G = +1		0.8		V/μs
	Settling time, 0.1%	V_S = ±18 V, G = 1, 10-V step		20		μs
	Settling time, 0.01%	V_S = ±18 V, G = 1, 10-V step		27		μs
	Overload recovery time	$V_{IN} \times G = V_S$		1		μs
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_{OUT} = 1 Vrms		0.0001		%

(1) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 μV.

ELECTRICAL CHARACTERISTICS: High-Voltage Operation (continued)

V_S = ±4 V to ±18 V (V_S = +8 V to +36 V)
Boldface limits apply over the specified temperature range, **T_A = –40°C to +105°C.**
At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA188, OPA2188, OPA4188 MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
	Voltage output swing from rail	R_L = 10 kΩ		220	250	mV
	Voltage output swing from rail	**R_L = 10 kΩ**		**310**	**350**	**mV**
I_{SC}	Short-circuit current			±18		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range		4 to 36 (±2 to ±18)			V
I_Q	Quiescent current (per amplifier)	V_S = ±4 V to V_S = ±18 V		415	475	μA
I_Q	**over temperature**	**I_O = 0 mA**			**525**	**μA**
TEMPERATURE RANGE						
	Specified range		–40		+105	°C
	Operating range		–40		+125	°C
	Storage range		–65		+150	°C

ELECTRICAL CHARACTERISTICS: Low-Voltage Operation

V_S = ±2 V to < ±4 V (V_S = +4 V to < +8 V)
Boldface limits apply over the specified temperature range, **T_A = –40°C to +105°C.**
At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA188, OPA2188, OPA4188 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			6	25	μV
dV_{OS}/dT	**vs temperature**			**0.03**	**0.085**	**μV/°C**
PSRR	vs power supply	V_S = 4 V to 36 V, V_{CM} = V_S/2		0.075	0.3	μV/V
	vs temperature	**V_S = 4 V to 36 V, V_{CM} = V_S/2**			**0.3**	**μV/V**
	Long-term stability			See Note (1)		μV
	Channel separation, dc			1		μV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		±160	±850	pA
	over temperature	**–40°C to +105°C**			**±4**	**nA**
I_{OS}	Input offset current			±320	±1700	pA
	over temperature	**–40°C to +105°C**			**±2**	**nA**
NOISE						
e_n	Input voltage noise, f = 0.1 Hz to 10 Hz			0.25		μV_{PP}
	Input voltage noise density, f = 1 kHz			8.8		$nV/\sqrt{Hz}$
i_n	Input current noise density, f = 1 kHz			7		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	**Common-mode voltage range**		**V–**		**(V+) – 1.5**	**V**
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	106	114		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V	114	120		dB
	over temperature	**(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V**	**110**	**120**		**dB**
INPUT IMPEDANCE						
	Differential			100/6		MΩ/pF
	Common-mode			6/95		10^{12} Ω/pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 5 kΩ, V_S = 5 V	110	120		dB
		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	120	130		dB
	Open-loop voltage gain	**(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ**	**114**	**120**		**dB**
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	G = +1		0.8		V/μs
	Overload recovery time	V_{IN} × G = V_S		1		μs
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_{OUT} = 1 Vrms		0.0001		%

(1) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 μV.

ELECTRICAL CHARACTERISTICS: Low-Voltage Operation (continued)

V_S = ±2 V to < ±4 V (V_S = +4 V to < +8 V)
Boldface limits apply over the specified temperature range, **T_A = –40°C to +105°C.**
At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA188, OPA2188, OPA4188 MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
	Voltage output swing from rail	**R_L = 10 kΩ**		**310**	**350**	**mV**
I_{SC}	Short-circuit current			±18		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range			4 to 36 (±2 to ±18)		V
I_Q	Quiescent current (per amplifier)	V_S = ±2 V to V_S = ±4 V		385	440	μA
	over temperature	**I_O = 0 mA**			**525**	**μA**
TEMPERATURE RANGE						
	Specified range		–40		+105	°C
	Operating range		–40		+125	°C
	Storage range		–65		+150	°C

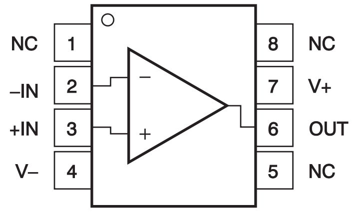
THERMAL INFORMATION: OPA2188

THERMAL METRIC(1)		OPA2188ID D 8 PINS	OPA2188IDGK DGK 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	111.0	159.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	54.9	37.4	
θ_{JB}	Junction-to-board thermal resistance	51.7	48.5	
ψ_{JT}	Junction-to-top characterization parameter	9.3	1.2	
ψ_{JB}	Junction-to-board characterization parameter	51.1	77.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

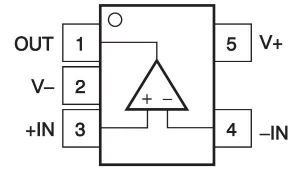
PIN CONFIGURATIONS

OPA188
D, DGK PACKAGES (SO-8, MSOP-8)
(TOP VIEW)

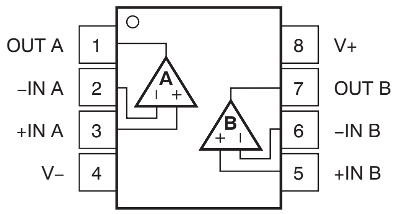


(1) NC = no connection.

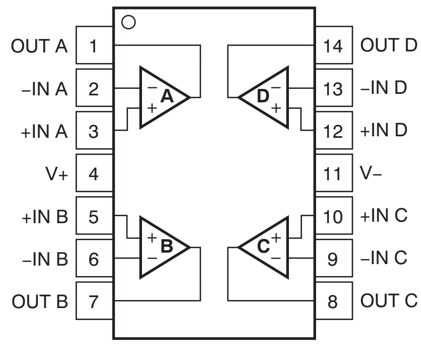
OPA188
DBV PACKAGE (SOT23-5)
(TOP VIEW)



OPA2188
D, DGK PACKAGES (SO-8, MSOP-8)
(TOP VIEW)



OPA4188
D, PW PACKAGES (SO-14, TSSOP-14)
(TOP VIEW)



TYPICAL CHARACTERISTICS

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4, Figure 5
Offset Voltage vs Power Supply	Figure 6
I_B and I_{OS} vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 10
CMRR vs Temperature	Figure 11, Figure 12
PSRR vs Temperature	Figure 13
0.1-Hz to 10-Hz Noise	Figure 14
Input Voltage Noise Spectral Density vs Frequency	Figure 15
THD+N Ratio vs Frequency	Figure 16
THD+N vs Output Amplitude	Figure 17
Quiescent Current vs Supply Voltage	Figure 18
Quiescent Current vs Temperature	Figure 19
Open-Loop Gain and Phase vs Frequency	Figure 20
Closed-Loop Gain vs Frequency	Figure 21
Open-Loop Gain vs Temperature	Figure 22
Open-Loop Output Impedance vs Frequency	Figure 23
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 24, Figure 25
No Phase Reversal	Figure 26
Positive Overload Recovery	Figure 27
Negative Overload Recovery	Figure 28
Small-Signal Step Response (100 mV)	Figure 29, Figure 30
Large-Signal Step Response	Figure 31, Figure 32
Large-Signal Settling Time (10-V Positive Step)	Figure 33
Large-Signal Settling Time (10-V Negative Step)	Figure 34
Short-Circuit Current vs Temperature	Figure 35
Maximum Output Voltage vs Frequency	Figure 36
Channel Separation vs Frequency	Figure 37
EMIRR IN+ vs Frequency	Figure 38

TYPICAL CHARACTERISTICS

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

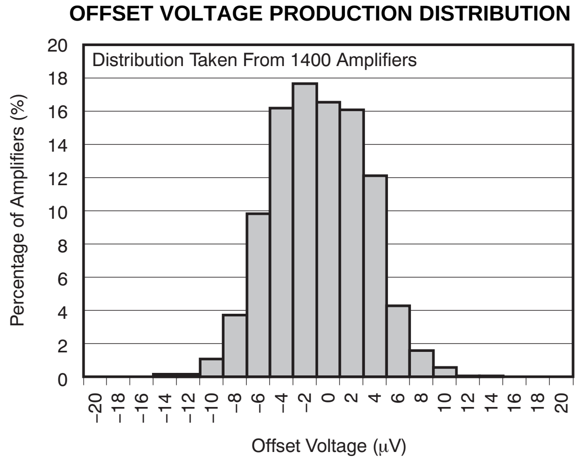


Figure 1.

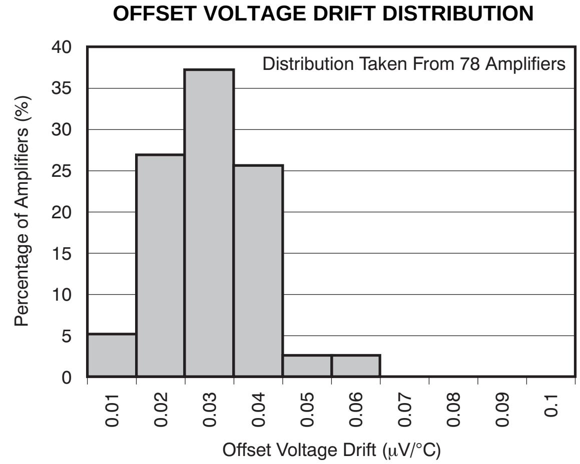


Figure 2.

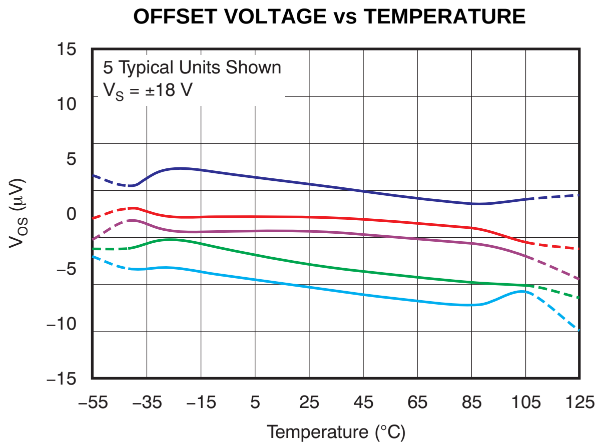


Figure 3.

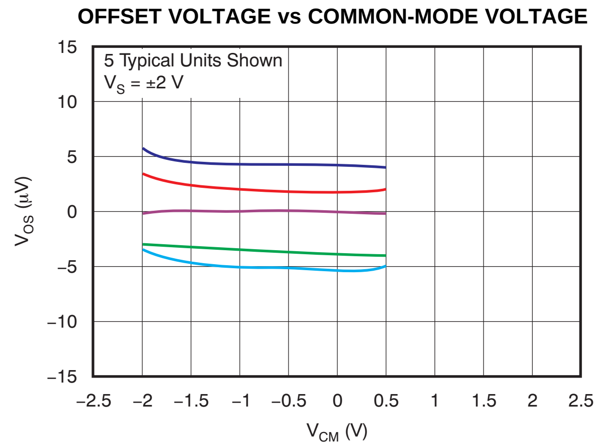


Figure 4.

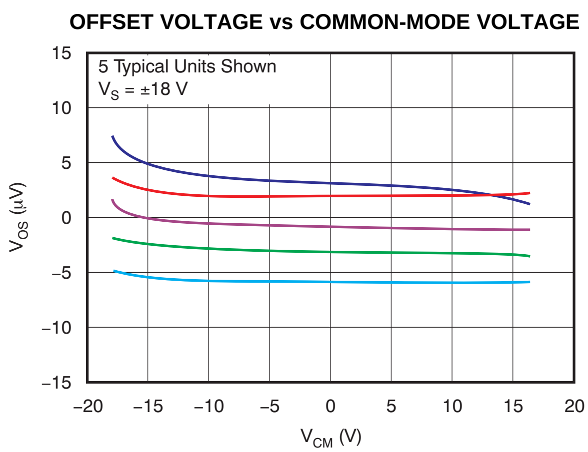


Figure 5.

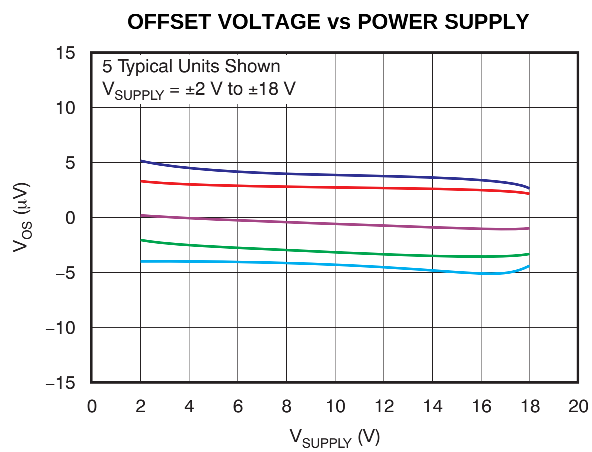


Figure 6.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

I_B AND I_{OS} vs COMMON-MODE VOLTAGE

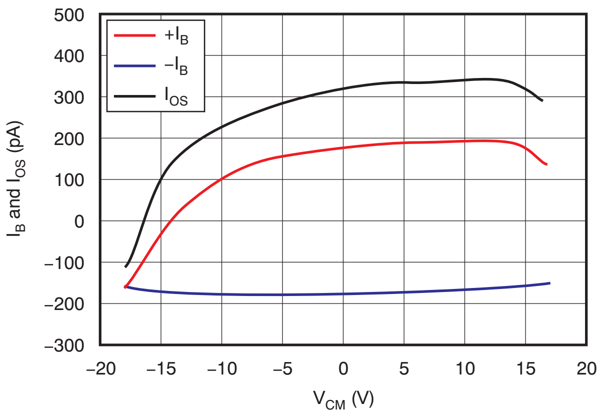


Figure 7.

INPUT BIAS CURRENT vs TEMPERATURE

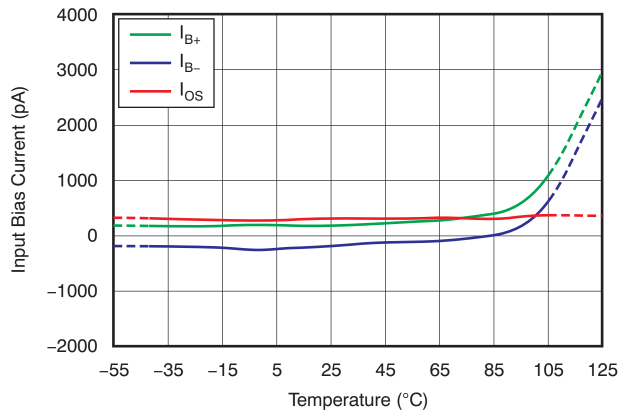


Figure 8.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (Maximum Supply)

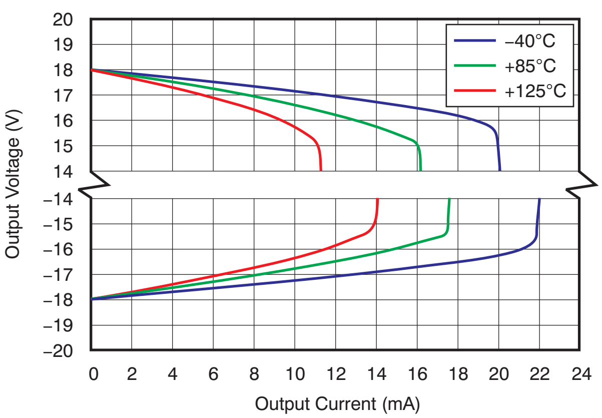


Figure 9.

CMRR AND PSRR vs FREQUENCY (Referred-to-Input)

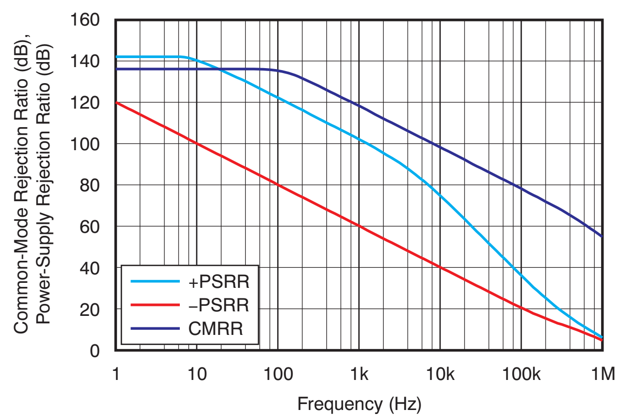


Figure 10.

CMRR vs TEMPERATURE

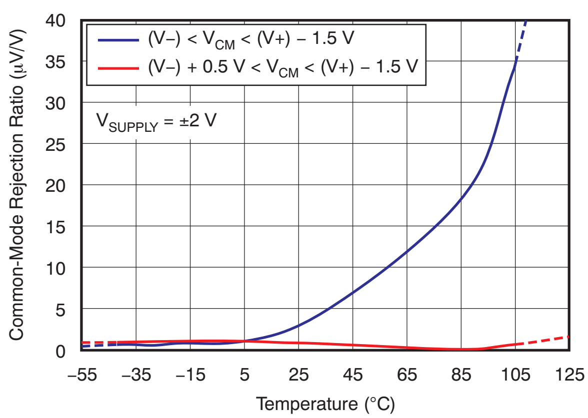


Figure 11.

CMRR vs TEMPERATURE

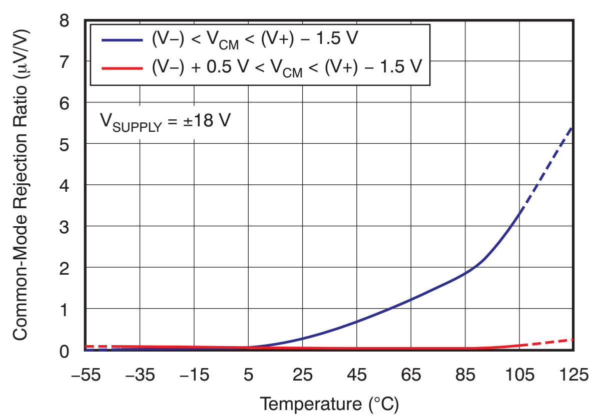


Figure 12.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

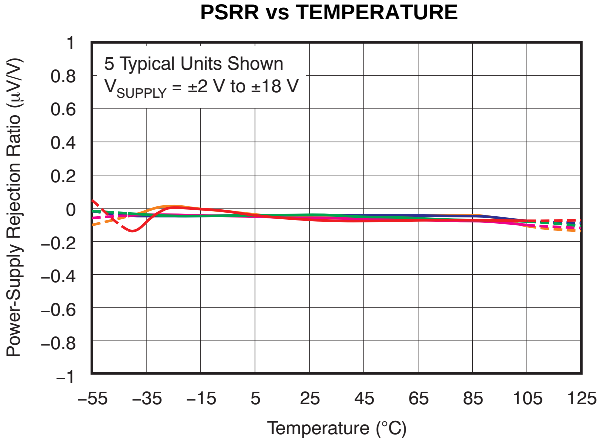


Figure 13.

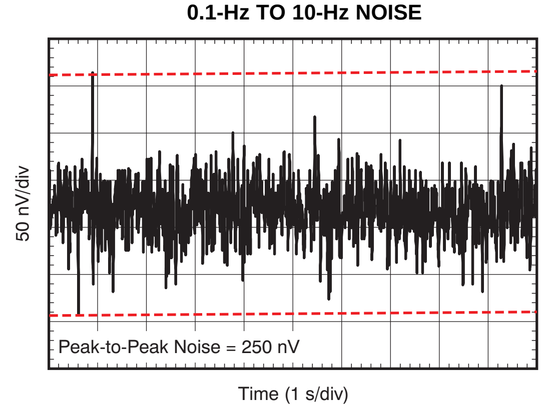


Figure 14.

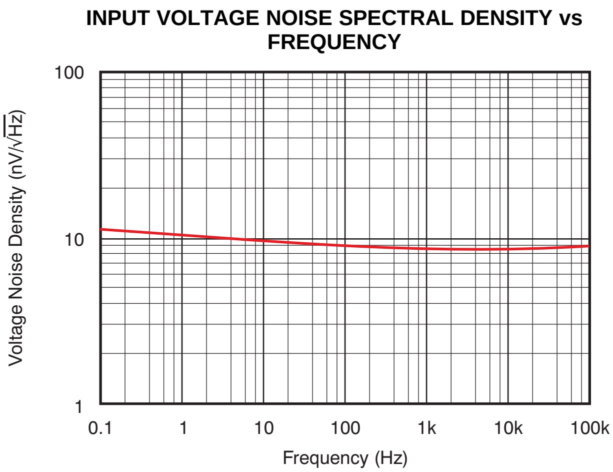


Figure 15.

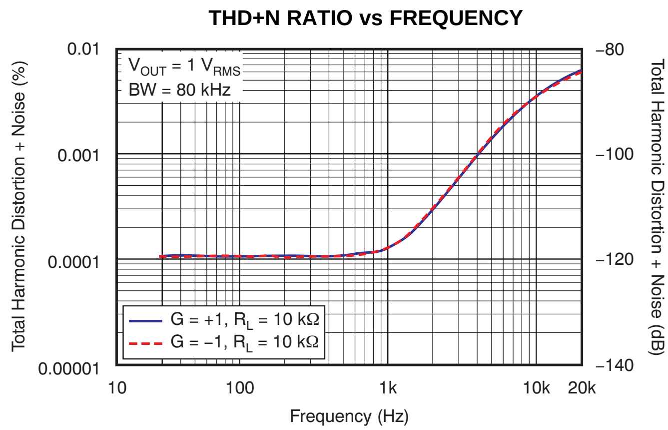


Figure 16.

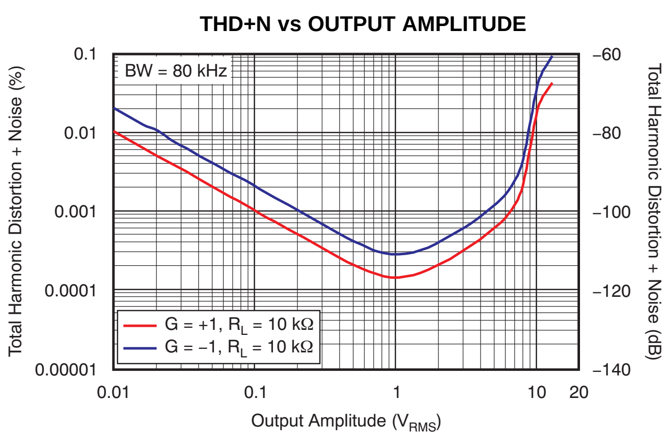


Figure 17.

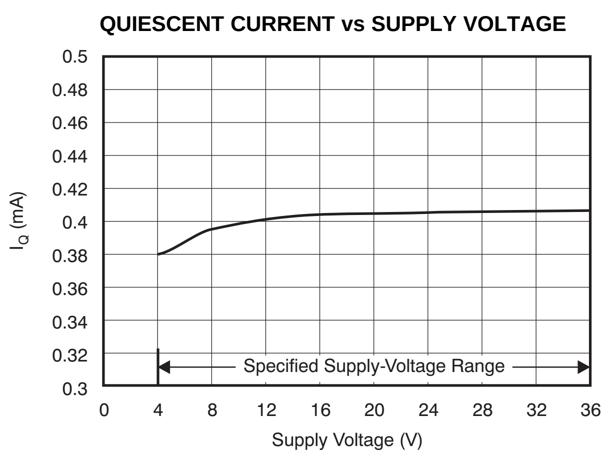


Figure 18.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

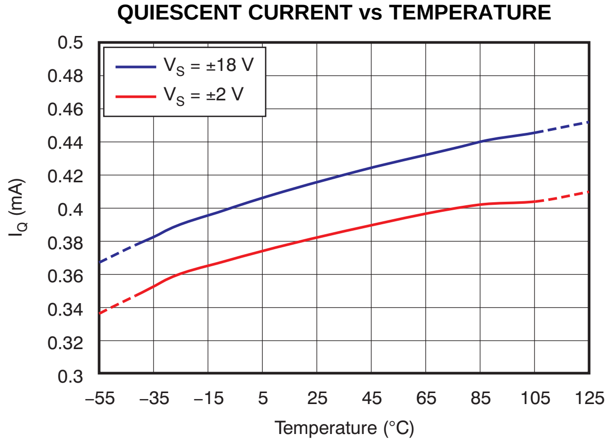


Figure 19.

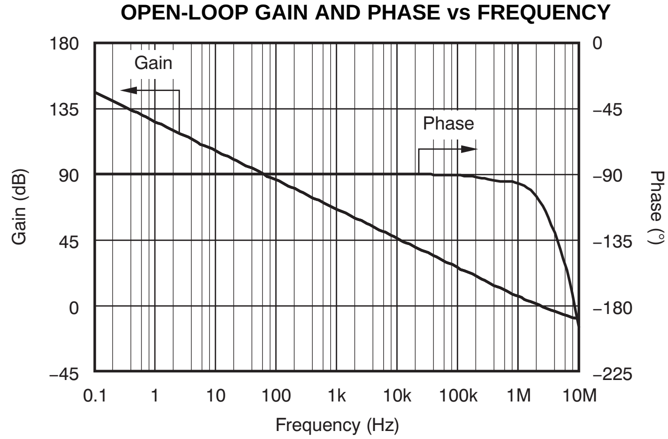


Figure 20.

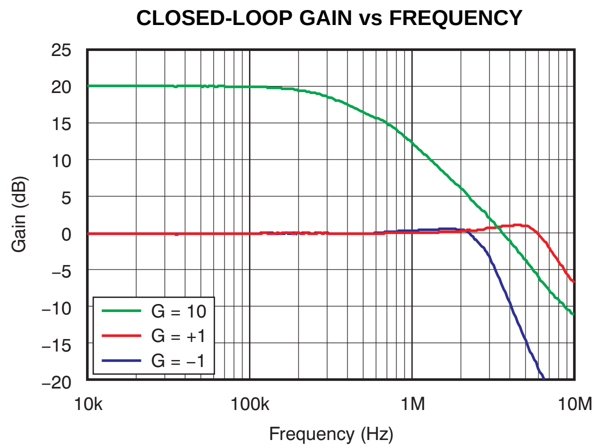


Figure 21.

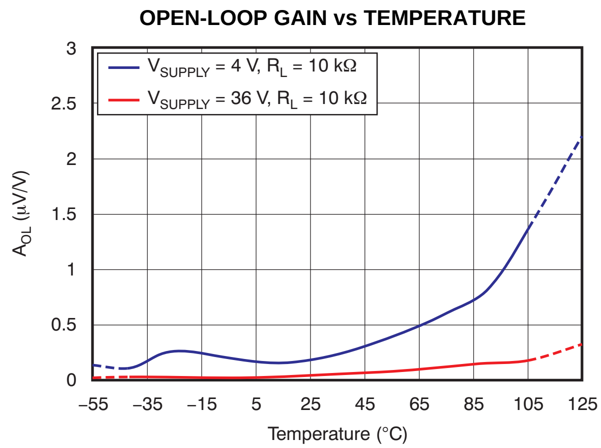


Figure 22.

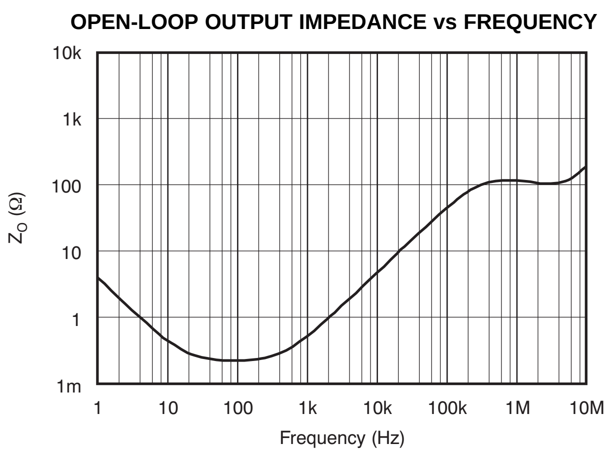


Figure 23.

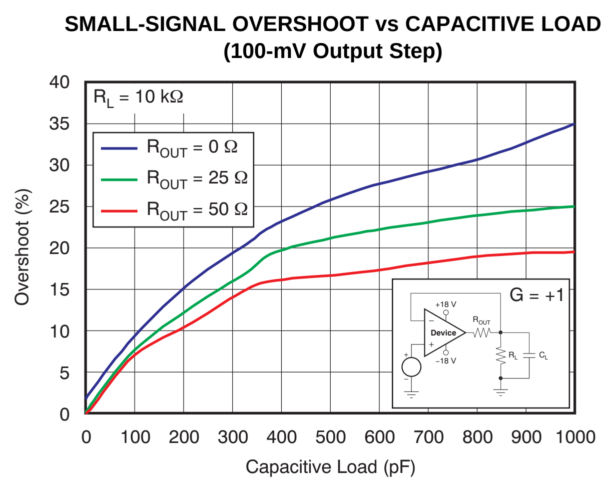


Figure 24.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)

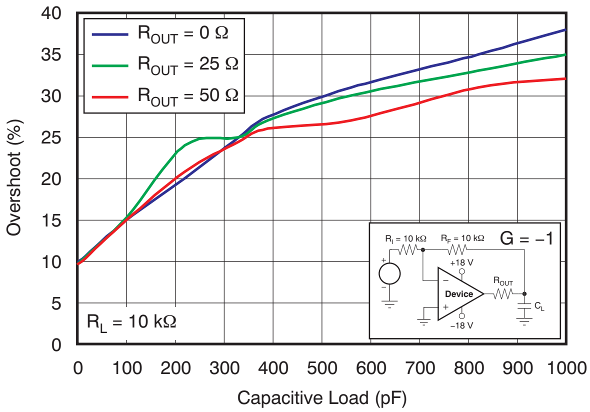


Figure 25.

NO PHASE REVERSAL

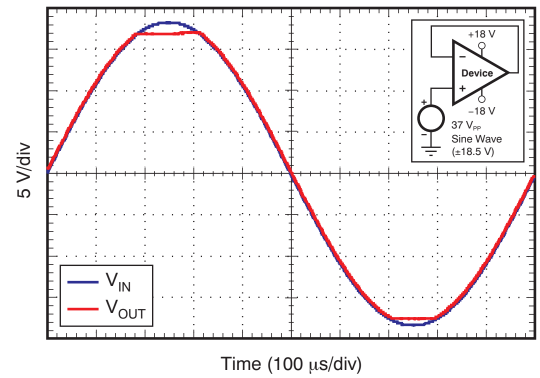


Figure 26.

POSITIVE OVERLOAD RECOVERY

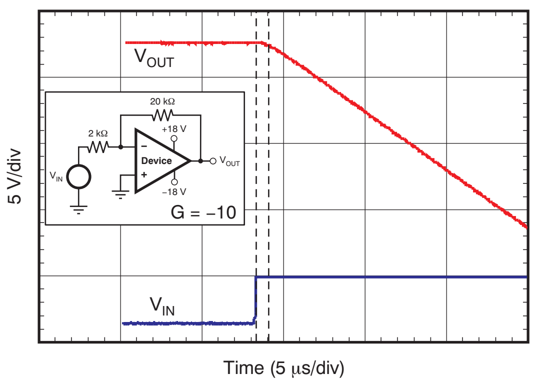


Figure 27.

NEGATIVE OVERLOAD RECOVERY

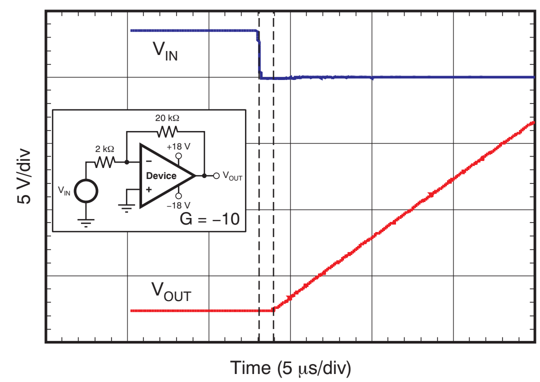


Figure 28.

SMALL-SIGNAL STEP RESPONSE (100 mV)

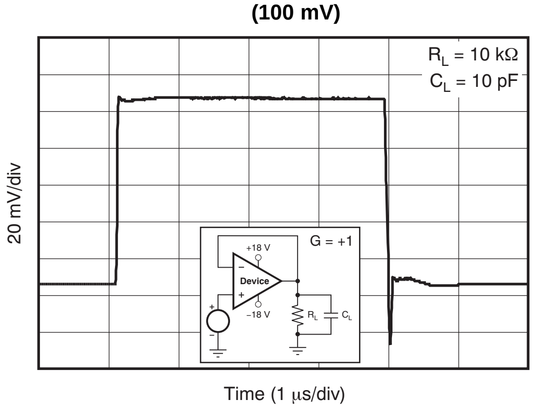


Figure 29.

SMALL-SIGNAL STEP RESPONSE (100 mV)

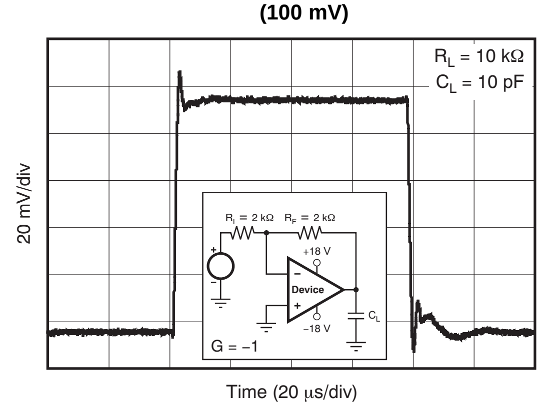


Figure 30.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

LARGE-SIGNAL STEP RESPONSE

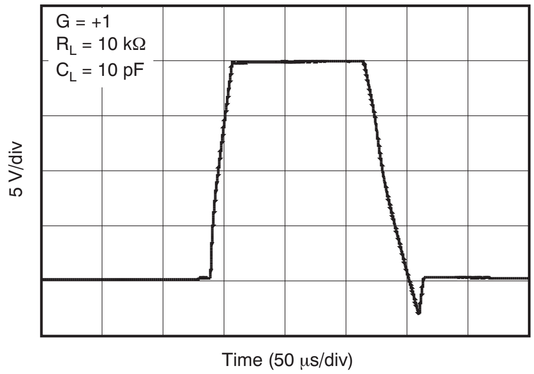


Figure 31.

LARGE-SIGNAL STEP RESPONSE

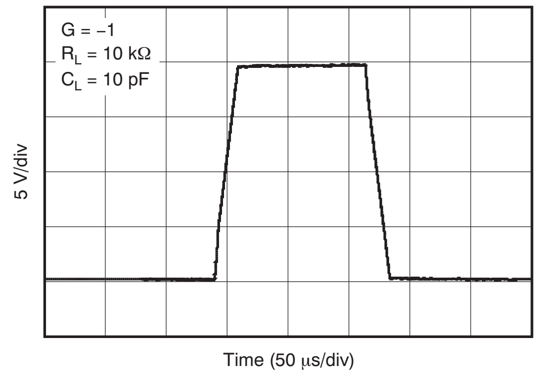


Figure 32.

LARGE-SIGNAL SETTLING TIME (10-V Positive Step)

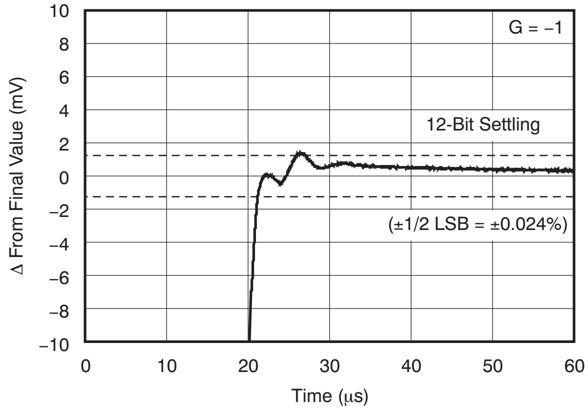


Figure 33.

LARGE-SIGNAL SETTLING TIME (10-V Negative Step)

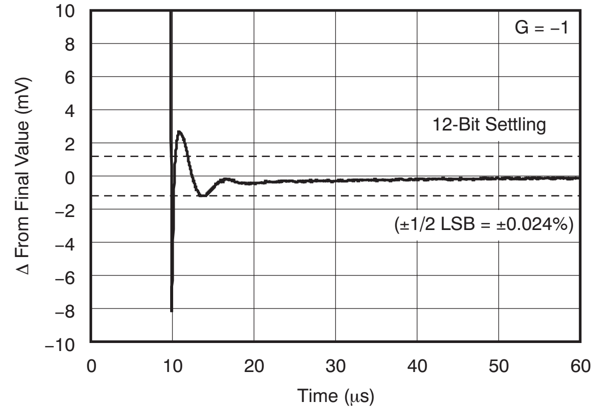


Figure 34.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

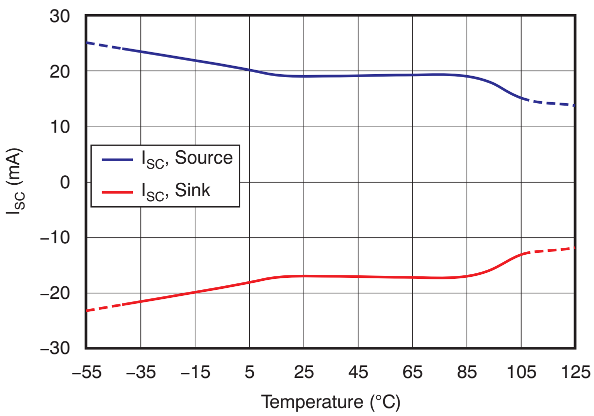


Figure 35.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

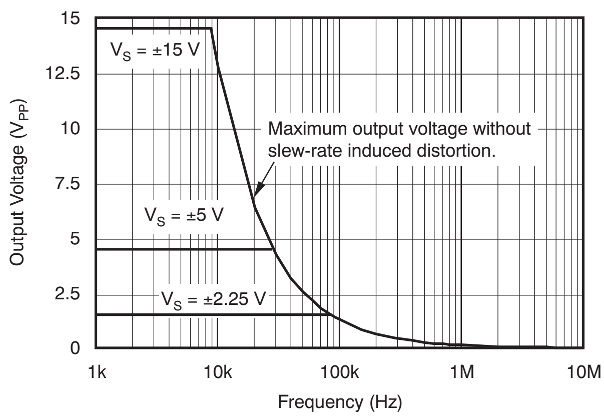


Figure 36.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

CHANNEL SEPARATION vs FREQUENCY

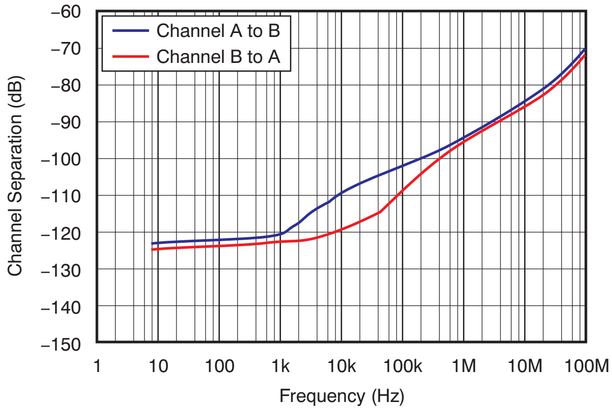


Figure 37.

EMIRR IN+ vs FREQUENCY

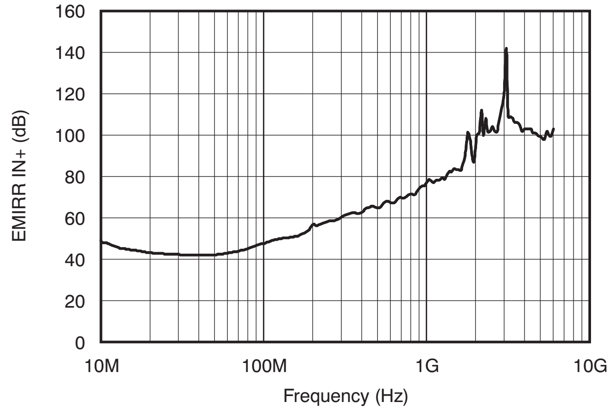


Figure 38.

APPLICATION INFORMATION

The OPAx188 family of operational amplifiers combine precision offset and drift with excellent overall performance, making them ideal for many precision applications. The precision offset drift of only 0.085 μV/°C provides stability over the entire temperature range. In addition, the device offers excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate.

OPERATING CHARACTERISTICS

The OPAx188 family of amplifiers is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many of the specifications apply from –40°C to +105°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

EMI REJECTION

The OPAx188 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx188 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 39 shows the results of this testing on the OPAx188. Detailed information can also be found in the Application Report EMI Rejection Ratio of Operational Amplifiers (*SBOA128*), available for download from the TI website.

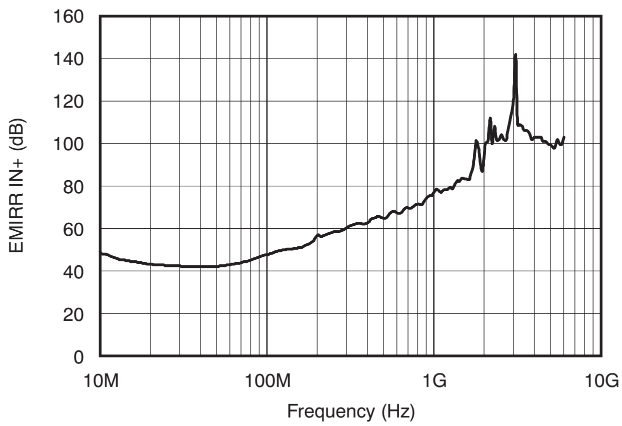


Figure 39. OPAx188 EMIRR Testing

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are recommended. Low-loss, 0.1-μF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

PHASE-REVERSAL PROTECTION

The OPAx188 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx188 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 40.

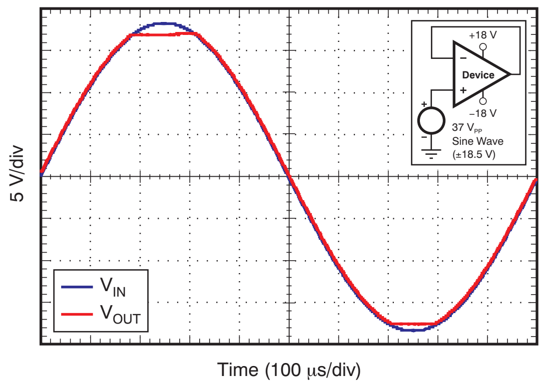


Figure 40. No Phase Reversal

CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPAx188 have been optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 41 and Figure 42 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to the Applications Report, *Feedback Plots Define Op Amp AC Performance* (SBOA015), available for download from the TI website, for details of analysis techniques and application circuits.

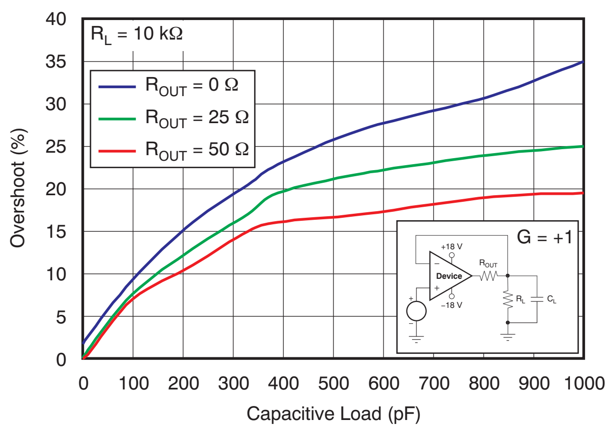


Figure 41. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

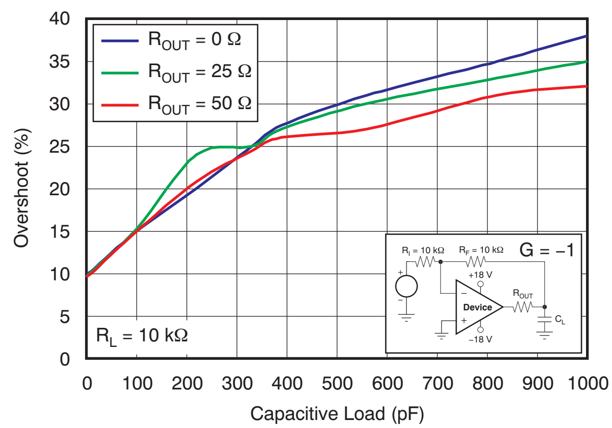


Figure 42. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings. Figure 43 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

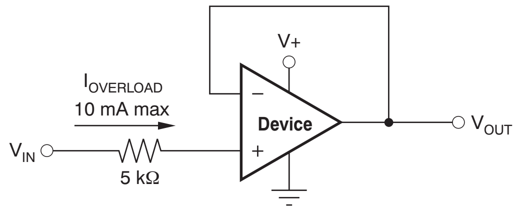


Figure 43. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

APPLICATION EXAMPLES

The application examples of Figure 44 and Figure 45 highlight only a few of the circuits where the OPAx188 family of devices can be used.

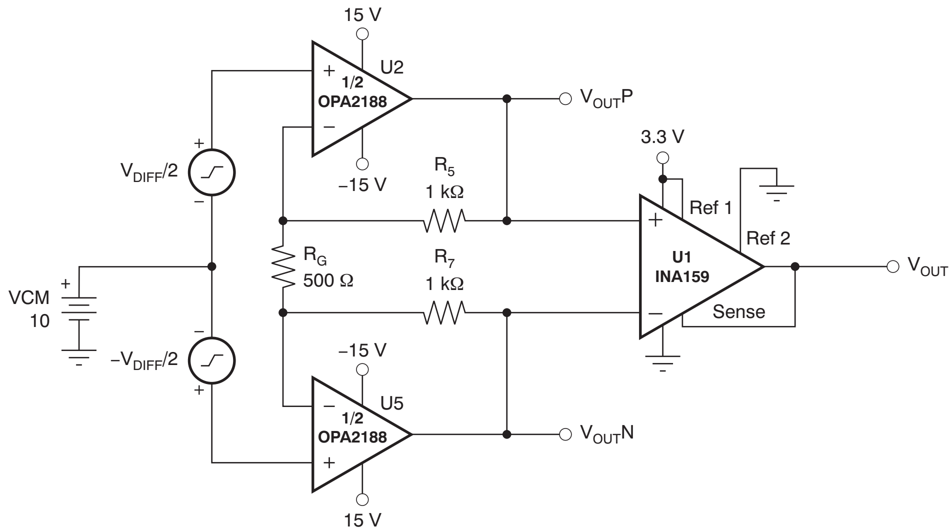
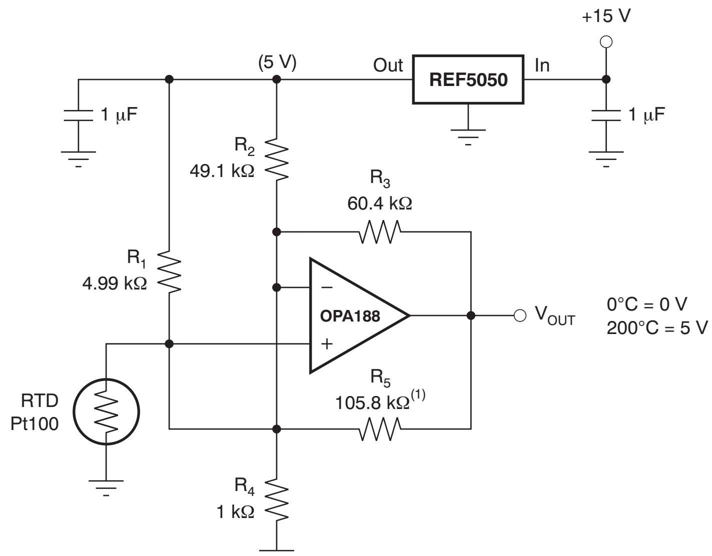


Figure 44. Discrete INA + Attenuation for ADC with 3.3-V Supply



(1) R_5 provides positive-varying excitation to linearize output.

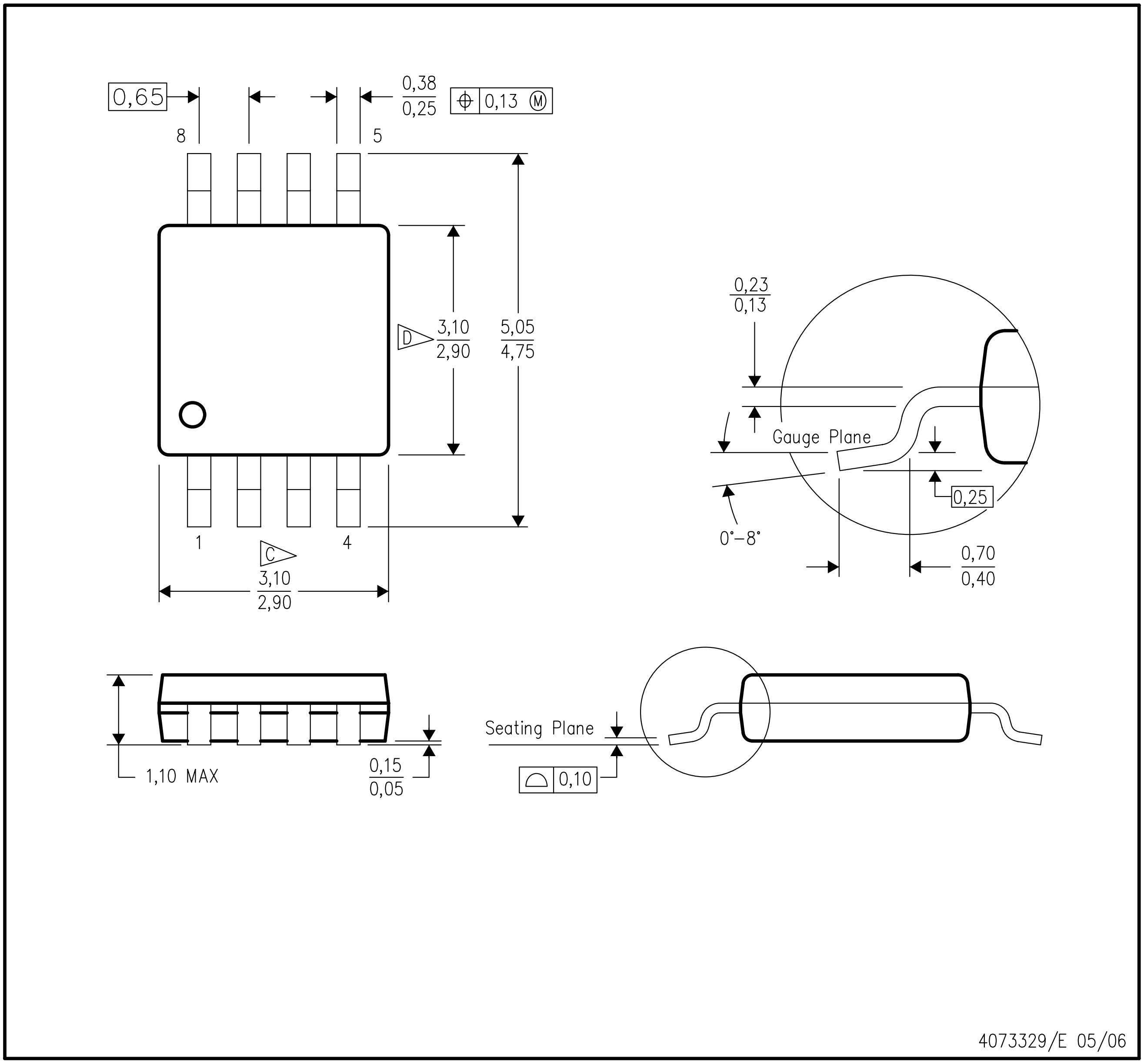
Figure 45. RTD Amplifier with Linearization

15-Aug-2011

PACKAGING INFORMATION

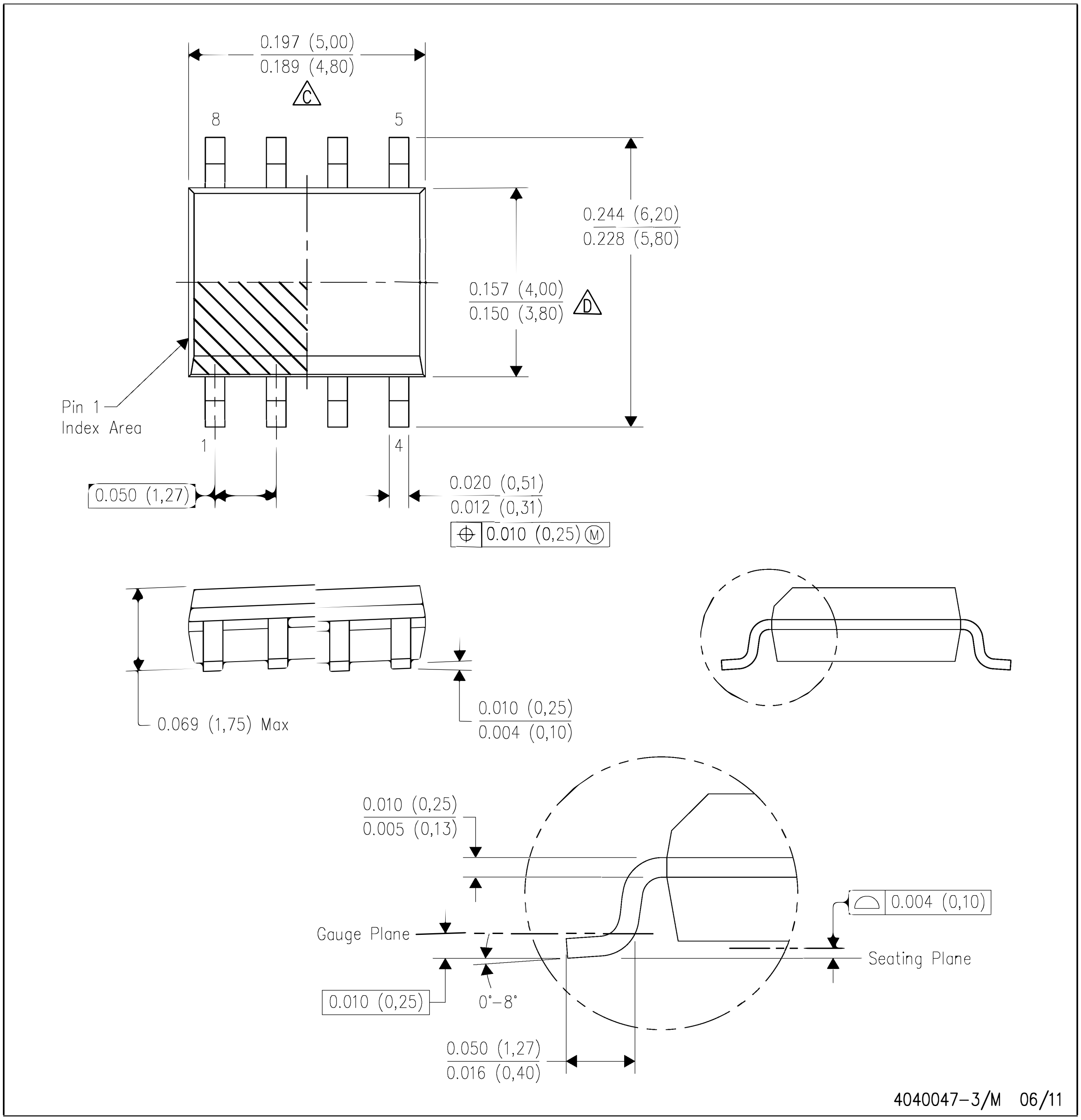
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
OPA2188AID	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	
OPA2188AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2188AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2188AIDR	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.