

# 1.5MHz, 1A, High Efficiency PWM Step-Down DC/DC Converter

## General Description

The RT8059 is a high efficiency Pulse Width Modulated (PWM) step-down DC/DC converter, capable of delivering 1A output current over a wide input voltage range from 2.8V to 5.5V. The RT8059 is ideally suited for portable electronic devices that are powered by 1-cell Li-ion battery or by other power sources within the range, such as cellular phones, PDAs and handy-terminals.

Internal synchronous rectifier with low  $R_{DS(ON)}$  dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical applications. The RT8059 automatically turns off the synchronous rectifier when the inductor current is low and enters discontinuous PWM mode. This can increase efficiency in light load condition.

The RT8059 enters low dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the upper P-MOSFET. The RT8059 enters shutdown mode and consumes less than 0.1 $\mu$ A when the EN pin is pulled low.

The switching ripple can be easily smoothed out by small package filtering elements due to a fixed operation frequency of 1.5MHz. This along with small TSOT-23-5 package provides small PCB area application. Other features include soft-start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection.

## Ordering Information

RT8059 □□

- Package Type  
J5 : TSOT-23-5
- Lead Plating System  
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

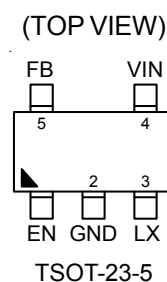
## Features

- Wide Input Voltage from 2.8V to 5.5V
- Adjustable Output from 0.6V to  $V_{IN}$
- 1A Output Current
- 95% Efficiency
- No Schottky Diode Required
- 1.5MHz Fixed Frequency PWM Operation
- Small TSOT-23-5 Package
- RoHS Compliant and Halogen Free

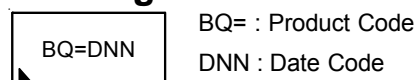
## Applications

- NIC Card
- Cellular Telephones
- Personal Information Appliances
- Wireless and DSL Modems
- MP3 Players
- Portable Instruments

## Pin Configurations



## Marking Information



# RT8059

## Typical Application Circuit

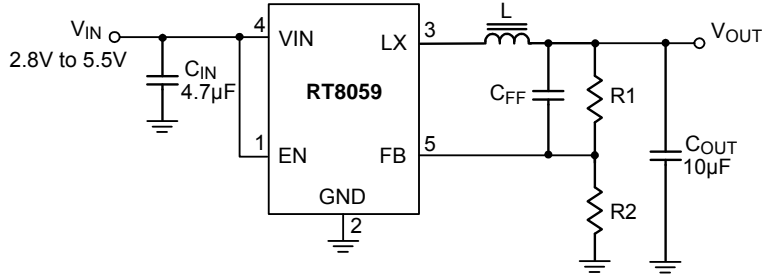


Table 1. Suggested Component Values

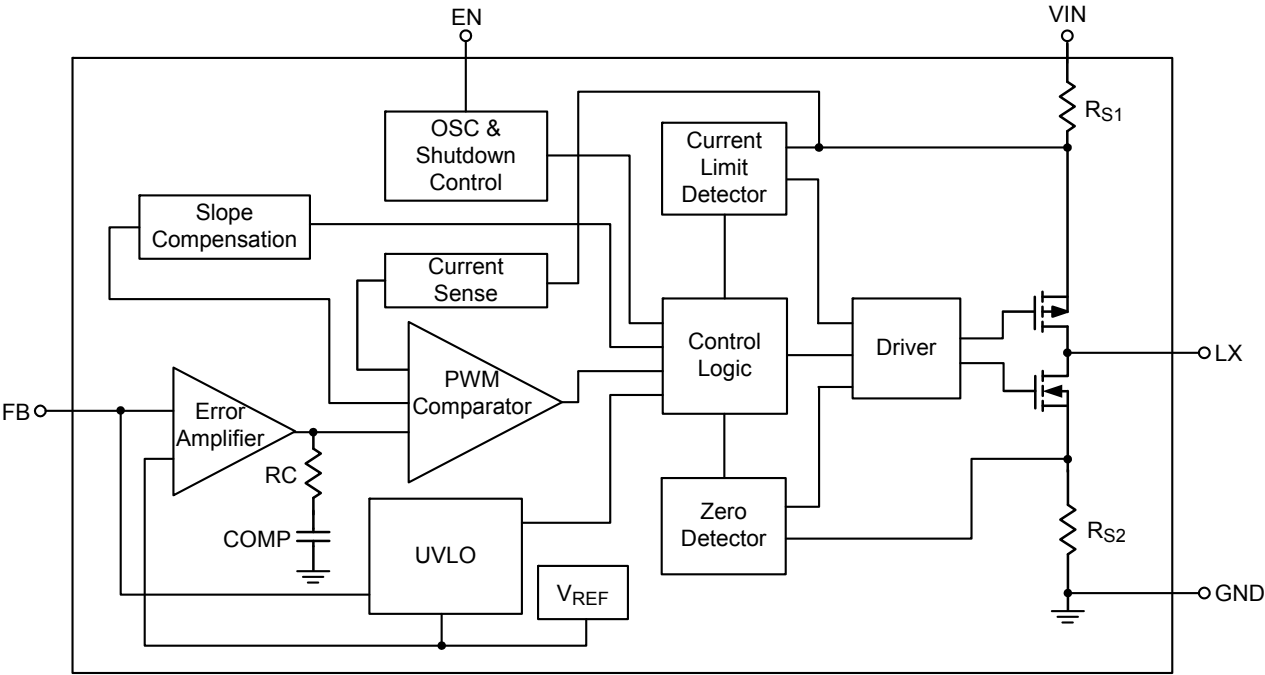
V <sub>OUT</sub> (V)	R1 (kΩ)	R2 (kΩ)	C <sub>FF</sub> (pF)	L (µH)	C <sub>OUT</sub> (µF) X5R 16V 0805
1	38.3	56.2	22 to 39	1.5	10
1.2	56	56	15 to 39	1.5	10
1.8	113	56.2	0 to 8.2	2.2	10
2.5	178	56	0 to 12	2.2	10
3.3	249	54.9	0 to 8.2	2.2	10

Note : All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC Bias.

## Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Chip Enable (Active High). Do not leave the EN pin floating.
2	GND	Ground.
3	LX	Switch Node.
4	VIN	Power Input.
5	FB	Feedback Input Pin.

Function Block Diagram



# RT8059

## Absolute Maximum Ratings (Note 1)

- VIN to GND ----- 6.5V
- LX to GND ----- -0.3V to (VIN + 0.3V)
- < 30ns ----- -5V to 7.5V
- EN, FB to GND ----- VIN + 0.6V
- Power Dissipation, PD @ TA = 25°C
- TSOT-23-5 ----- 0.392W
- Package Thermal Resistance (Note 2)
- TSOT-23-5, θJA ----- 255°C/W
- Junction Temperature Range ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
- HBM (Human Body Mode) ----- 2kV
- MM (Machine Mode) ----- 200V

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ----- 2.8V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

## Electrical Characteristics

(VIN = 3.6V, VOUT = 2.5V, L = 2.2μH, CIN = 4.7μF, COUT = 10μF, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current	I <sub>Q</sub>	I <sub>OUT</sub> = 0mA, V <sub>FB</sub> = V <sub>REF</sub> + 5%	--	78	--	μA
Shutdown Current	I <sub>SHDN</sub>	EN = GND	--	0.1	1	μA
Reference Voltage	V <sub>REF</sub>		0.588	0.6	0.612	V
Adjustable Output Range	V <sub>OUT</sub>	(Note 5)	V <sub>REF</sub>	--	V <sub>IN</sub> - 0.2	V
Adjustable Output Voltage Accuracy	ΔV <sub>OUT</sub>	V <sub>IN</sub> = V <sub>OUT</sub> + ΔV to 5.5V, 0A < I <sub>OUT</sub> < 1A, (Note 6)	-3	--	3	%
FB Input Current	I <sub>FB</sub>	V <sub>FB</sub> = V <sub>IN</sub>	-50	--	50	nA
P-MOSFET R <sub>ON</sub>	R <sub>DS(ON)_P</sub>	I <sub>OUT</sub> = 200mA	--	0.28	--	Ω
N-MOSFET R <sub>ON</sub>	R <sub>DS(ON)_N</sub>	I <sub>OUT</sub> = 200mA	--	0.25	--	
P-Channel Current Limit	I <sub>LM_P</sub>	V <sub>IN</sub> = 2.8V to 5.5V	--	1.5	--	A
EN Input Threshold Voltage	Logic-High	V <sub>IH</sub>	V <sub>IN</sub> = 2.8V to 5.5V	1.5	--	V
	Logic-Low	V <sub>IL</sub>	V <sub>IN</sub> = 2.8V to 5.5V	--	0.4	
Under Voltage Lockout Threshold	V <sub>UVLO</sub>		--	2.3	--	V
Under Voltage Lockout Hysteresis	ΔV <sub>UVLO</sub>		--	0.2	--	V
Oscillator Frequency	f <sub>OSC</sub>	I <sub>OUT</sub> = 100mA	1.2	1.5	1.8	MHz
Thermal Shutdown Temperature	T <sub>SD</sub>		--	150	--	°C
Max. Duty Cycle	D <sub>MAX</sub>		100	--	--	%

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.**  $\theta_{JA}$  is measured at  $T_A = 25^\circ\text{C}$  on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

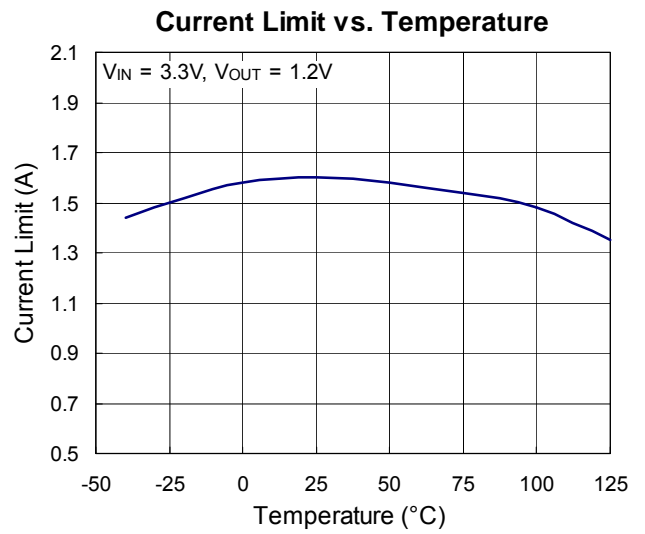
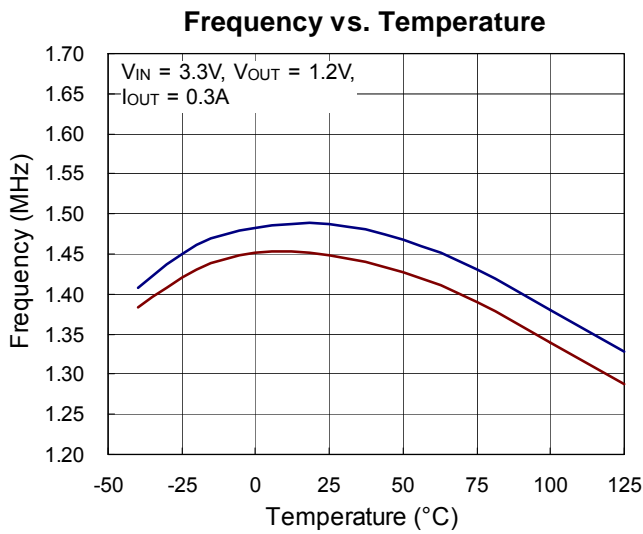
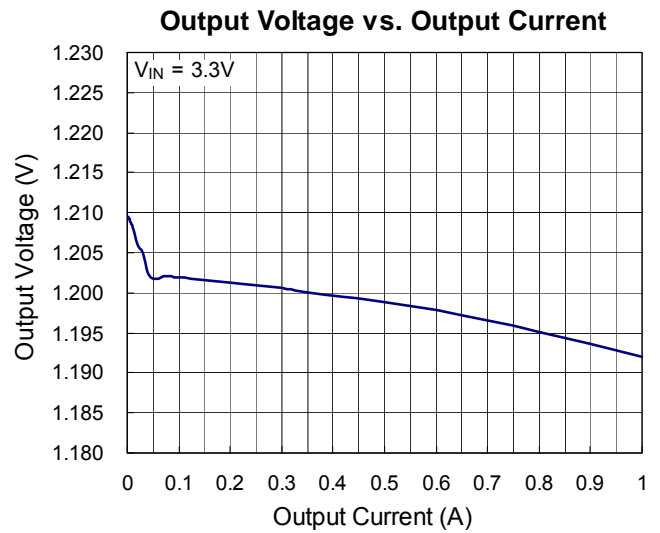
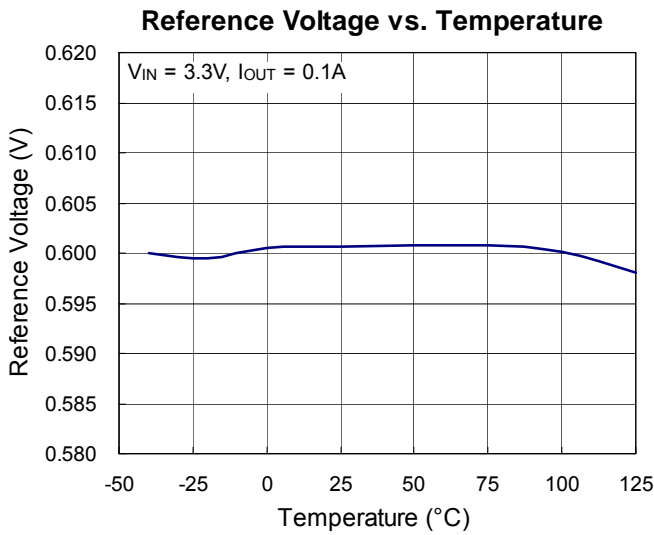
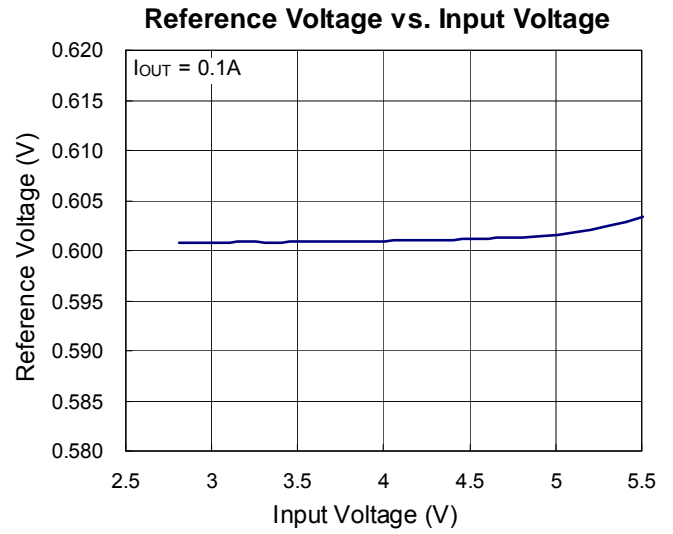
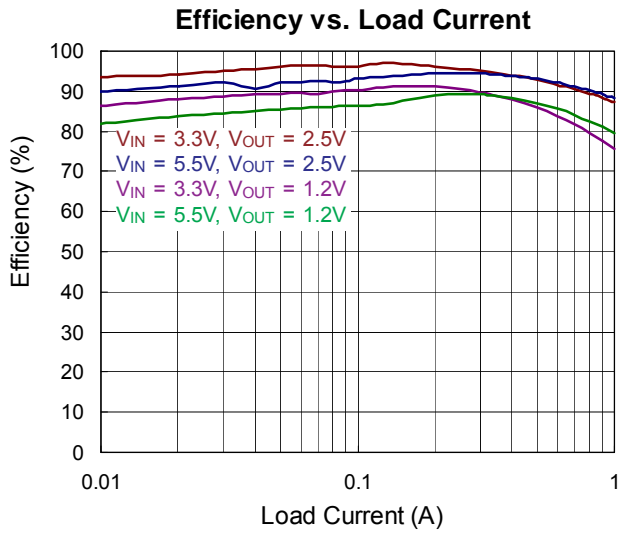
**Note 3.** Devices are ESD sensitive. Handling precaution recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

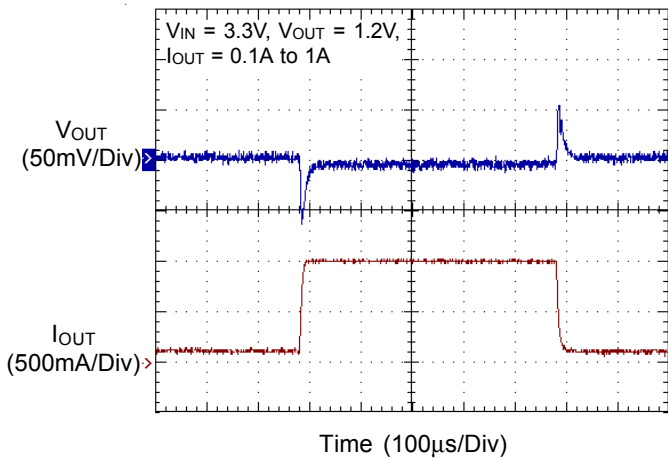
**Note 5.** Guaranteed by design.

**Note 6.**  $\Delta V = I_{OUT} \times R_{DS(ON)}$

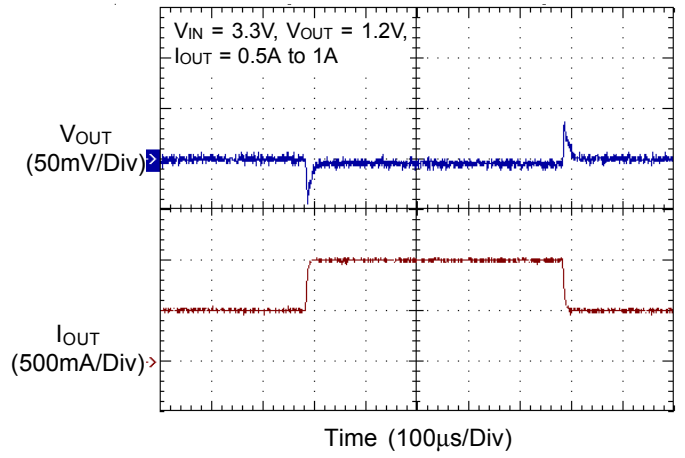
## Typical Operating Characteristics



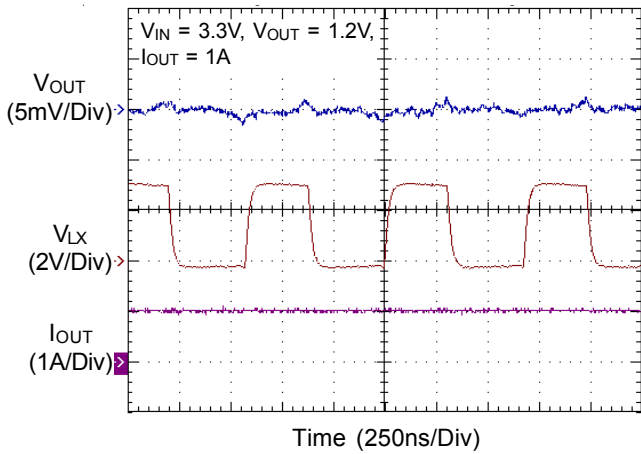
### Load Transient Response



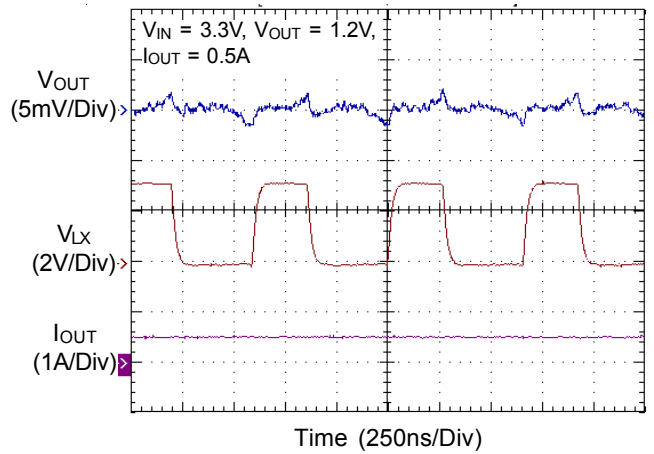
### Load Transient Response



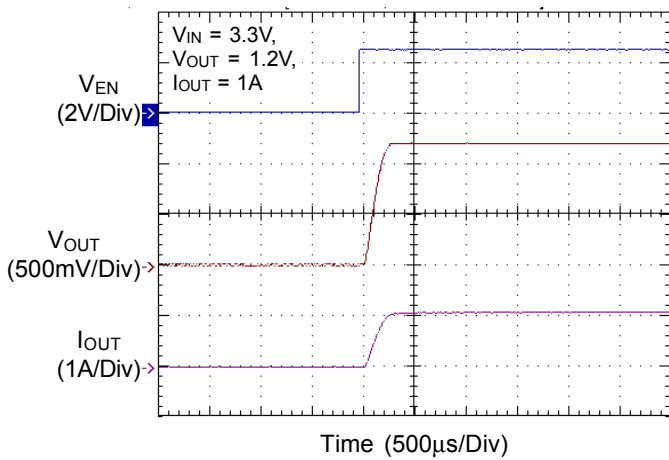
### Switching



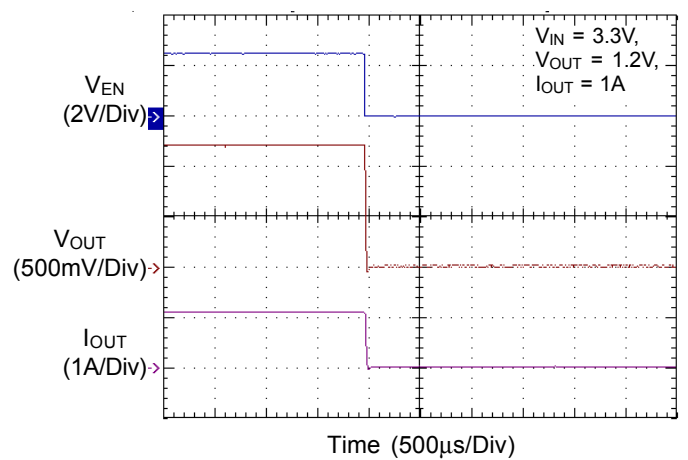
### Switching



### Power On from EN



### Power Off from EN



## Applications Information

The basic RT8059 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by  $C_{IN}$  and  $C_{OUT}$ .

### Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current  $\Delta I_L$  increases with higher  $V_{IN}$  and decreases with higher inductance.

$$\Delta I_L = \left[ \frac{V_{OUT}}{f \times L} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is  $\Delta I_L = 0.4(I_{MAX})$ . The largest ripple current occurs at the highest  $V_{IN}$ . To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[ \frac{V_{OUT}}{f \times \Delta I_L(MAX)} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

### Inductor Core Selection

Once the value for L is known, the type of inductor can be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore, results in higher copper losses.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design

current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements.

### $C_{IN}$ and $C_{OUT}$ Selection

The input capacitance,  $C_{IN}$ , is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not result in much difference. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of  $C_{OUT}$  is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple,  $\Delta V_{OUT}$ , is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ ESR + \frac{1}{8fC_{OUT}} \right]$$

where f is the switching frequency and  $\Delta I_L$  is the inductor ripple current.



The output ripple is highest at maximum input voltage since  $\Delta I_L$  increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

### Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input,  $V_{IN}$ . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at  $V_{IN}$  large enough to damage the part.

### Output Voltage Setting

The resistive voltage divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

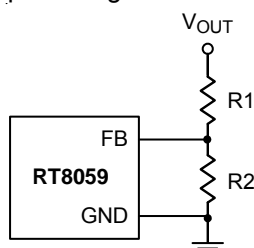


Figure 1. Setting Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF} \left(1 + \frac{R1}{R2}\right)$$

where  $V_{REF}$  is the internal reference voltage (0.6V typ.)

### Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs,  $V_{OUT}$  immediately shifts by an amount equal to  $\Delta I_{LOAD}$  (ESR), where ESR is the effective series resistance of  $C_{OUT}$ .  $\Delta I_{LOAD}$  also begins to charge or discharge  $C_{OUT}$  generating a feedback error signal used by the regulator to return  $V_{OUT}$  to its steady-state value. During this recovery time,  $V_{OUT}$  can be monitored for overshoot or ringing which would indicate a stability problem.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8059, the maximum junction temperature is 125°C and  $T_A$  is the ambient temperature. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For TSOT-23-5 packages, the thermal resistance,  $\theta_{JA}$ , is 255°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (255^\circ\text{C/W}) = 0.392\text{W for TSOT-23-5 package}$$

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The maximum power dissipation depends on the operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance,  $\theta_{JA}$ . For the RT8059 package, the derating curves in Figure 2 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

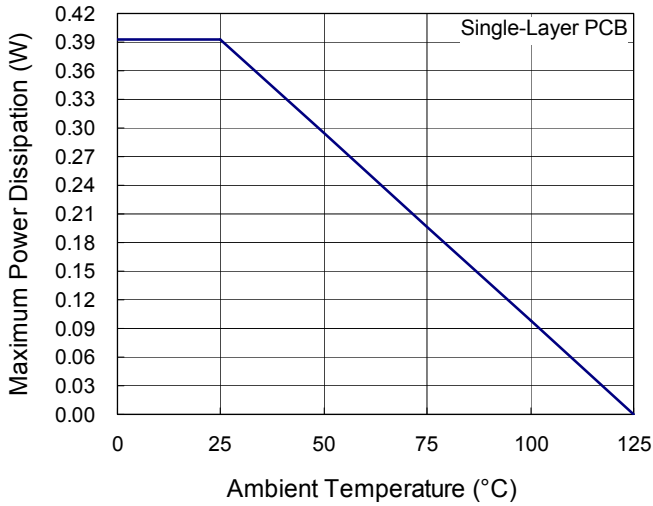


Figure 2. Derating Curves for RT8059 Package

## Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT8059.

- ▶ Keep the trace of the main current paths as short and wide as possible.
- ▶ Place the input capacitor as close as possible to the device pins (VIN and GND).
- ▶ LX node experiences high frequency voltage swings and should be kept in a small area. Keep analog components away from the LX node to prevent stray capacitive noise pick-up.
- ▶ Place the feedback components as close as possible to the FB pin.
- ▶ GND and Exposed Pad must be connected to a strong ground plane for heat sinking and noise protection.

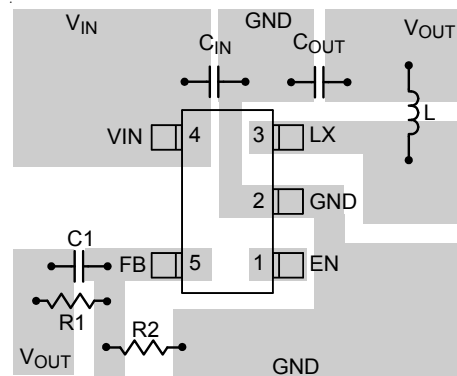
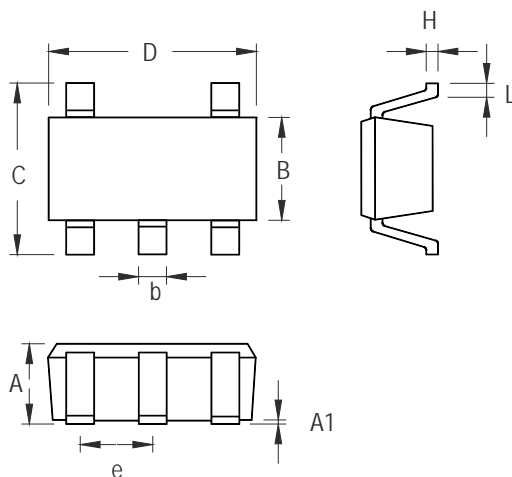


Figure 3. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024