2A, 18V, 500KHz, Synchronous Step-Down DC/DC Converter

FEATURES

- 4.75V to 18V input voltage
- Output adjustable from 0.923V to 15V
- Output current up to 2A
- Integrated 135mΩ/100mΩ power MOSFET switches
- Shutdown current 3μA typical
- Efficiency up to 95%
- Fixed frequency 500KHz
- Internal soft start
- Over current protection and Hiccup
- Over temperature protection
- RoHS Compliant and 100% Lead (Pb) Free

APPLICATIONS

- Distributed power systems
- Networking systems
- FPGA, DSP, ASIC power supplies
- Notebook computers
- Green electronics or appliance

ORDERING INFORMATION

PART	PACKAGE	RoHS	Ship, Quantity
ZTP7192S	SOP-8L	Yes	Tape and Reel, 3000

DESCRIPTION

The ZTP7192S is a high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve a 2A continuous output current over a wide input supply range, with excellent load and line regulation. The ZTP7192S has synchronous-mode operation for higher efficiency over the output current-load range.

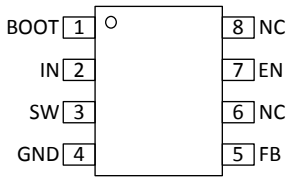
Current-mode operation provides fast transient response and eases loop stabilization.

Protection features include over-current protection and thermal shutdown.

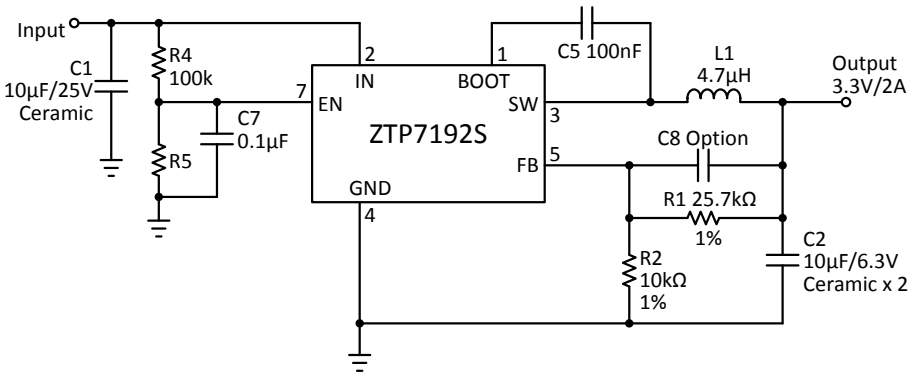
The ZTP7192S requires a minimal number of readily available, standard external components and is available in space-saving SOP-8L packages.

Pins Configuration

Top View
SOP-8L



Typical Application Circuit



Note: R5 and C7 are optional.

Details please see the DVT report.

Absolute Maximum Ratings

Supply Voltage V_{IN} ..... –0.3V to +20V
Switch Node V_{SW} ..... –0.3V to V_{IN}+0.3V
Boost V_{BOOT} ..... V_{SW}–0.3V to V_{SW}+6V
All Other Pins ..... –0.3V to +6V
Junction Temperature ..... +150°C
Lead Temperature ..... +260°C
Storage Temperature Range ..... –65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electro-Static Discharge Sensitivity

This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with proper precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

Recommended Operating Conditions

Supply Voltage V_{IN} ..... 4.75V to 18V
Output Voltage V_{OUT} ..... 0.923V to V_{IN}–3V
Operating Temperature Range ..... –40°C to +125°C

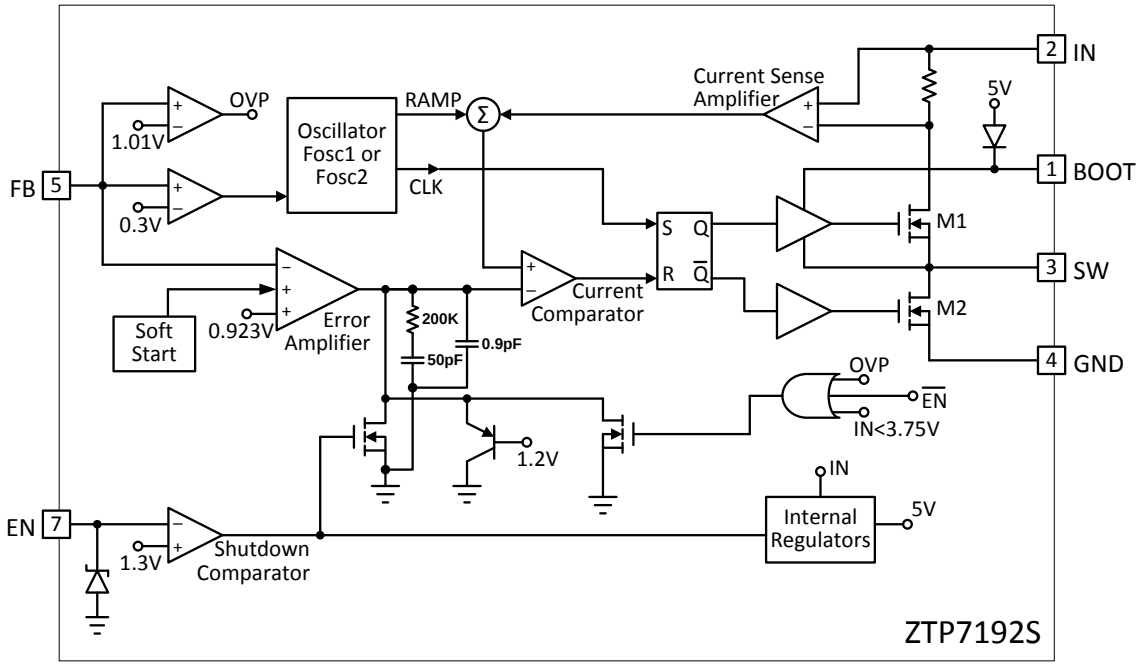
Package Thermal Characteristics

SOP-8L:
Thermal Resistance, θ_{JA} ..... 90°C/W
Thermal Resistance, θ_{JC} ..... 45°C/W

Pins Description

SOP-8L	Symbol	Description
1	BOOT	High-side gate drive boost input.
2	IN	Power input.
3	SW	Power switching output.
4	GND	Ground.
5	FB	Feedback input.
6	NC	Not connected.
7	EN	Enable input.
8	NC	Not connected.

Functional Block Diagram



Electrical Specifications

(T_A = +25°C, V_{IN} = +12V, unless otherwise noted.)

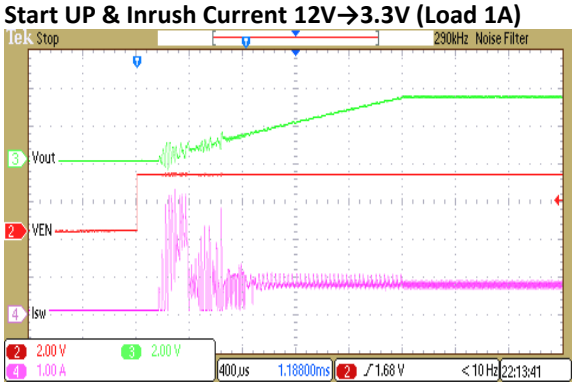
PARAMETER	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{IN}		4.75		18	V
Output Voltage	V_{OUT}		0.923		15	V
Shutdown Supply Current		V_{EN} = 0V		3	6	μA
Supply Current		V_{EN} = 2.0V, V_{FB} = 1V		7		mA
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 18V	0.900	0.923	0.946	V
Feedback Over-voltage Threshold				1.01		V
Error Amplifier Voltage Gain *	A_{EA}			1000		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_C = ±10μA		40		μA/V
High-Side Switch-On Resistance *	$R_{DS(ON)1}$			135		mΩ
Low-side Switch-On Resistance *	$R_{DS(ON)2}$			100		mΩ
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V, T_A = +125°C			10	μA
Upper Switch Current Limit		Minimum Duty Cycle	3	3.6		A
Lower Switch Current Limit		From Drain to Source		0		A
Oscillation Frequency	F_{OSC1}		400	500	600	KHz
Short Circuit Oscillation Frequency	F_{OSC2}	V_{FB} = 0V	100	125	150	KHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.5V		90		%
Minimum On Time *				100		ns
EN Falling Threshold Voltage		V_{EN} Falling		1.22		V
EN Rising Threshold Voltage		V_{EN} Rising		1.32		V
Input Under Voltage Lockout Threshold		V_{IN} Rising		3.75		V
Input Under Voltage Lockout Threshold Hysteresis				200		mV
Soft-Start Period				2		ms
Hiccup Period				8		ms
Thermal Shutdown *				150		°C

* Guaranteed by design, not tested.

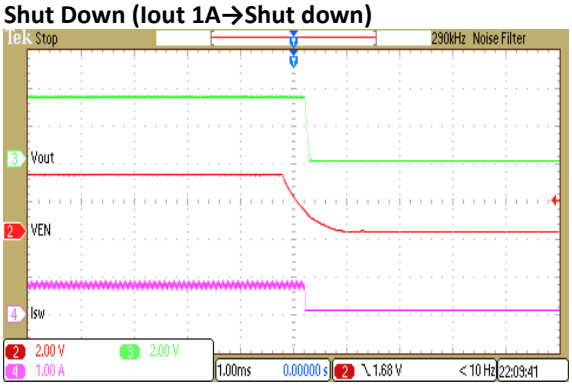
Typical Characteristics

V_{IN} = 12V, V_O = 3.3V, L1 = 4.7µH, C1 = 10µF, C2 = 10µF x 2, T_A = +25°C, unless otherwise noted.

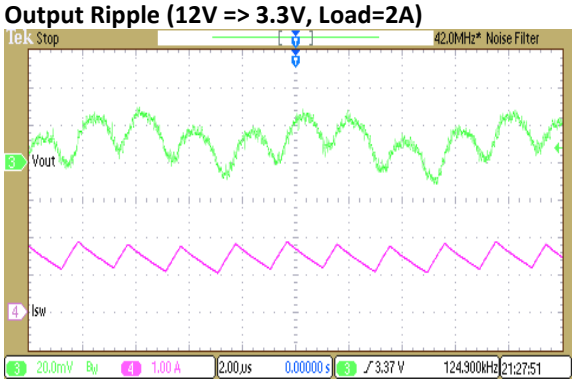
Start UP & Inrush Current 12V→3.3V (Load 1A)



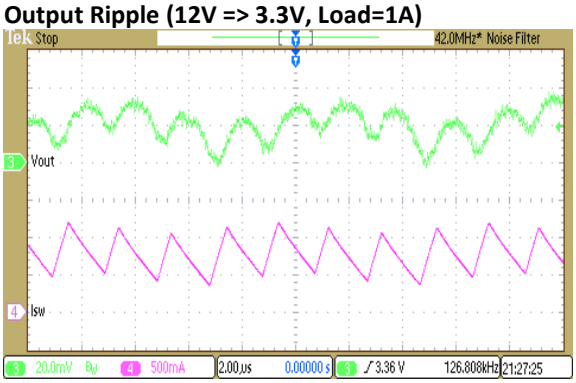
Shut Down (Iout 1A→Shut down)



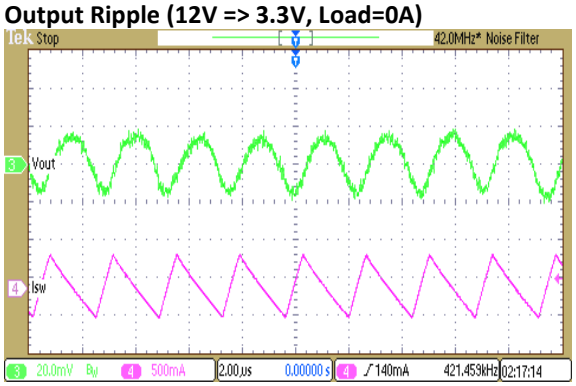
Output Ripple (12V => 3.3V, Load=2A)



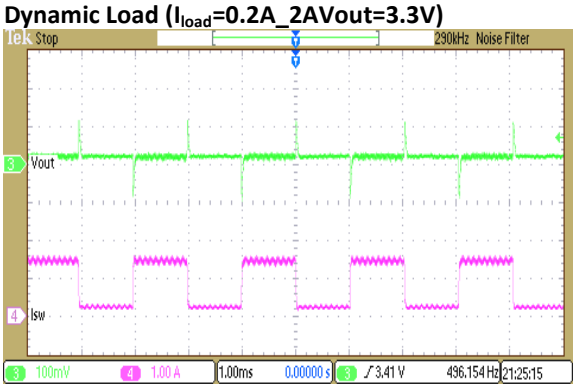
Output Ripple (12V => 3.3V, Load=1A)



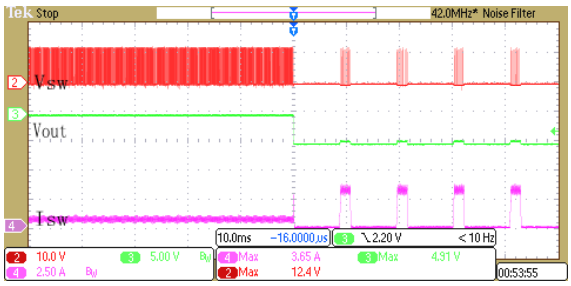
Output Ripple (12V => 3.3V, Load=0A)



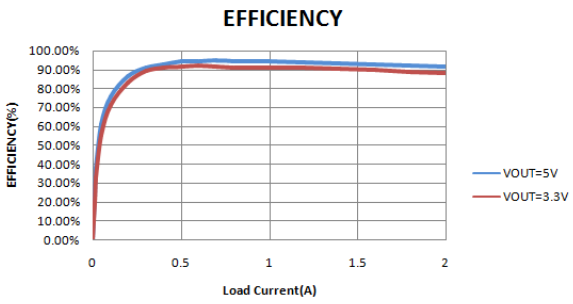
Dynamic Load (I_{load}=0.2A_2AVout=3.3V)



Short Circuit Protection



Efficiency



APPLICATION INFORMATION

Overview

The ZTP7192S is a synchronous rectified, current-mode, step-down regulator. It regulates input voltages from 4.75V to 18V down to an output voltage as low as 0.923V, and supplies up to 2A of load current.

The ZTP7192S uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BOOT is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the ZTP7192S FB pin exceeds 10% of the nominal regulation voltage of 0.923V, the over voltage comparator is tripped, forcing the high-side switch off.

Pins Description

BOOT: High-Side Gate Drive Boost Input. BOOT supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.1µF or greater capacitor from SW to BOOT to power the high side switch.

IN: Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 18V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC.

SW: Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BOOT to power the high-side switch.

GND: Ground.

FB: Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 0.923V.

EN: Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Pull up with 100kΩ resistor for automatic startup.

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \times R2 / (R1 + R2)$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Thus the output voltage is:

$$V_{OUT} = 0.923 \times (R1 + R2) / R2$$

R2 can be as high as 100kΩ, but a typical value is 10kΩ.

Using the typical value for R2, R1 is determined by:

$$R1 = 10.83 \times (V_{OUT} - 0.923V) (K\Omega)$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = [V_{OUT} / (f_S \times \Delta I_L)] \times (1 - V_{OUT}/V_{IN})$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + [V_{OUT} / (2 \times f_S \times L)] \times (1 - V_{OUT}/V_{IN})$$

Where I_{LOAD} is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI requirements.

Optional Schottky Diode

During the transition between high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table 1 lists example Schottky diodes and their Manufacturers.

Part Number	Voltage and Current Rating	
B130	30V, 1A	
SK13	30V, 1A	
MBRS130	30V, 1A	International Rectifier

Table 1: Diode selection guide.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times [(V_{OUT}/V_{IN}) \times (1 - V_{OUT}/V_{IN})]^{1/2}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{C1} = I_{LOAD}/2$. For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = [I_{LOAD}/(C1 \times f_S)] \times (V_{OUT}/V_{IN}) \times (1 - V_{OUT}/V_{IN})$$

Where C1 is the input capacitance value.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = [V_{OUT}/(f_S \times L)] \times (1 - V_{OUT}/V_{IN}) \times [R_{ESR} + 1 / (8 \times f_S \times C2)]$$

Where C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = [V_{OUT}/(8 \times f_S^2 \times L \times C2)] \times (1 - V_{OUT}/V_{IN})$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = [V_{OUT}/(f_S \times L)] \times (1 - V_{OUT}/V_{IN}) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The ZTP7192S can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BOOT diode are:

- V_{OUT} = 5V or 3.3V; and
- Duty cycle is high: $D = V_{OUT}/V_{IN} > 65\%$

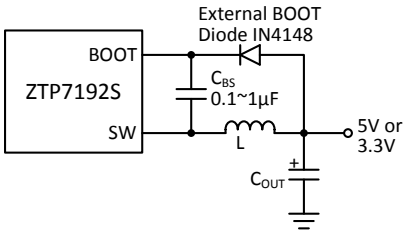


Figure 1: Add optional external bootstrap diode to enhance efficiency.

In these cases, an external BOOT diode is recommended

from the output of the voltage regulator to BOOT pin, as shown in Figure 1.

The recommended external BOOT diode is IN4148, and the BOOT capacitor is 0.1 ~ 1μF.

When V_{IN} ≤ 6V, for the purpose of promote the efficiency, it can add an external Schottky diode between IN and BOOT pins, as shown in Figure 2.

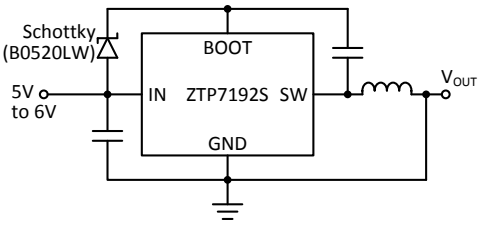


Figure 2: Add a Schottky diode to promote efficiency when V_{IN} ≤ 6V.

PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow the guidelines below.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the V_{IN} Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Rout SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

BOM of ZTP7192S

Please refer to the Typical Application Circuit.

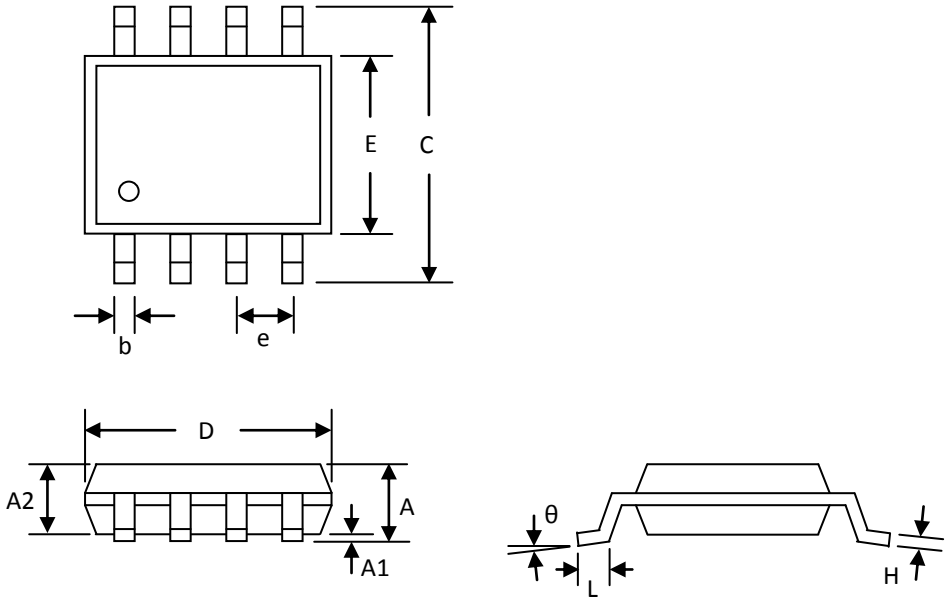
Item	Reference	Part
1	C1	10μF
2	C5	100nF
3	C7	0.1μF
4	R4	100K

Table 2: BOM selection table I.

	L1	R1	R2	C2	C8
Vout = 5.0V	6.8μH	44.2K	10K	10μF×2	100pF
Vout = 3.3V	4.7μH	25.7K	10K	10μF×2	100pF
Vout = 2.5V	4.7μH	17.1K	10K	10μF×2	50pF
Vout = 1.8V	3.3μH	9.50K	10K	10μF×2	50pF
Vout = 1.2V	2.2μH	3.00K	10K	10μF×2	20pF
Vout = 1.0V	2.2μH	0.834K	10K	10μF×2	20pF

Table 3: BOM selection table II.

PACKAGE DIMENSIONS SOP-8L



SYMBOLS	DIMENSION (MM)		DIMENSION (INCH)	
	MIN	MAX	MIN	MAX
A	1.300	1.752	0.051	0.069
A1	0.000	0.203	0.000	0.008
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	5.790	6.200	0.228	0.244
D	4.700	5.110	0.185	0.201
E	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
H	0.170	0.254	0.007	0.010
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°