General Description

The MXD8546F is a CMOS, Silicon-On-Insulator (SOI) double-pole, double-throw (DPDT) switch. The switch provides high linearity performance, low insertion loss and high isolation.

Switching is controlled by one control voltage, V1. Depending on the logic voltage level applied to this pin, the RF1 and RF2 pins connect to one of the two other RF port pins (RF3 or RF4) through a low insertion loss path, while maintaining a high isolation path to the alternate port. No external DC blocking capacitors are required on the RF path as long as no DC voltage is applied externally.

The MXD8546F DPDT switch is provided in a compact Quad Flat No-Lead (QFN) 2 x 2 mm package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Applications

- Simultaneous voice and LTE systems
- Diversity antenna switching

Features

- Single control voltage input
- Broadband frequency range: 0.4 to 3.8 GHz
- Low insertion loss: 0.45 dB @ 2.7 GHz
- P0.1dB of 38dBm
- No DC blocking capacitors required
- Positive control voltage range: 1.8 to 3.3 V
- Small, QFN (12-pin, 2 x 2 mm) package

Functional Block Diagram and Pin Function

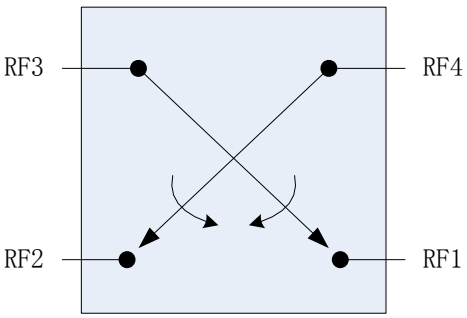


Figure 1. Functional Block Diagram

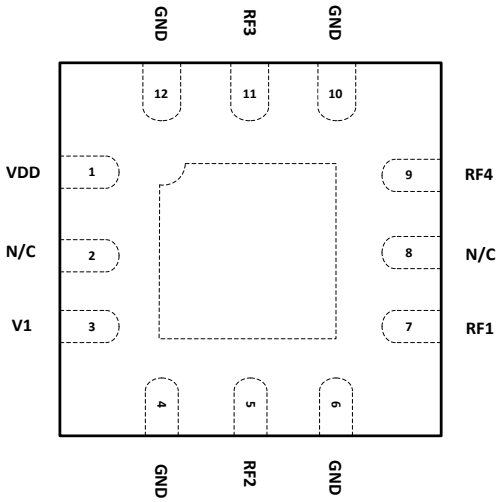


Figure 2. Pin Diagram

Application Circuit

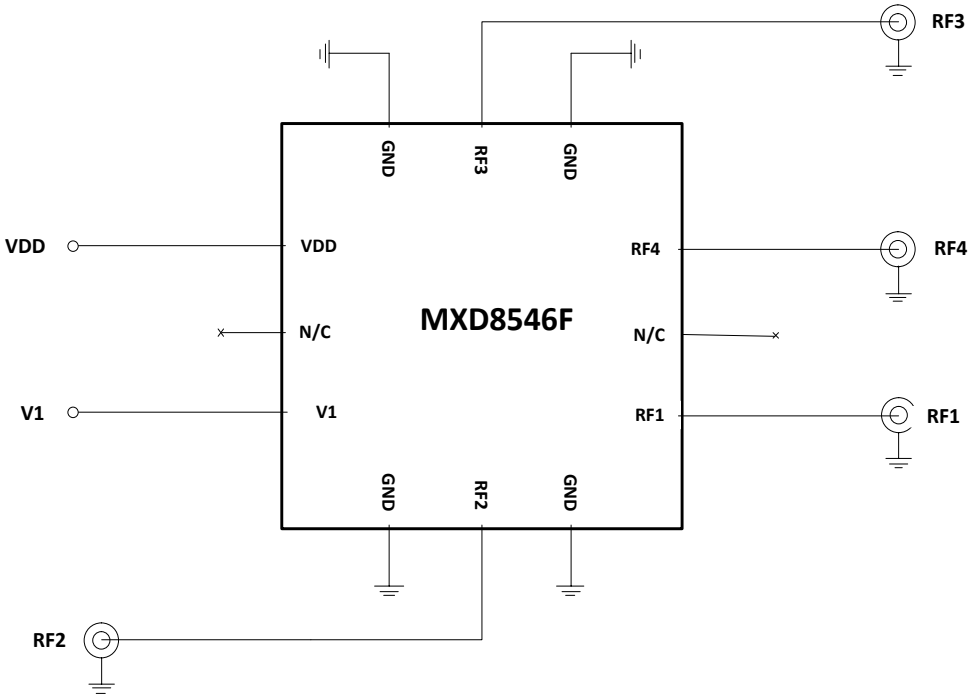


Figure 3. MXD8546F Application Circuit

Table 1. Pin Description

Pin No.	Name	Description	Pin No.	Name	Description
1	VDD	DC power supply	7	RF1	RF port 1
2	N/C	No connection	8	N/C	No connection
3	V1	DC control voltage 1.	9	RF4	RF Port 4
4	GND	Ground.	10	GND	Ground.
5	RF2	RF port 2	11	RF3	RF port 3
6	GND	Ground.	12	GND	Ground.

Note: Bottom ground paddles must be connected to ground.

Truth Table

Table 2.

V1	State
1	RF3 to RF1,RF4 to RF2
0	RF3 to RF2, RF4 to RF1

Note: “1” = 1.8 to 3.1 V,“0” = –0.20 to +0.45 V;
Any state other than described in this Table places the switch into an undefined state.

Recommended Operation Range

Table 3.

Parameters	Symbol	Min	Typ	Max	Units
Operation Frequency	f1	0.4	-	3.8	GHz
Power supply	V_{DD}	1.8	2.8	3.3	V
Switch Control Voltage High	V_{CTL_H}	1.0	1.8	3.3	V
Switch Control Voltage Low	V_{CTL_L}	0	0	0.3	V

Specifications

Table 4. Electrical Specifications

Parameter	Symbol	Specification			Units	Test Condition
		Min.	Typical	Max.		
DC Specifications						
Control voltage: Low High	 V_{CTL_L} V_{CTL_H}	 0 1.0	 0 1.8	 0.3 3.3	 V V	
Supply voltage	V_{DD}	1.8	2.8	3.3	V	
Supply current	I_{DD}		60	85		V_{DD} = 2.8 V
Control current	I_{CTL}		1	5	μA	V_{CTL}= 1.8 V
RF Specifications						
Insertion loss (RF1/RF2 to RF3/RF4)	IL		0.33 0.40 0.45 0.55		dB dB dB dB	0.7 to 1.0 GHz 1.0 to 2.2 GHz 2.5 to 2.7 GHz 3.4 to 3.8 GHz
Isolation (RF1/RF2 to RF3/RF4, RF1 to RF2, RF3 to RF4)	ISO	28 24 21 16	31 26 23 18		dB dB dB dB	0.7 to 1.0 GHz 1.0 to 2.2 GHz 2.5 to 2.7 GHz 3.4 to 3.8 GHz
Input return loss (RF1/RF2 to RF3/RF4)	RL	15	20		dB	0.7 to 3.8 GHz
0.1 dB Compression Point (RF1/RF2 to RF3/RF4)	$P_{0.1dB}$		+38		dBm	0.7 to 3.8 GHz
2nd Harmonic (RF1/RF2 to RF3/RF4)	2fo		-100	-83	dBc	fo = 824 to 915 MHz, P_{IN} = +35 dBm
3rd Harmonic(RF1/RF2 to RF3/RF4)	3fo		-95	-83	dBc	
Switching on time			2	5	μs	50% VCTL to 90% RF
Switching off time			2	5	μs	50% VCTL to 10% RF
Startup time			10		μs	Power off state to any RF switch state

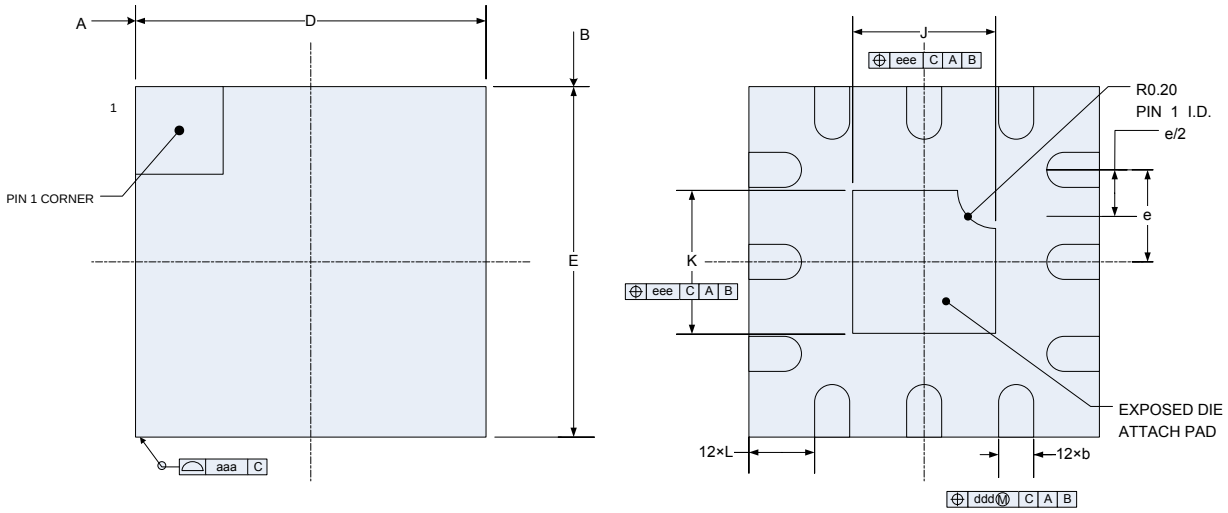
Absolute Maximum Ratings

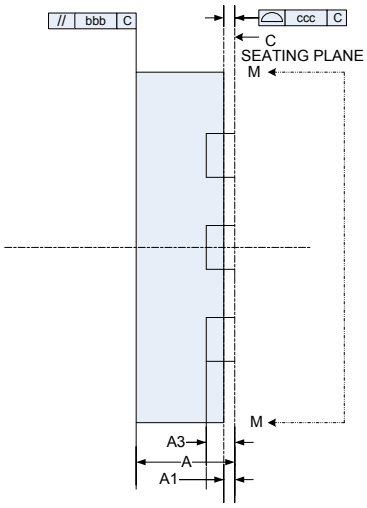
Table 5. Maximum ratings

Parameters	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}	+1.8	+3.3	V
Digital control voltage	V_{CTL}	0	+3.3	V
RF input power	P_{IN}		+39	dBm
Operating temperature	T_{OP}	–30	+85	℃
Storage temperature	T_{STG}	–55	+150	℃
Electrostatic Discharge Human body model (HBM), Class 2 Machine Model (MM), Class B Charged device model (CDM), Class III	 ESD_HBM ESD_MM ESD_CDM		 2000 200 500	 V

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device

Package Outline Dimension





DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTALTHICKNESS		A	0.51	0.55	0.60
STAND OFF		A1	00. 0	0.02	0.05
L/F THICKNESS		A3	-	0.15 Ref	-
EAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D	-	2.00 BSC	-
	Y	E	-	2.00 BSC	-
LEAD PITCH		e	0.50 BSC		
EP SIZE	X	J	0.77	0.92	1.02
	Y	K	0.77	0.92	1.02
LEAD LENGTH		L	0.19	0.29	0.39
PACKAGE EDGE TOLERANCE		aaa	0.05		
MOLD FLATNESS		bbb	0.10		
COPLANARITY		ccc	0.10		
LEAD OFFSET		ddd	0.05		
EXPOSED PAD OFFSET		eee	0.08		

Figure 4. package outline dimension

Reflow Chart

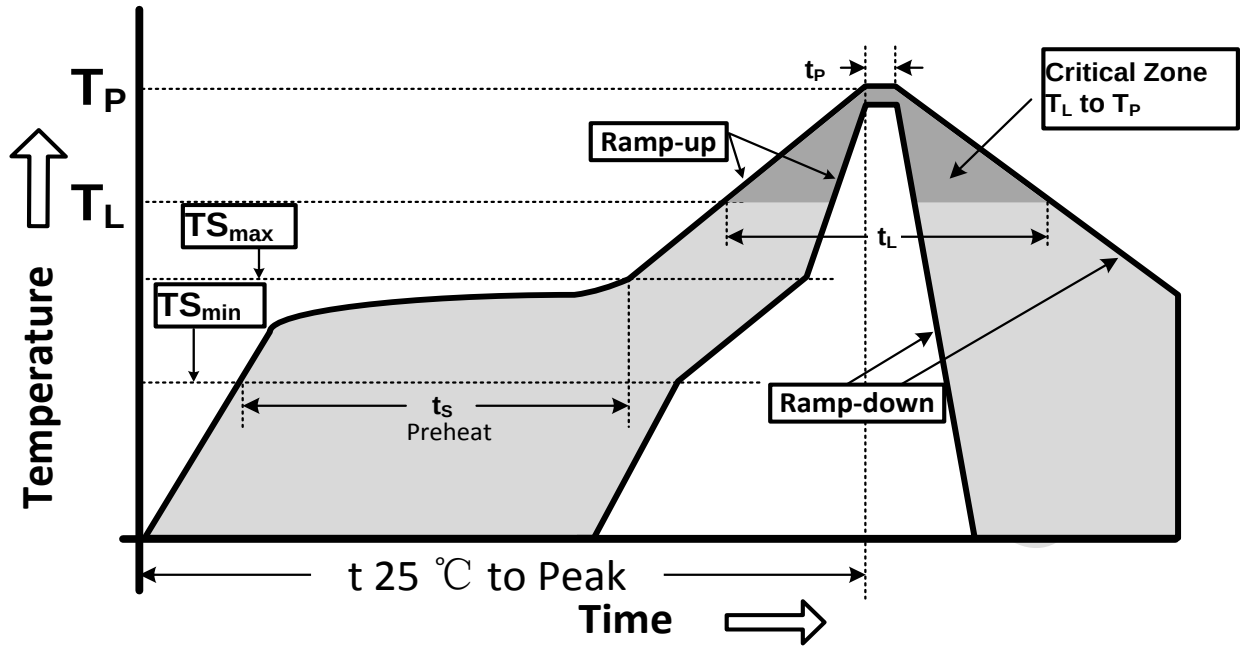


Figure 5. Recommended Lead-Free Reflow Profile

Table 6 Reflow condition

Profile Parameter	Lead-Free Assembly, Convection, IR/Convection
Ramp-up rate（TS_{max} to T_p）	3℃/second max.
Preheat temperature（TS_{min} to TS_{max}）	150℃ to 200℃
Preheat time（t_s）	60 - 180 seconds
Time above TL , 217℃（t_L）	60 - 150 seconds
Peak temperature（T_p）	260℃
Time within 5℃ of peak temperature(t_p)	20 - 40 seconds
Ramp-down rate	6℃/second max.
Time 25℃ to peak temperature	8 minutes max.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be used when handling these devices.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.