SGM2054
Sink and Source DDR Termination Regulator

GENERAL DESCRIPTION

The SGM2054 device is a sink and source double data rate (DDR) termination regulator. It is specifically designed for low-cost and low-external component count systems.

The SGM2054 provides fast transient response and only requires a minimum 20μF output capacitance. The SGM2054 supports remote sensing functions and all features required to power the DDR2, DDR3, DDR3L, Low-Power DDR3, DDR4 and DDR5 VTT bus termination. In addition, the SGM2054 provides an open-drain PGOOD to monitor the output regulation. EN signal that can be used to discharge VO when EN less than 0.3V.

The SGM2054 is available in a Green TDFN-3×3-10L package. It operates over an operating temperature range of -40℃ to +125℃.

APPLICATIONS

Memory Termination Regulator for DDR2, DDR3, DDR3L, Low-Power DDR3, DDR4 and DDR5
Notebooks, Desktops and Servers
Telecom and Datacom
Base Stations
LCD-TVs and PDP-TVs
Copiers and Printers
Set-Top Boxes

FEATURES

- **Input Voltage: Supports 2.5V Rail and 3.3V Rail**
- **VLDOIN Voltage Range: 1.1V to 3.5V**
- **Requires Minimum Output Capacitance of 20μF (Typically 3 × 10μF MLCCs) for Memory Termination Applications (DDR)**
- **PGOOD to Monitor Output Regulation**
- **EN Input**
- **REFIN Input Allows for Flexible Input Tracking either Directly or through Resistor Divider**
- **Remote Sensing (VOSNS)**
- **±10mA Buffered Reference (REFOUT)**
- **Built-in Soft-Start, UVLO and OCL**
- **Thermal Shutdown**
- **Supports DDR2, DDR3, DDR3L, Low-Power DDR3, DDR4 and DDR5 VTT Applications**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TDFN-3×3-10L Package**

TYPICAL APPLICATION

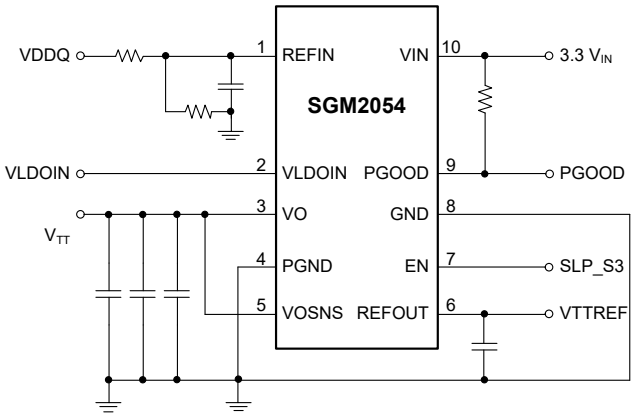


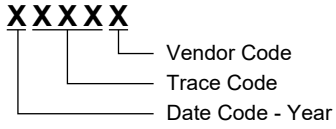
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2054	TDFN-3×3-10L	-40℃ to +125℃	SGM2054XTD10G/TR	SGM 2054D XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

REFIN, VIN, VLDOIN, VOSNS ..... -0.3V to 3.6V
EN to GND ..... -0.3V to 3.6V
PGND to GND ..... -0.3V to 0.3V
REFOUT ..... -0.3V to (V_{REFOUT} + 0.3V)
VO ..... -0.3V to (V_{LDOIN} + 0.3V)
PGOOD ..... -0.3V to 3.6V
Package Thermal Resistance
TDFN-3×3-10L, θ_{JA} ..... 56℃/W
TDFN-3×3-10L, θ_{JB} ..... 26℃/W
TDFN-3×3-10L, $\theta_{JC(TOP)}$ ..... 59℃/W
TDFN-3×3-10L, $\theta_{JC(BOT)}$ ..... 10℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.375V to 3.5V
EN, VLDOIN, VOSNS ..... -0.1V to 3.5V
REFIN ..... 0.5V to 1.8V
PGOOD, VO ..... -0.1V to 3.5V
REFOUT ..... -0.1V to 1.8V
PGND ..... -0.1V to 0.1V
Input Capacitance, C_{IN} ..... 15μF (MIN)
Output Capacitance, C_{OUT} ..... 10μF to 100μF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

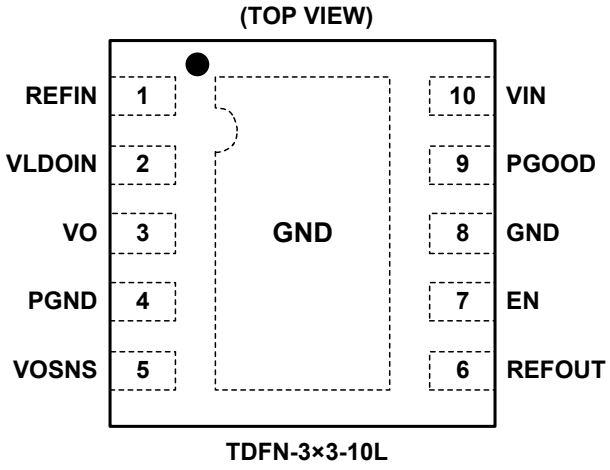
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	REFIN	I	Reference Input.
2	VLDOIN	I	Supply Voltage for the LDO.
3	VO	O	Power Output for the LDO.
4	PGND	G	Power Ground for the LDO.
5	VOSNS	I	Voltage Sense Input for the LDO. Connect to positive terminal of the output capacitor or the load.
6	REFOUT	O	Reference Output. Connect to GND through a 0.1μF ceramic capacitor.
7	EN	I	Enable Pin. Driving EN high to turn on the regulator. Driving EN low to turn off the regulator.
8	GND	G	Signal Ground.
9	PGOOD	O	Open-Drain, Power-Good Indicator.
10	VIN	I	2.5V or 3.3V Power Supply. A ceramic decoupling capacitor with a value between 1μF and 4.7μF is required.
Exposed Pad	GND	G	Exposed Pad. The exposed pad on the bottom of the package enhances thermal performance and is electrically connected to GND inside the package.

NOTE: I = Input, O = Output, G = Ground.

ELECTRICAL CHARACTERISTICS

(Typical values are at T_J = +25℃, V_{IN} = 3.3V, V_{LDOIN} = 1.8V, V_{REFIN} = 0.9V, V_{OSNS} = 0.9V, V_{EN} = V_{IN}, C_{OUT} = 3 × 10μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
Supply Current	I_{IN}	V_{EN} = 3.3V, no load		0.75		mA
Shutdown Current	I_{SHDN}	V_{EN} = 0V, V_{REFIN} = 0V, no load		50		μA
		V_{EN} = 0V, V_{REFIN} > 0.4V, no load		170		
Supply Current of VLDOIN	I_{LDOIN}	V_{EN} = 3.3V, no load		1		μA
Shutdown Current of VLDOIN	$I_{LDOIN(SHDN)}$	V_{EN} = 0V, no load		0.1		μA
Input Current						
Input Current of REFIN	I_{REFIN}	V_{EN} = 3.3V		0.01		μA
VO Output						
Output DC Voltage of VO	V_{OSNS}	V_{REFOUT} = 0.9V (DDR2), I_{OUT} = 0A		0.9		V
		V_{REFOUT} = 0.75V (DDR3), I_{OUT} = 0A		0.75		V
		V_{REFOUT} = 0.675V (DDR3L), I_{OUT} = 0A		0.675		V
		V_{REFOUT} = 0.6V (DDR4), I_{OUT} = 0A		0.6		V
		-2A < I_{OUT} < 2A		0.55		V
Output Voltage Tolerance to REFOUT	V_{OTOL}			±1		mV
VO Source Current Limit	I_{VOSRCL}	With reference to REFOUT, V_{OSNS} = 90% × V_{REFOUT}		4.6		A
VO Sink Current Limit	I_{VOSNCL}	With reference to REFOUT, V_{OSNS} = 110% × V_{REFOUT}		3.7		A
Discharge Resistance of VO	R_{DIS}	V_{REFIN} = 0V, V_{OUT} = 0.3V, V_{EN} = 0V		16		Ω
Power-Good Comparator						
VO PGOOD Threshold	$V_{TH(PG)}$	PGOOD window lower threshold with respect to REFOUT		-20		%
		PGOOD window upper threshold with respect to REFOUT		20		
		PGOOD hysteresis		2		
PGOOD Start-Up Delay	$t_{PGSTUPDLY}$	Start-up rising edge, VOSNS within 15% of REFOUT		2		ms
Output Low Voltage	$V_{PGOODLOW}$	I_{SINK} = 4mA		0.17		V
PGOOD Bad Delay	$t_{PBADDLY}$	VOSNS is outside of the ±20% PGOOD window		0.5		μs
Leakage Current	$I_{PGOODLKG}$	V_{OSNS} = V_{REFIN} (PGOOD high impedance), V_{PGOOD} = V_{IN} + 0.2V		0.001		μA
REFIN and REFOUT						
REFIN Voltage Range	V_{REFIN}	T_J = +25℃	0.5		1.8	V
REFIN Under Voltage Lockout	$V_{REFINUVLO}$	REFIN rising		380		mV
REFIN Under Voltage Lockout Hysteresis	$V_{REFINUVHYS}$			20		mV
REFOUT Voltage	V_{REFOUT}			REFIN		V
REFOUT Voltage Tolerance to V_{REFIN}	$V_{REFOUTTOL}$	-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 1.25V		1.25		V
		-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 0.9V		0.9		
		-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 0.75V		0.75		
		-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 0.675V		0.675		
		-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 0.6V		0.6		
		-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 0.55V		0.55		
REFOUT Source Current Limit	$I_{REFOUTSRCL}$	V_{REFOUT} = 0V		40		mA
REFOUT Sink Current Limit	$I_{REFOUTSNCL}$	V_{REFOUT} = V_{IN}		40		mA

ELECTRICAL CHARACTERISTICS (continued)

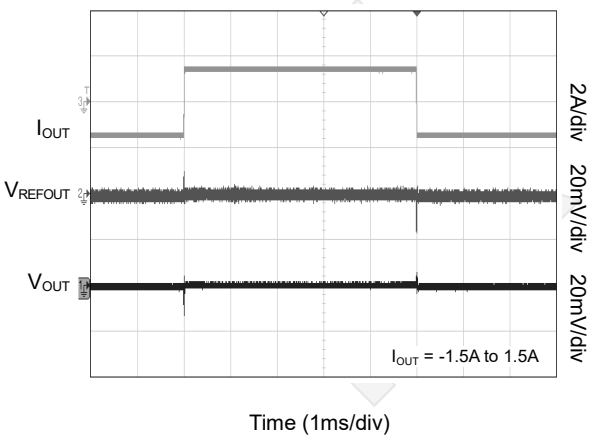
(Typical values are at T_J = +25℃, V_{IN} = 3.3V, V_{LDOIN} = 1.8V, V_{REFIN} = 0.9V, V_{OSNS} = 0.9V, V_{EN} = V_{IN}, C_{OUT} = 3 × 10μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO and EN Logic Threshold						
UVLO Threshold	V_{UVLO}	Wake up		2.2		V
		Hysteresis		35		mV
High-Level Input Voltage	V_{ENIH}	Enable, T_J = +25℃	1.7			V
Low-Level Input Voltage	V_{ENIL}	Enable, T_J = +25℃			0.3	
Hysteresis Voltage	V_{ENYST}	Enable		0.03		
Logic Input Leakage Current	I_{EN-LKG}	EN		0.01		μA
Start-Up Time	t_{STR}	C_{OUT} = 100μF, $V_{OUT(NOM)}$ = 0.6V, EN turns on to V_{OUT} = 90% × $V_{OUT(NOM)}$		27		μs
Thermal Shutdown						
Thermal Shutdown Temperature	T_{SHDN}			150		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}			20		

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{IN} = 3.3V, V_{LDOIN} = 1.2V, C_{LDOIN} = 20μF, C_{IN} = 4.7μF, C_{OUT} = 30μF, C_{REFOUT} = 1μF, unless otherwise noted.

Load Transient Response



DETAILED DESCRIPTION

Sink and Source Regulator (VO Pin)

The SGM2054 is an ultra-low dropout linear regulator specifically designed to provide termination voltage for DDR memory system with current capability up to 3A.

The SGM2054 builds in a high-side N-MOSFET which provides current sourcing and a low-side N-MOSFET which provides current sinking. The SGM2054 employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, connect a remote sensing terminal, VOSNS, should be connected to the positive terminal of each output capacitor as a separate trace from the high current path from VO.

Reference Input (REFIN Pin)

The output voltage, V_{OUT}, is regulated to track the reference voltage input REFIN. The SGM2054 device supports REFIN voltages from 0.5V to 1.8V, making it versatile and ideal for many types of low-power LDO applications. When REFIN is configured for standard DDR termination applications, REFIN can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ).

Reference Output (REFOUT Pin)

REFOUT is independent of the EN pin state. The output voltage is tightly regulated to track the reference voltage applied at REFIN pin. REFOUT becomes active when REFIN voltage rises to 380mV and VIN is above the UVLO threshold. When REFOUT is lower than 360mV, it is disabled and subsequently discharges to GND through an internal 130Ω (TYP) MOSFET.

It is capable of supporting both a sourcing and sinking load of 10mA. When it is configured for DDR termination applications, REFOUT generates the DDR VTT reference voltage for the memory application.

Soft-Start Sequencing

The SGM2054 features a current clamp which implements the soft-start function of the VO pin. It limits inrush current for charging the output capacitors. The soft-start function is completely symmetrical and the over-current limit works for both directions. The soft-start function works not only from GND to the REFOUT voltage, but also from VLDOIN to the REFOUT voltage. When VO is outside of the power-good window, the current clamp level is one-half of the full over-current limit (OCL) level. When VO rises or falls within the PGOOD window, the current clamp level switches to the full OCL level.

Enable Control (EN Pin)

EN pin is used to enable/disable control of the chip. Pulling V_{EN} lower than 0.3V disables an internal discharge MOSFET of 16Ω R_{DIS} turns on to pull output voltage to ground. Pulling V_{EN} higher than 1.7V enables the output voltage. Ensure that the EN pin voltage remains lower than or equal to V_{IN} at all times.

Power-Good Function (PGOOD Pin)

The PGOOD is an open drain that asserts high with 2ms (TYP) delay time after the VO enters power-good window which is VO within +20% of REFOUT. When the VO is out of the PGOOD window, PGOOD de-asserts within 0.5μs (TYP). Because PGOOD is an open-drain output, a pull-up resistor with a value of 100kΩ (TYP), the resistor should be placed between PGOOD and a stable active supply voltage rail.

Current Protection (VO Pin)

The LDO has a constant over-current limit (OCL). Note that the OCL level reduces by one half when the output voltage is not within the power-good window. This reduction is a non-latch protection.

UVLO Protection (VIN Pin)

VIN under-voltage lockout (UVLO) protection works through monitoring VIN voltage. If the VIN voltage is lower than the UVLO threshold voltage, both VO and REFOUT regulators are powered off. This shutdown is a non-latch protection.

Thermal Shutdown

To guarantee safe operation, the SGM2054 provides on-chip thermal shutdown protection. When the chip junction temperature exceeds +150℃, the part will shut down. When the junction temperature falls back to +130℃, the device resumes normal operation. If the junction temperature exceeds the thermal shutdown threshold then the VO and VREFOUT regulators both shut off, discharged by the internal discharge MOSFETs. The shutdown is a non-latch protection.

DETAILED DESCRIPTION (continued)

Tracking Start-Up and Shutdown

The SGM2054 supports tracking start-up and shutdown function when the EN pin is connected directly to the system bus and not used to turn on or turn off the device. VO follows REFOUT once REFIN voltage is higher than 380mV when tracking start-up. REFIN follows the rise of VDDQ rail through a voltage divider. The typical soft-start time (t_{SS}) for the VDDQ rail is approximately 3ms, however it may vary depending on the system configuration. The soft-start time of the VO output no longer depends on the OCL setting, but it is a function of the soft-start time of the VDDQ rail. PGOOD is asserted 2ms after V_{OUT} is within ±20% of REFOUT. When tracking shutdown, the VO pin voltage falls following REFOUT until REFOUT reaches 360mV. When REFOUT falls below 360mV, the internal discharge MOSFETs turn on and quickly discharge both REFOUT and VO to GND. If VO is beyond the ±20% range of REFOUT, PGOOD will be de-asserted. Figure 2 shows the typical timing diagram of tracking start-up and shutdown in the application.

Low Input Voltage Applications

The SGM2054 can be used in the application which offers either a 2.5V rail or a 3.3V rail. The voltage tolerance for a 2.5V rail input is between -5% and 5% accuracy or better. If a 2.5V rail is used for VIN, it should be ensured that the voltage (both DC and transient) at the device pin is 2.2V or greater.

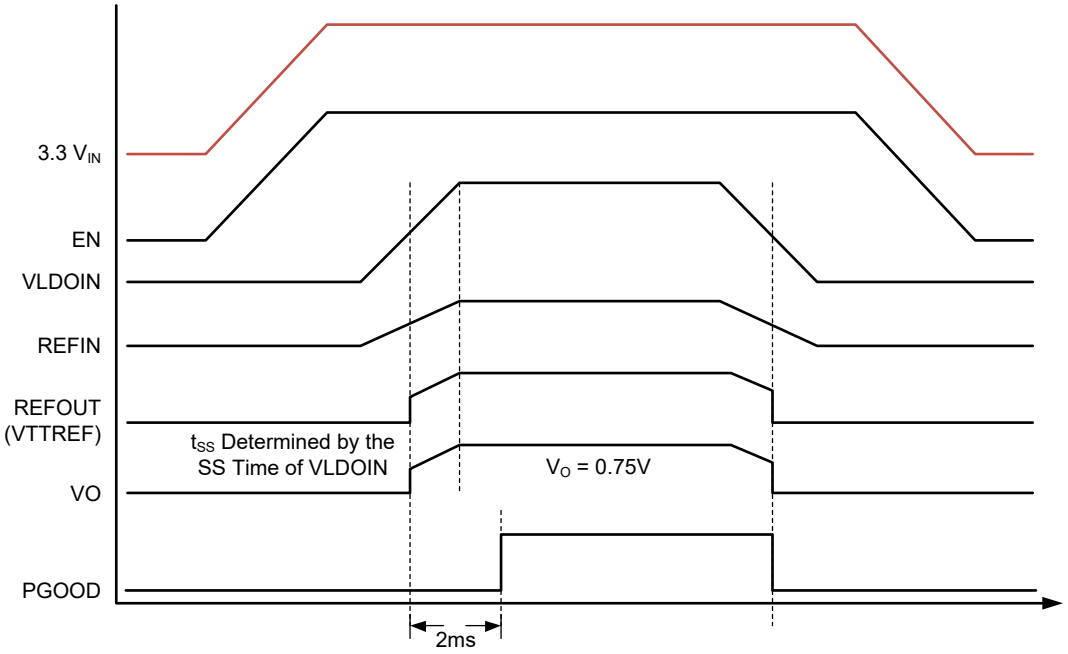
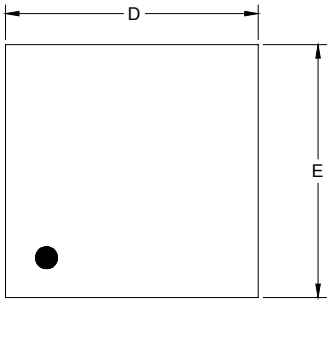


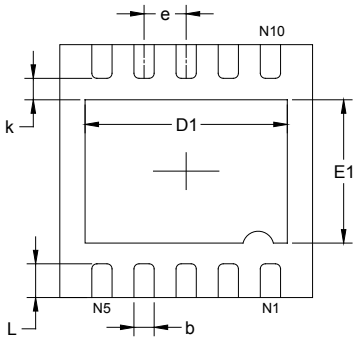
Figure 2. Typical Timing Diagram of Tracking Start-Up and Shutdown

PACKAGE OUTLINE DIMENSIONS

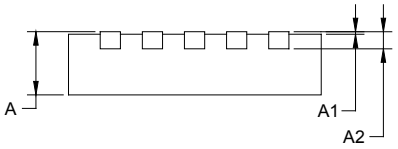
TDFN-3×3-10L



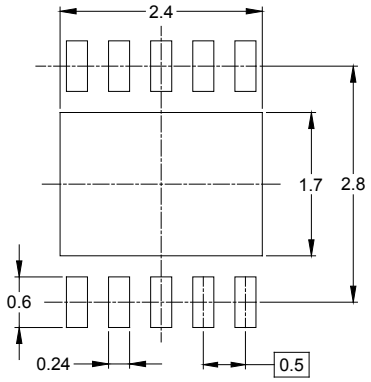
TOP VIEW



BOTTOM VIEW



SIDE VIEW

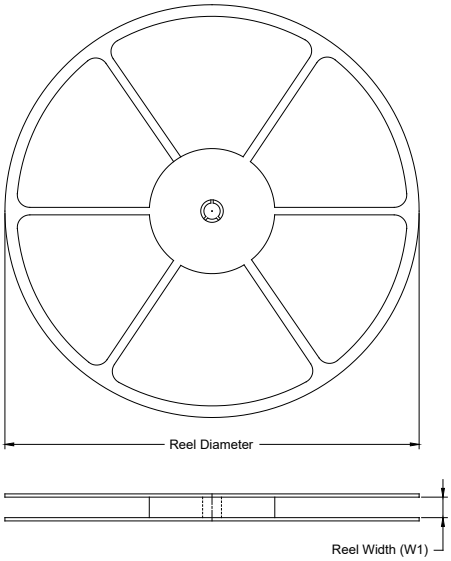


RECOMMENDED LAND PATTERN (Unit: mm)

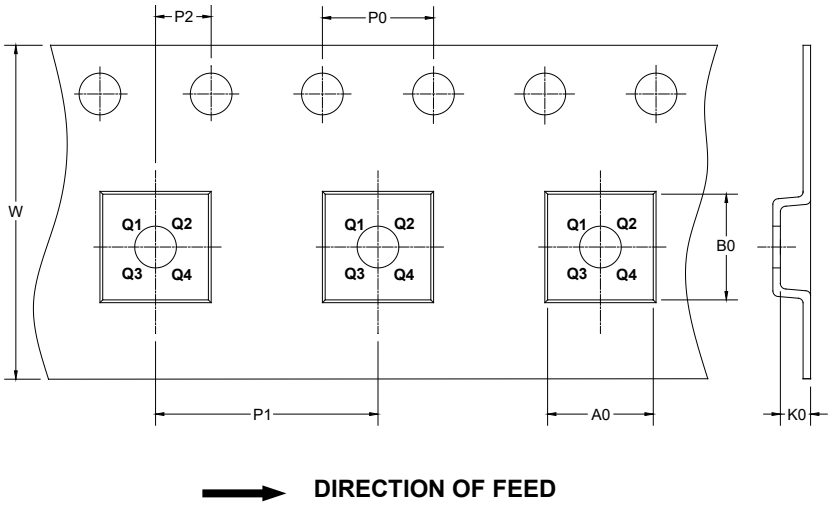
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



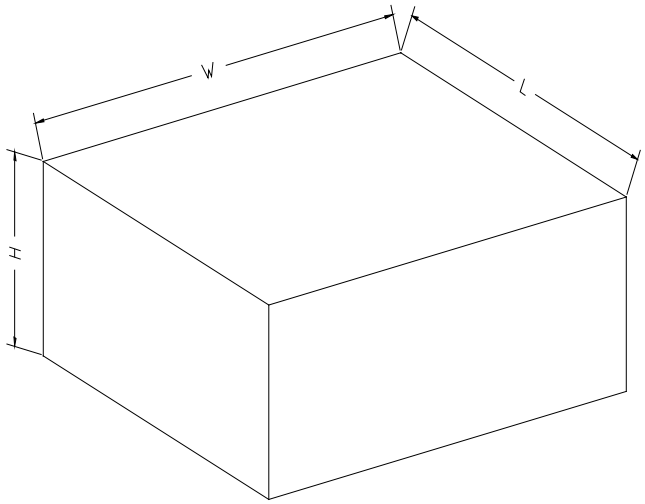
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-10L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002