3.8V-40V Vin, 3.5A, High Efficiency Synchronous Step-down DCDC Converter with Internal Compensation

FEATURES

- Wide Input Range: 3.8V-40V
- Up to 3.5A Continuous Output Current
- 0.8V ±1% Feedback Reference Voltage
- Integrated 80mΩ High-Side and 50mΩ Low-Side Power MOSFETs
- Pulse Skipping Mode PSM with 25uA Quiescent Current in Sleep Mode
- Fixed Frequency 570kHz
- 100ns Minimum On-time
- 2ms Internal Soft-start Time
- Frequency Spread Spectrum FSS Modulation for EMI Reduction
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Low Dropout Mode Operation
- Derivable Inverting Voltage Regulator
- Over-voltage and Over Temperature Protection
- Available in an ESOP-8 Package

APPLICATIONS

- Battery Pack Powered System - Cordless Power Tools, Cordless Home Appliance, Drone, Aero Modeling, GPS Tracker etc.
- Cigarette Lighter Adapters, Chargers
- LCD Display
- USB Type-C Power Delivery, USB Charging
- Industrial and Medical Distributed Power Supplies
- Optical Communication and Networking System
- Automotive System

DESCRIPTION

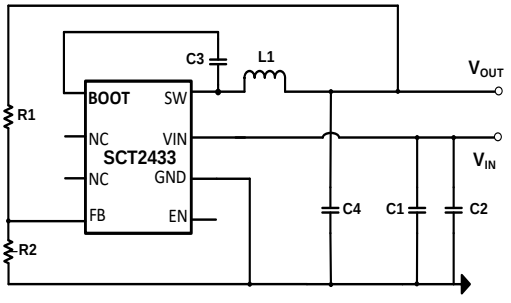
The SCT2433 is 3.5A synchronous buck converters with wide input voltage, ranging from 3.8V to 40V, which integrates an 80mΩ high-side MOSFET and a 50mΩ low-side MOSFET. The SCT2431, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 25uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

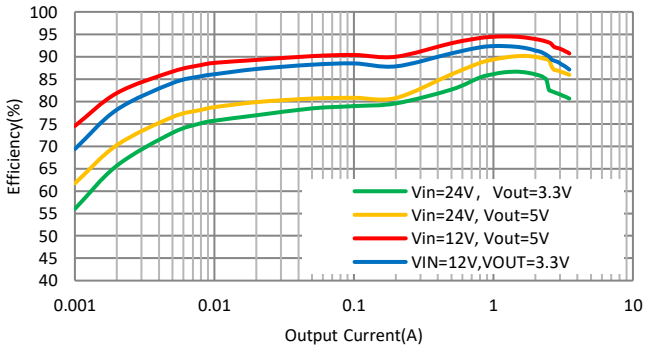
The SCT2433 features internal soft start with 570kHz switching frequency. The converter allows power conversion from high input voltage to low output voltage with a minimum 100ns on-time of high-side MOSFET. It also supports Low Drop-Out LDO operation at low voltage difference from input to output condition.

The SCT2433 is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2433 features Frequency Spread Spectrum FSS with ±6% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT2433 offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin thermally enhanced SOP-8 package.

TYPICAL APPLICATION





REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Market

Revision 1.1: Updated Description

Revision 1.2: Updated Figure 5 Description

Revision 1.3: Updated Figure 15. SCT2433 Design Example

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT2433STE	2433	8-Lead Plastic ESOP

1) For Tape & Reel, Add Suffix R (e.g. SCT2433STER)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	42	V
BOOT	-0.3	46	V
SW	-0.3	42	V
BOOT-SW	-0.3	6	V
FB	-0.3	6	V
Operating junction temperature TJ(2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION

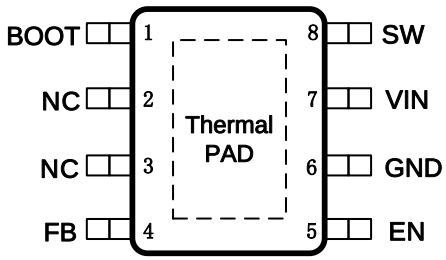


Figure 1. 8-Lead Plastic E-SOP

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
BOOT	1	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
NC	2	NC
NC	3	NC
FB	4	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
EN	5	Enable pin to regulator with internal pull-up current source. Pull below 1.1V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
GND	6	Ground

VIN	7	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	40	V
V_{OUT}	Output voltage range	0.8	40	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	SOP-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	42	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	45.8	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2433 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2433. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.8		40	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising		3.5		V
	Hysteresis			400		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		1		μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		25		μA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		80		mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			50		mΩ

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Reference and Control Loop						
V_{REF}	Reference voltage of FB			0.8		V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		4.25	5	5.75	A
I_{LIM_LSSRC}	Low-side power MOSFET souring current limit threshold			5.5		A
T_{HIC_W}	Over current protection hiccup wait time			512		cycles
T_{HIC_R}	Over current protection hiccup restart time			8192		cycles
Enable and Soft Startup						
V_{EN_H}	Enable high threshold			1.18		V
V_{EN_L}	Enable low threshold			1.1		V
I_{EN_L}	Enable pin pull-up current	EN=1V		1.5		μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		5.5		uA
T_{ss}	Internal soft start time			2		ms
Switching Frequency and External Clock Synchronization						
F_{SW}	Switching frequency		510	570	630	kHz
F_{JITTER}	Frequency spread spectrum in percentage of Fsw			±6		%
t_{ON_MIN}	Minimum on-time	V_{IN}=24V		100		ns
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising V_{FB}/V_{REF} falling		110 105		% %
V_{BOOTUV}	BOOT-SW UVLO threshold	BOOT-SW falling Hysteresis		2.36 300		V mV
T_{SD}	Thermal shutdown threshold	T_J rising Hysteresis		170 25		°C °C

TYPICAL CHARACTERISTICS

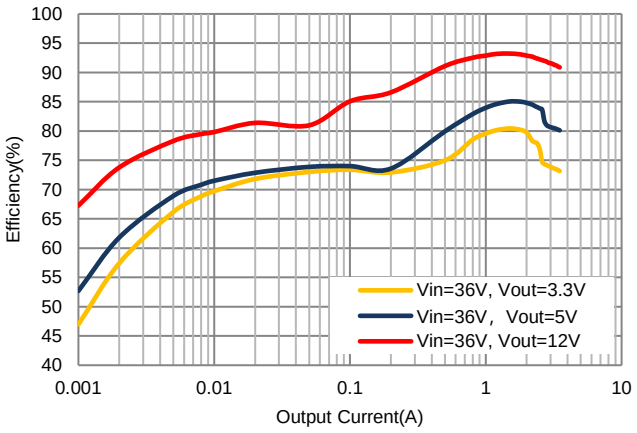


Figure 2. Efficiency vs Load Current, Vin=36V

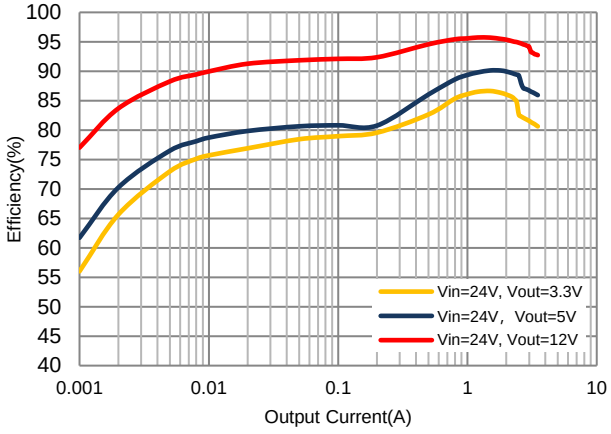


Figure 3. Efficiency vs Load Current, Vin=24V

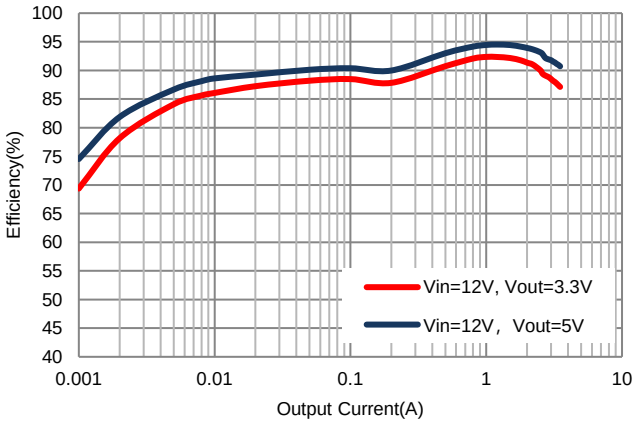


Figure 4. Efficiency vs Load Current, Vin=12V

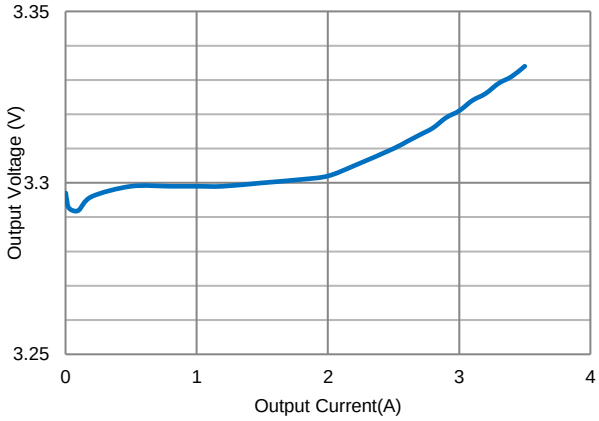


Figure 5. Load Regulation (Vin =12V, Vout=3.3V)

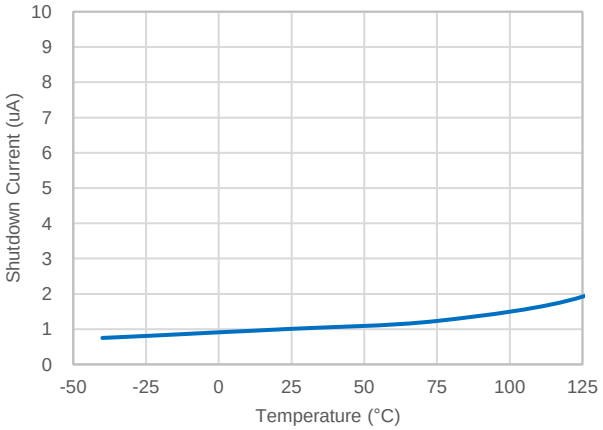


Figure 6. Shutdown Current vs Temperature

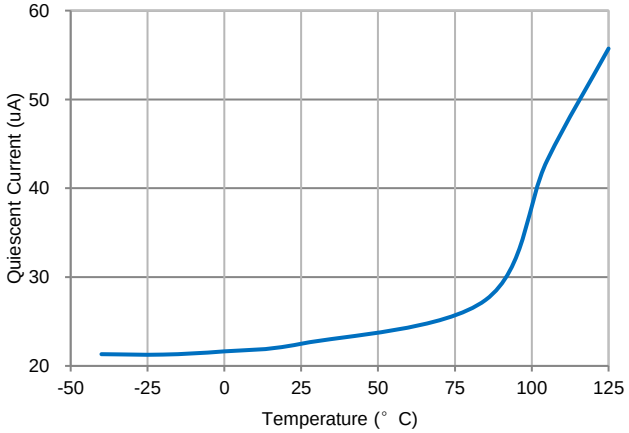


Figure 7. Quiescent Current vs Temperature

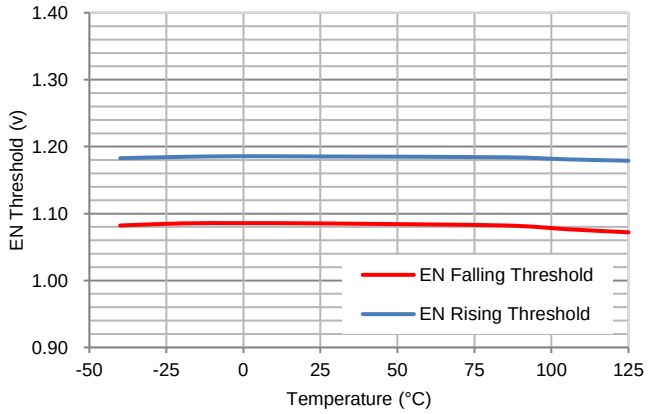


Figure 8. EN Threshold vs Temperature

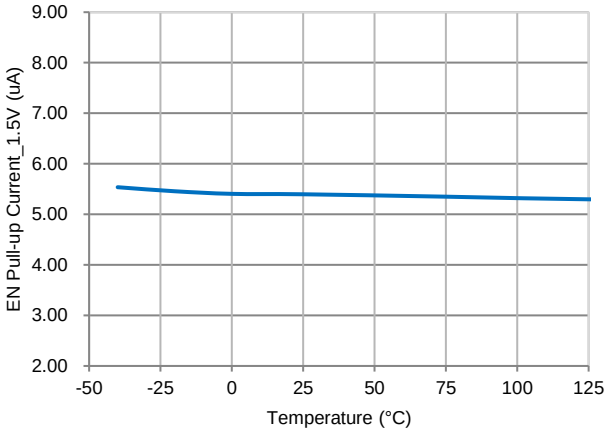


Figure 9. EN Pull-up Current vs Temperature

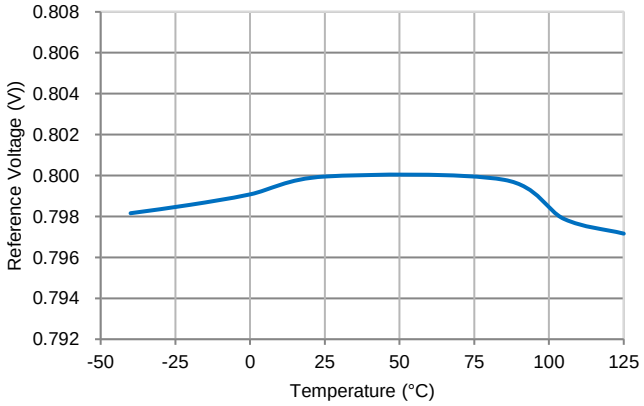


Figure 10. Reference Voltage vs Temperature

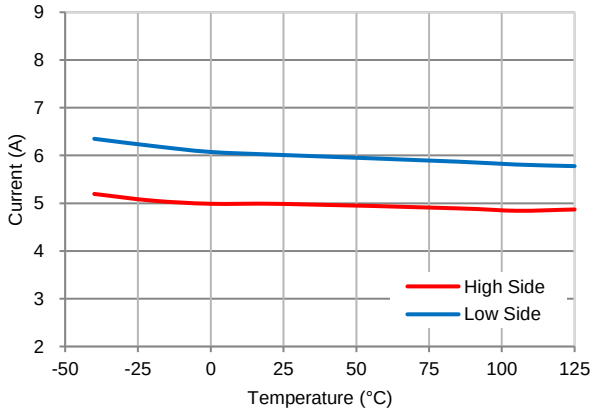


Figure 11. Peak Current Limit vs Temperature

FUNCTIONAL BLOCK DIAGRAM

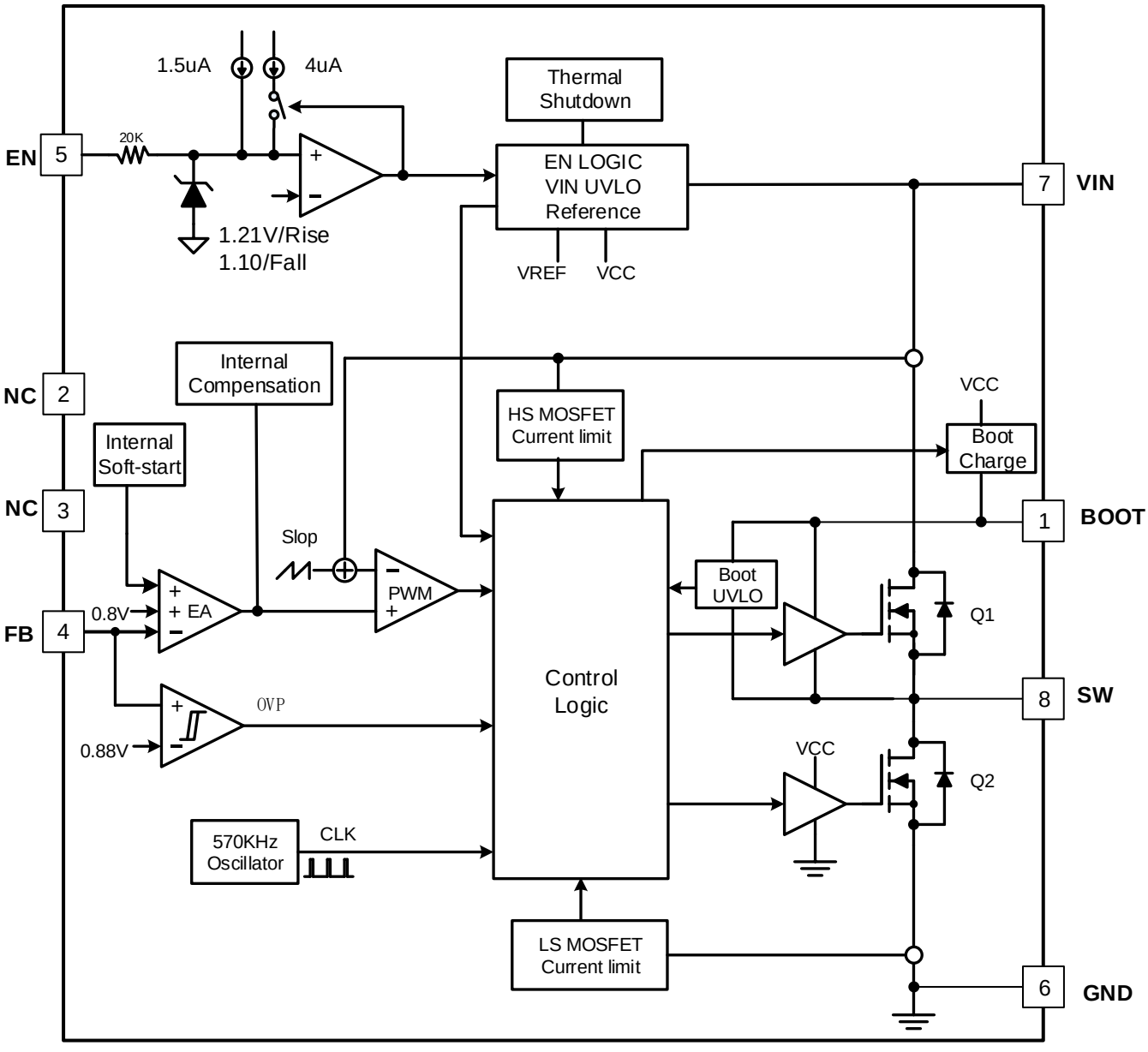


Figure 12. Functional Block Diagram

OPERATION

Overview

The SCT2433 is a 3.8V-40V input, 3.5A output, EMI friendly synchronous buck converter with built-in 80mΩ Rdson high-side and 50Ω Rdson low-side power MOSFETs. It implements constant frequency peak current mode control with internal compensation to regulate output voltage, providing excellent line and load transient response and make free the frequency compensation design.

The SCT2433 features 2ms internal soft-start time to avoid large inrush current and output voltage overshoot during startup and the switching frequency is 570kHz fixed. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 25uA under no load or sleep mode condition to achieve high efficiency at light load.

The SCT2433 has a default input start-up voltage of 3.5V with 400mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2433 implements the Frequency Spread Spectrum FSS modulation spreading of ±6% centered the selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time.

The SCT2433 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2433 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2433 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (400mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 1A peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 25uA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The SCT2433 is enabled when the VIN pin voltage rises about 3.5V and the EN pin voltage exceeds the enable threshold of 1.18V. The device is disabled when the VIN pin voltage falls below 3.1V or when the EN pin voltage is below 1.1V. An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 13 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = 1.18 * \left(1 + \frac{R1}{R2}\right) - 1.5uA * R1 \quad (1)$$

$$V_{fall} = 1.1 * \left(1 + \frac{R1}{R2}\right) - 5.5uA * R1 \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

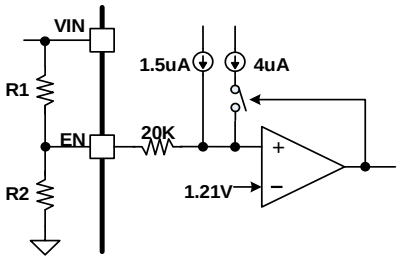


Figure 13. System UVLO by enable divide

Output Voltage

The SCT2433 regulates the internal reference voltage at 0.8V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Frequency Spread Spectrum

To reduce EMI, the SCT2433 implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the programmed switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency.

Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The UVLO of high-side MOSFET gate driver has rising threshold of 2.7V and hysteresis of 350mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.35V, BOOT UVLO occurs. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, SCT2433 operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.7V. When the voltage from BOOT to SW drops below 2.4V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 100ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.7V for high-side

MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e. during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem the SCT2433 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

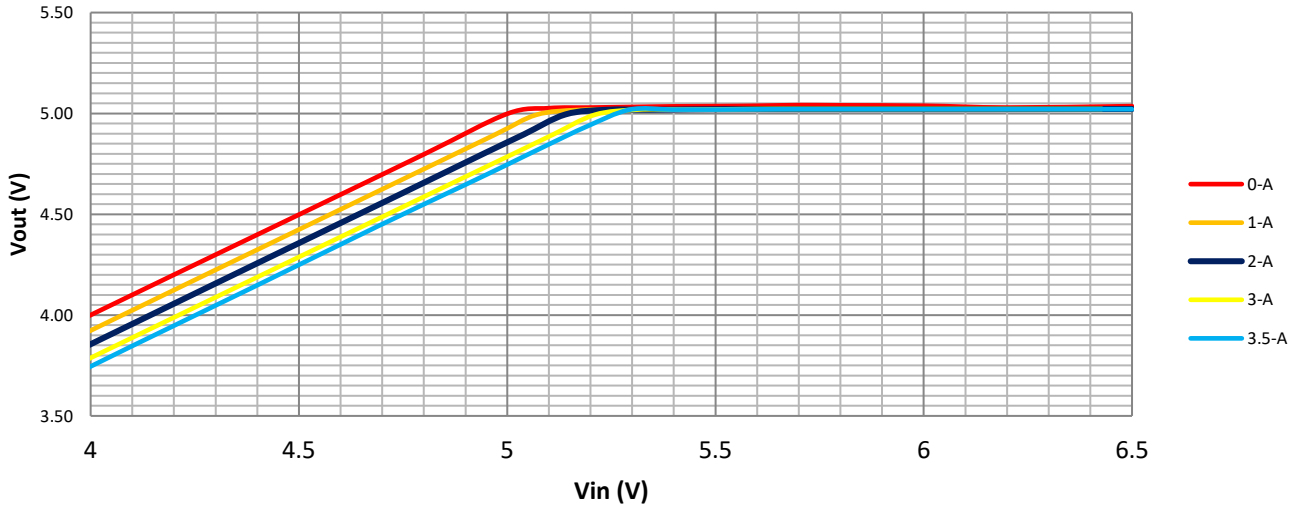


Figure 14. LDO Operation Characteristic (Vout =5V)

Over Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2433 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The COMP pin voltage ramps up to high clamp voltage 3.7V typical. When COMP voltage is clamped for 512 cycles, the converter stops switching. After remaining OFF for 8192 cycles，the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high for 512 cycles，the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enter normal regulating operation.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

Over voltage Protection

The SCT2433 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

The SCT2433 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 170C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 145C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

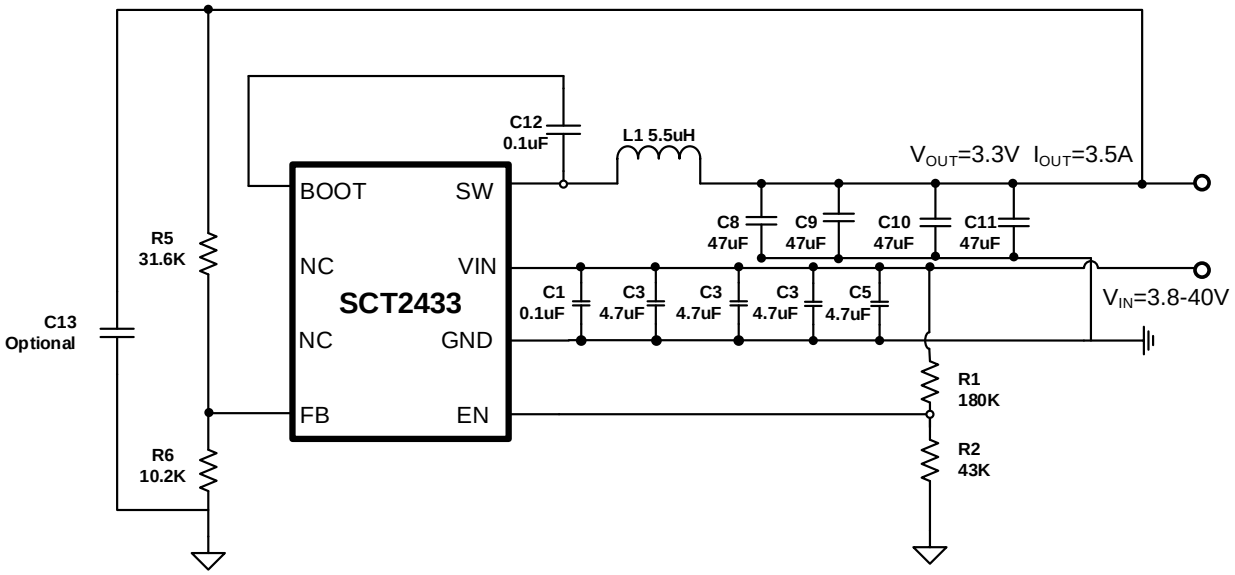


Figure 15. SCT2432 Design Example, 3.3V Output with Programmable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 3.8V to 40V
Output Voltage	3.3V
Maximum Output Current	3.5A
Switching Frequency	570 KHz
Output voltage ripple (peak to peak)	16.5mV
Transient Response 1.25A to 3.75A load step	ΔVout = 135mV
Start Input Voltage (rising VIN)	5.76V
Stop Input Voltage (falling VIN)	4.66V

Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use equation 4 to calculate R5.

$$R_5 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_6 \quad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V

Table 1. R_5, R_6Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_5	R_6
1.8 V	12.7 KΩ	10.2 KΩ
2.5 V	21.5 KΩ	10.2 KΩ
3.3 V	31.6 KΩ	10.2 KΩ
5 V	53.6 KΩ	10.2 KΩ
12 V	143 KΩ	10.2 KΩ
24V	294 KΩ	10.2 KΩ

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.7V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.64 V (stop or disable). Use Equation 5 and Equation 6 to calculate the values 173 kΩ and 42 kΩ of R_1 and R_2 resistors.

$$\mathrm{V_{rise}} = 1.18 * \left(1 + \frac{R_1}{R_2}\right) - 1.5\mathrm{uA} * \mathrm{R_1} \quad (5)$$

$$\mathrm{V_{fall}} = 1.1 * \left(1 + \frac{R_1}{R_2}\right) - 5.5\mathrm{uA} * R_1 \quad (6)$$

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 9.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (7)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 7 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (8)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 9 and equation 10.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (9)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (10)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2433 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

For this design, use LIR=0.2 or 0.3, and the inductor value is calculated to be 5.7uH, the RMS inductor current is 3.51A and the peak inductor current is 4A. The chosen inductor is a WE 744325650, which has a saturation current rating of 10A and a RMS current rating of 8.4A. This also has a typical inductance of 6.5μH at no load and 6 μH at 4A load. The inductor DCR is 12.5 mΩ.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 13.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (11)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (12)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

For this example, three 4.7μF, X7R ceramic capacitors rated for 50 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 14 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \quad (14)$$

Where

- $\Delta V_{OUT}$is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- $V_{IN}$is the input voltage

Due to capacitor's degrating under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 47μF ceramic output capacitors work for most applications.

Inverting Power application

The SCT2433 can be used to convert a positive input voltage to a negative output voltage. Typical applications are amplifiers requiring a negative power supply.

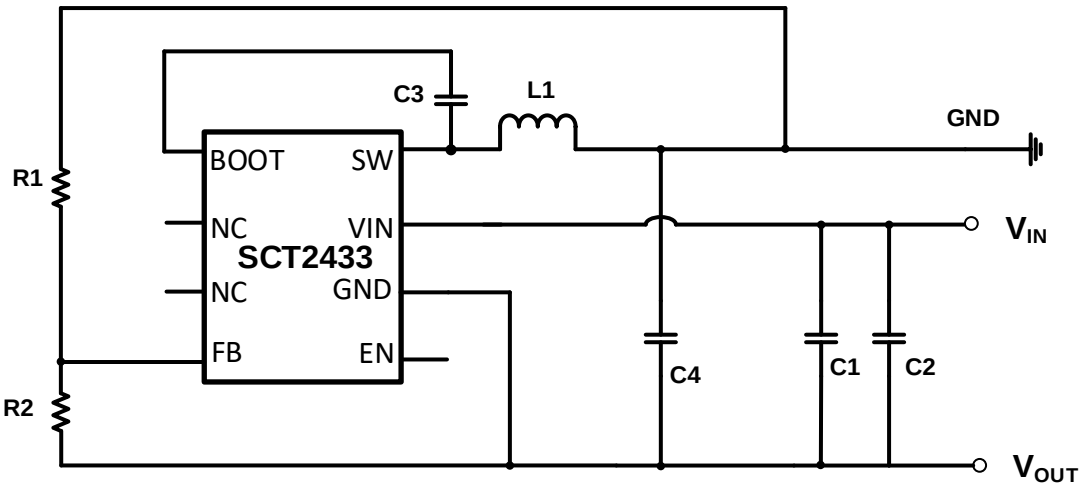


Figure 16. SCT2433 Inverting Power Supply

Application Waveforms

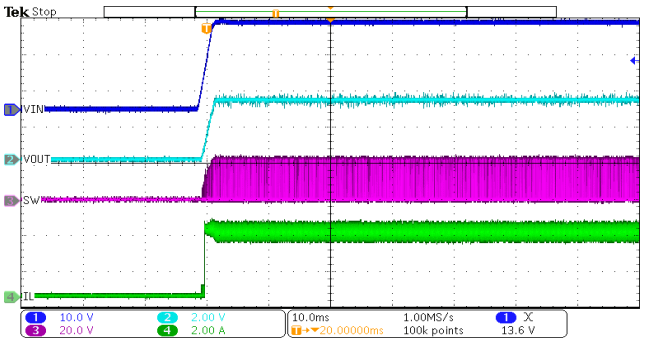


Figure 17. Power up

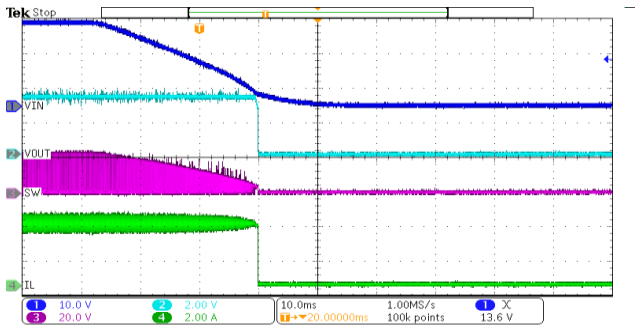


Figure 18. Power down

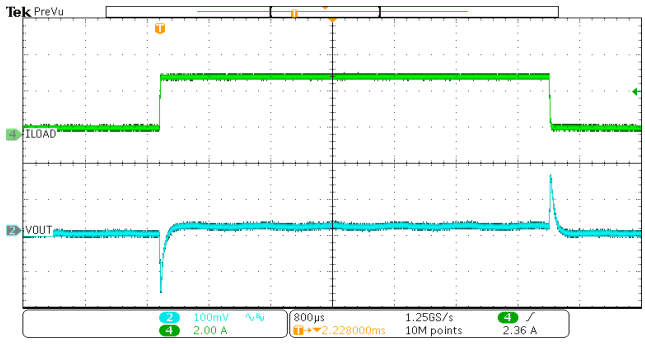


Figure 19.Load Transient (0.35A-3.15A, 250mA/us)

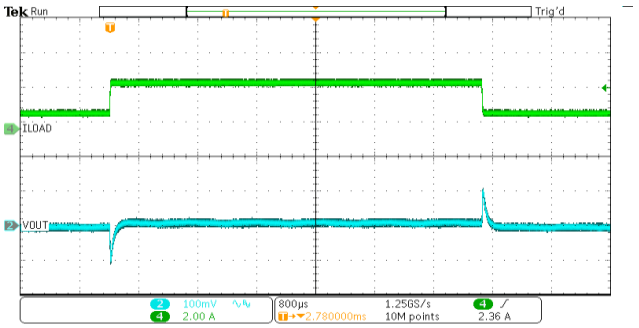


Figure 20. Load Transient (0.875A-2.625A, 250mA/us)

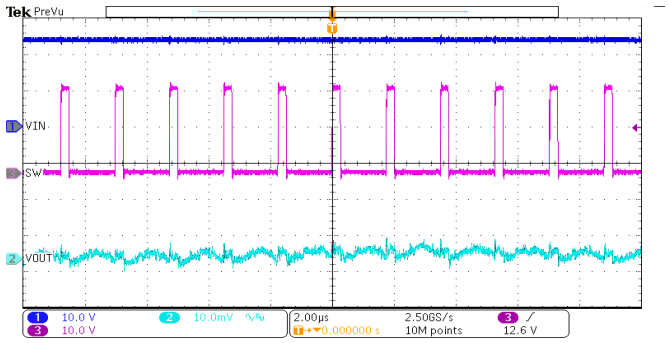


Figure 21. SW and Vout Ripple, (Iout=3.5A)

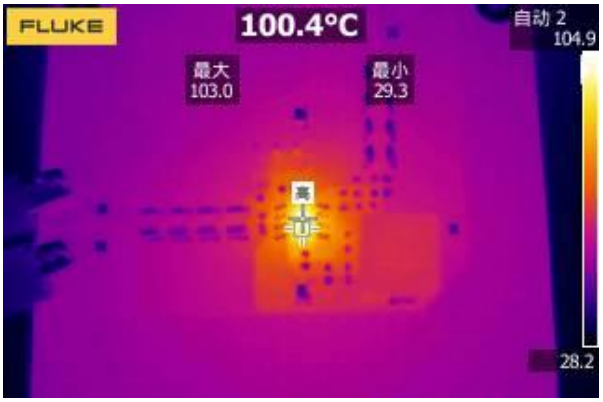


Figure 22. Thermal, 3.3Vout/3.5A

Layout Guideline

Proper PCB layout is a critical for SCT2433's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.

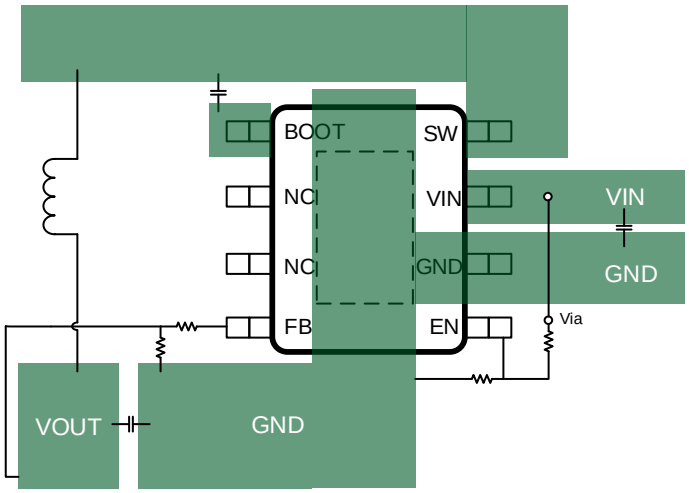
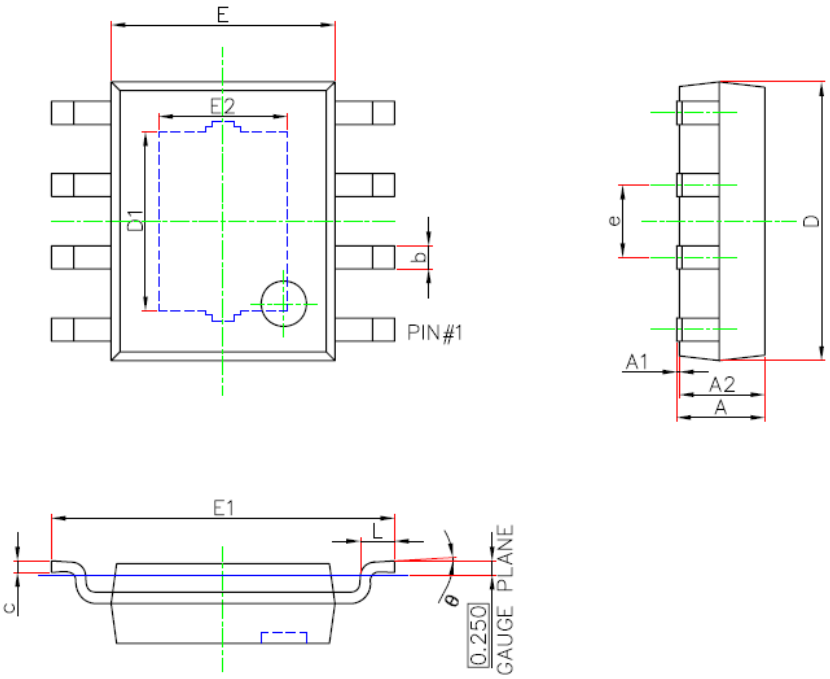


Figure 23. PCB Layout Example

PACKAGE INFORMATION



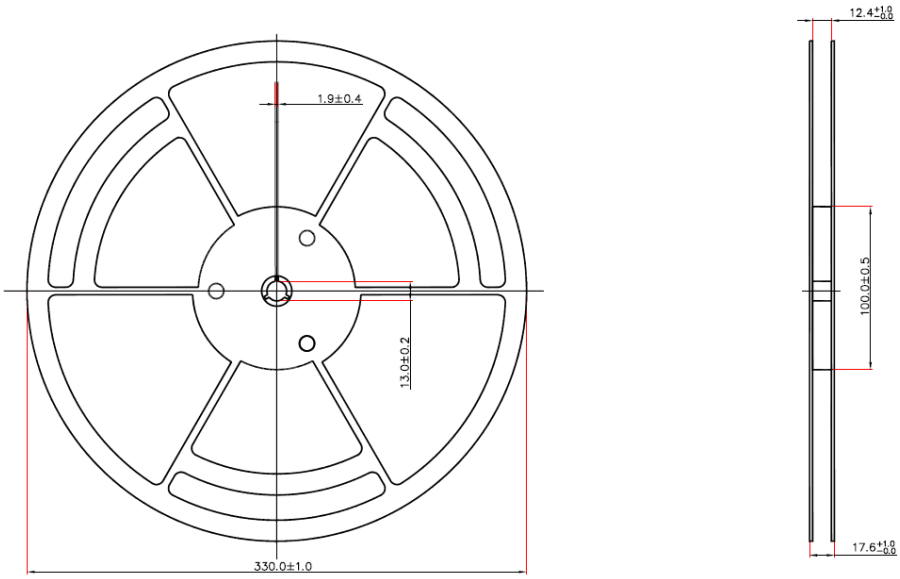
SOP8/PP(95x130) Package Outline Dimensions

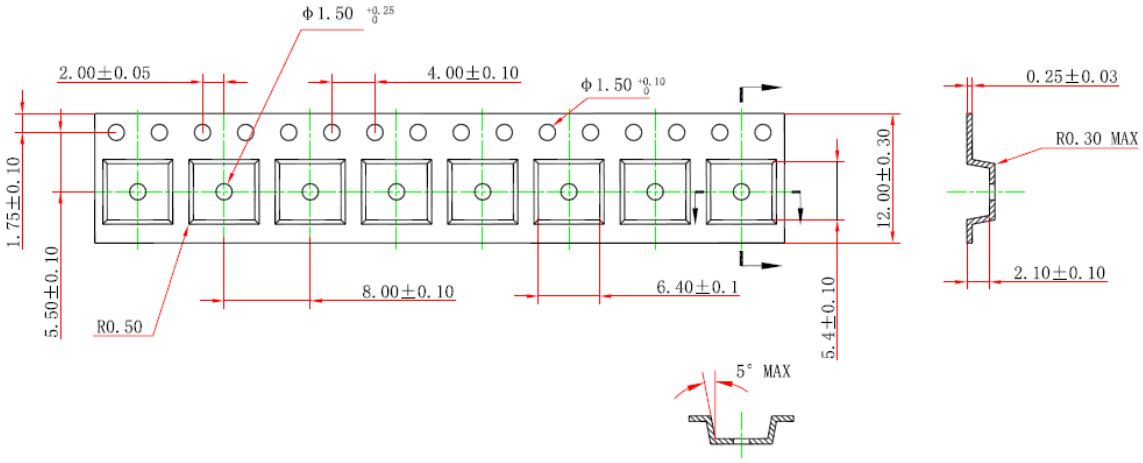
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

TAPE AND REEL INFORMATION





RELATED PARTS

PART NUMBERS	DESCRIPTION	COMMENTS
SCT2450	36V Vin, 5A Synchronous Step-down DCDC Converter with Programmable switching frequency and external synchronous clock	45mΩ / 20mΩ HS/LS MOSFETs Programmable soft start time Freq. = 100KHz- 1.1MHz adjustable Clock synchronization
SCT2451	36V Vin, 5A Synchronous Step-down DCDC Converter with Adjustable Soft Start Time	45mΩ / 20mΩ HS/LS MOSFETs Programmable soft start time Freq. = 570KHz
SCT2430A	36V Vin, 3.5A Synchronous Step-down DCDC Converter with 100KHz-1.1MHz Programmable Switching Frequency	55mΩ / 30mΩ HS/LS MOSFETs Internal 2ms Soft-time Freq. = 100KHz-1.1MHz adjustable. Clock synchronization
SCT2431A	36V Vin, 3.5A Synchronous Step-down DCDC Converter with Adjustable Soft Start Time	55mΩ / 30mΩ HS/LS MOSFETs Programmable soft start time Freq. = 570KHz
SCT2430	40V Vin, 3.5A Synchronous Step-down DCDC Converter with 100KHz-2.2MHz Programmable Switching Frequency	80mΩ / 50mΩ HS/LS MOSFETs Internal 2ms Soft-time Freq. = 100KHz-2.2MHz adjustable. Clock synchronization
SCT2432	40V Vin, 3.5A Synchronous Step-down DCDC Converter with 100KHz-2.2MHz Programmable Switching Frequency, Programmable Soft Start Time and Internal-compensation	80mΩ / 50mΩ HS/LS MOSFETs Programmable soft start time Freq. = 100KHz-2.2MHz adjustable. Clock synchronization Internal Compensation

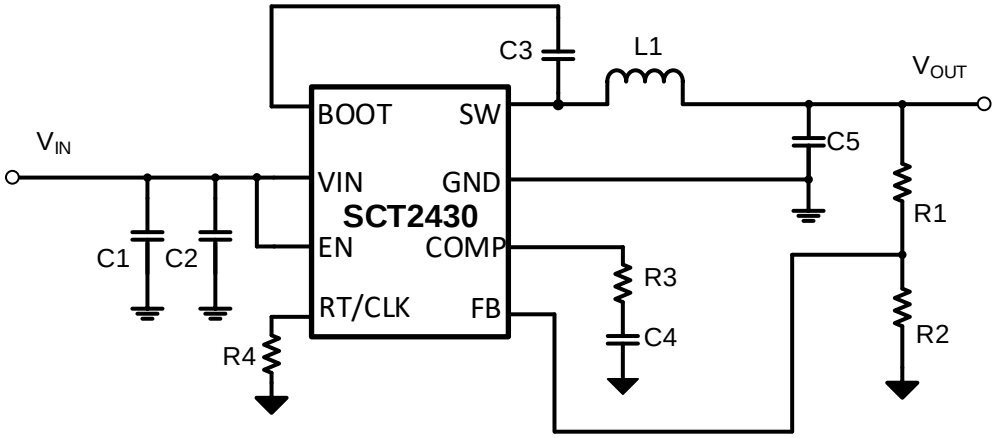


Figure 24. SCT2430 Typical Application

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