# 74LVTH16373
# 3.3V, 16-Bit D-Type Transparent Latch with 3-State Outputs

## GENERAL DESCRIPTION

The 74LVTH16373 is a high performance product designed for $V_{CC}$ operation at 3.3V. This device is a 16-bit D-type transparent latch with non-inverting 3-state bus compatible outputs, designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When latch enable (nLE) input is high, the nQn outputs follow the data nDn inputs. When nLE input is taken low, the nQn outputs are latched at the levels of the nDn inputs one set-up time prior to the high-to-low transition.

A buffered output enable ($n\overline{OE}$) input can be used to place the 8 outputs in either a normal logic state (high or low logic levels) or a high-impedance state.

The 74LVTH16373 bus hold on data inputs eliminates the need for external pull-up/pull-down resistors to hold unused inputs.

## FEATURES

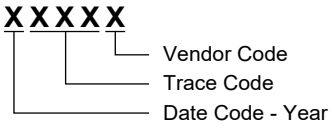
- **16-Bit Transparent Latch**
- **3-State Buffers**
- **Output Capability: +64mA/-32mA**
- **TTL Input and Output Switching Levels**
- **Input and Output Interface Capability to Systems at 5V Supply**
- **Bus Hold on Data Inputs Eliminates the Need for External Pull-Up/Pull-Down Resistors**
- **Live Insertion and Extraction Permitted**
- **Power-Up Reset**
- **Power-Up 3-State**
- **No Bus Current Loading When Output is Tied to 5V Bus**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TSSOP-48 Package**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| 74LVTH16373 | TSSOP-48 | -40℃ to +125℃ | 74LVTH16373XTS48G/TR | 74LVTH16373<br>XTS48<br>XXXXX | Tape and Reel, 2500 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, $V_{CC}$ ..... -0.5V to 4.6V
Input Voltage, $V_I$ (2) ..... -0.5V to 7V
Output Voltage, $V_O$ (2)
Output in 3-State or High-State ..... -0.5V to 7V
Input Clamping Current, $I_{IK}$ ($V_I$ < 0V) ..... -50mA
Output Clamping Current, $I_{OK}$ ($V_O$ < 0V) ..... -50mA
Output Current, $I_O$
Output in High-State ..... -64mA
Output in Low-State ..... 128mA
Supply Current, $I_{CC}$ ..... 128mA
Ground Current, $I_{GND}$ ..... -256mA
Junction Temperature (3) ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM ..... 8000V
CDM ..... 1000V

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage, $V_{CC}$ ..... 2.7V to 3.6V
Input Voltage, $V_I$ ..... 0V to 5.5V
High-Level Output Current, $I_{OH}$ ..... -32mA
Low-Level Output Current, $I_{OL}$ ..... 64mA
Input Transition Rise and Fall Rate, Δt/ΔV
..... 10ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

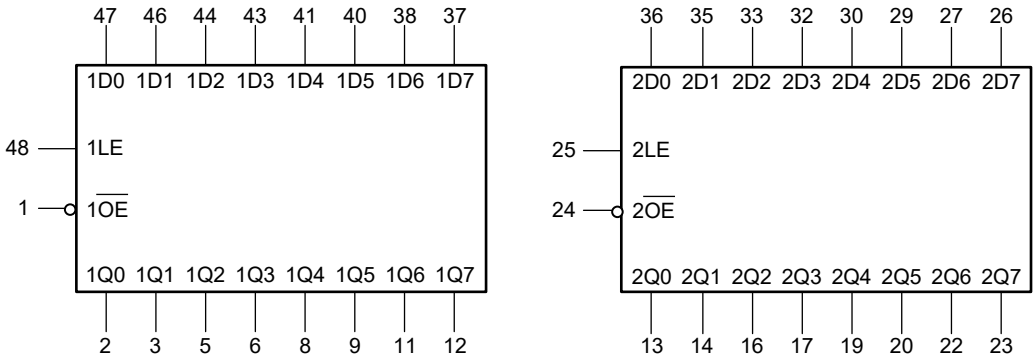
## ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

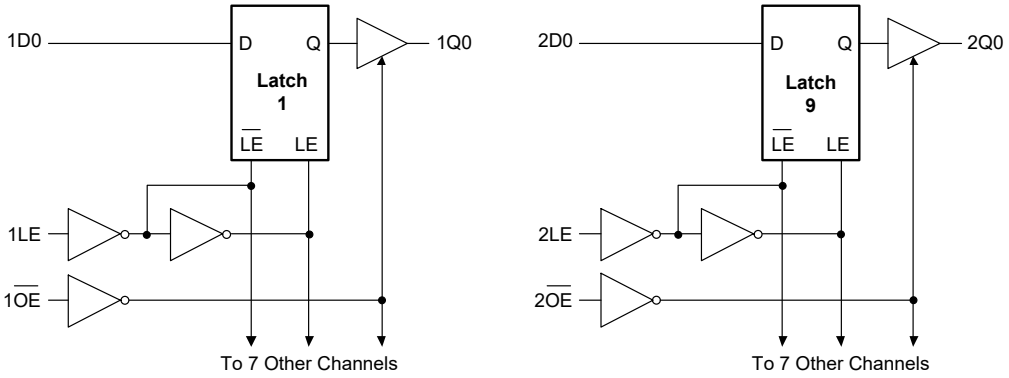
## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## LOGIC SYMBOL




## LOGIC DIAGRAM




## FUNCTION TABLE

| OPERATING MODE | CONTROL INPUT | | | INTERNAL REGISTER | OUTPUT |
|---|---|---|---|---|---|
| | $n\overline{OE}$ | nLE | nDn | | nQn |
| Enable and Read Register (Transparent Mode) | L | H | L | L | L |
| | L | H | H | H | H |
| Latch and Read Register | L | L | l | L | L |
| | L | L | h | H | H |
| Latch Register and Disable Outputs | H | L | l | L | Z |
| | H | L | h | H | Z |

H = High Voltage Level

L = Low Voltage Level

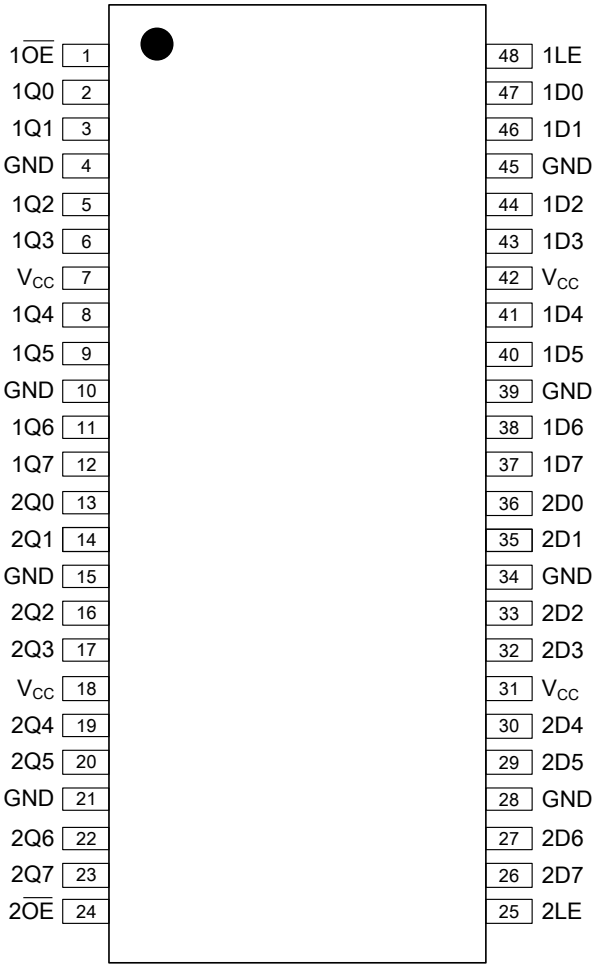
h = High Voltage Level One Set-Up Time Prior to the High-to-Low LE Transition

l = Low Voltage Level One Set-Up Time Prior to the High-to-Low LE Transition

Z = High-Impedance State

## PIN CONFIGURATION

(TOP VIEW)




TSSOP-48

## PIN DESCRIPTION

| PIN | NAME | FUNCTION |
|---|---|---|
| 47, 46, 44, 43, 41, 40, 38, 37 | 1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7 | Data Inputs. |
| 36, 35, 33, 32, 30, 29, 27, 26 | 2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7 | Data Inputs. |
| 1, 24 | 1$\overline{OE}$, 2$\overline{OE}$ | Output Enable Inputs (Active Low). |
| 48, 25 | 1LE, 2LE | Latch Enable Inputs (Active High). |
| 2, 3, 5, 6, 8, 9, 11, 12 | 1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7 | Data Outputs. |
| 13, 14, 16, 17, 19, 20, 22, 23 | 2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7 | Data Outputs. |
| 4, 10, 15, 21, 28, 34, 39, 45 | GND | Ground. |
| 7, 18, 31, 42 | $V_{CC}$ | Supply Voltage. |

# ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at $V_{CC}$ = 3.3V and $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | TEMP | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Input Clamping Voltage | $V_{IK}$ | $V_{CC}$ = 2.7V, $I_{IK}$ = -18mA | | Full | -1.2 | -0.78 | | V |
| High-Level Input Voltage | $V_{IH}$ | $V_{CC}$ = 2.7V to 3.6V | | Full | 2 | | | V |
| Low-Level Input Voltage | $V_{IL}$ | $V_{CC}$ = 2.7V to 3.6V | | Full | | | 0.8 | V |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$ = -100μA, $V_{CC}$ = 2.7V to 3.6V | | Full | $V_{CC}$ - 0.05 | $V_{CC}$ - 0.001 | | V |
| | | $I_{OH}$ = -8mA, $V_{CC}$ = 2.7V | | Full | 2.45 | 2.6 | | |
| | | $I_{OH}$ = -32mA, $V_{CC}$ = 3.0V | | Full | 2.1 | 2.65 | | |
| Low-Level Output Voltage | $V_{OL}$ | $V_{CC}$ = 2.7V | $I_{OL}$ = 100μA | Full | | 0.001 | 0.05 | V |
| | | | $I_{OL}$ = 24mA | Full | | 0.15 | 0.28 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 16mA | Full | | 0.1 | 0.18 | |
| | | | $I_{OL}$ = 32mA | Full | | 0.2 | 0.36 | |
| | | | $I_{OL}$ = 64mA | Full | | 0.4 | 0.55 | |
| Power-Up Low-Level Output Voltage (1) | $V_{OL\_PU}$ | $V_{CC}$ = 3.6V, $I_{OL}$ = 1mA, $V_I$ = $V_{CC}$ or GND | | Full | | 5 | 50 | mV |
| Input Leakage Current | $I_I$ | Control pins, $V_{CC}$ = 3.6V, $V_I$ = $V_{CC}$ or GND | | Full | | ±0.01 | ±1 | μA |
| | | Control pins, $V_{CC}$ = 0V or 3.6V, $V_I$ = 5.5V | | Full | | 0.01 | 5 | |
| | | Input data pins (2), $V_{CC}$ = 0V or 3.6V, $V_I$ = 5.5V | | Full | | 0.4 | 5 | |
| | | Input data pins (2), $V_{CC}$ = 3.6V, $V_I$ = $V_{CC}$ | | Full | | 0.3 | 2 | |
| | | Input data pins (2), $V_{CC}$ = 3.6V, $V_I$ = GND | | Full | -2 | -0.01 | | |
| Off-State Output Current | $I_{OZ}$ | $V_{CC}$ = 3.6V | $V_O$ = 3.0V | Full | | 0.01 | 2 | μA |
| | | | $V_O$ = 0.5V | Full | -2 | -0.01 | | |
| Output Leakage Current | $I_{LO}$ | Output in high-state when $V_O$ > $V_{CC}$, $V_O$ = 5.5V, $V_{CC}$ = 3.0V | | Full | | 1 | 30 | μA |
| Power-Up/Down Output Current | $I_{O\_PU/PD}$ | $V_{CC}$ ≤ 1.2V, $V_O$ = 0.5V to $V_{CC}$, $V_I$ = GND or $V_{CC}$, $n\overline{OE}$ = don't care | | +25℃ | | 0.01 | 10 | μA |
| Power-Off Leakage Current | $I_{OFF}$ | $V_{CC}$ = 0V, $V_I$ or $V_O$ = 0V to 5.5V | | Full | | 0.01 | 10 | μA |
| Supply Current | $I_{CC}$ | $V_{CC}$ = 3.6V, $V_I$ = GND or $V_{CC}$, $I_O$ = 0A | Outputs high | Full | | 12 | 80 | μA |
| | | | Outputs low | Full | | 12 | 80 | |
| | | | Outputs disabled (3) | Full | | 12 | 80 | |
| Additional Supply Current (4) | $\Delta I_{CC}$ | Per input pin, $V_{CC}$ = 3.0V to 3.6V, one input at $V_{CC}$ - 0.6V, other inputs at $V_{CC}$ or GND | | Full | | 0.2 | 200 | μA |
| Input Capacitance | $C_I$ | Input pins, $V_I$ = 0V or 3.0V | | +25℃ | | 6 | | pF |
| Output Capacitance | $C_O$ | Output pins nQn, outputs disabled, $V_O$ = 0V or $V_{CC}$ | | +25℃ | | 9 | | pF |
| Bus Hold Low Current | $I_{BHL}$ | $V_{CC}$ = 3.0V, $V_I$ = 0.8V | | Full | 50 | 100 | | μA |
| Bus Hold High Current | $I_{BHH}$ | $V_{CC}$ = 3.0V, $V_I$ = 2.0V | | Full | | -130 | -75 | μA |
| Bus Hold Low Overdrive Current (5) | $I_{BHLO}$ | Input data pins, $V_I$ = 0V to 3.6V, $V_{CC}$ = 3.6V | | Full | 500 | 200 | | μA |
| Bus Hold High Overdrive Current (5) | $I_{BHHO}$ | Input data pins, $V_I$ = 0V to 3.6V, $V_{CC}$ = 3.6V | | Full | | -280 | -500 | μA |

NOTES:

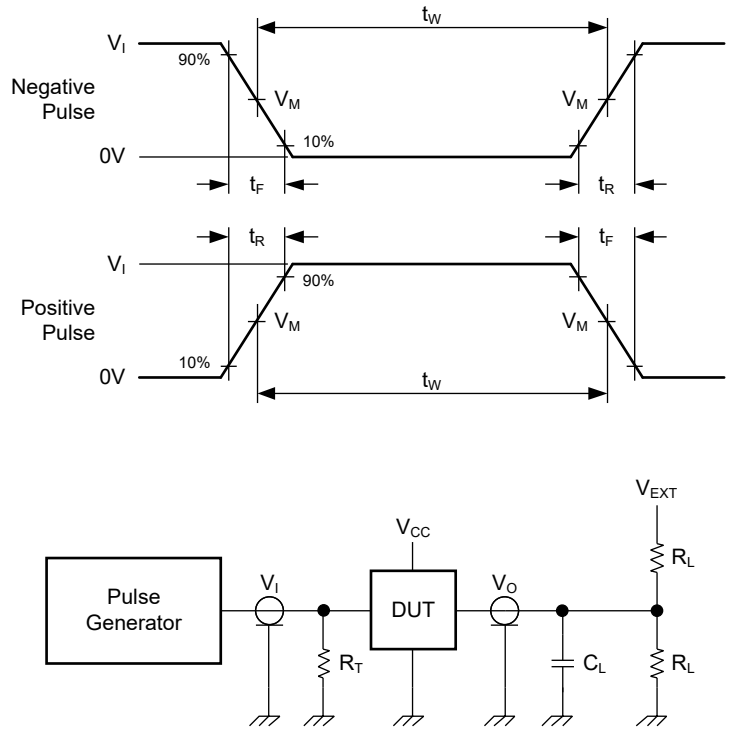
1. For valid test results, data must not be loaded into the latches after applying power.
2. Unused pins at $V_{CC}$ or GND.
3. $I_{CC}$ is measured with outputs pulled to $V_{CC}$ or GND.
4. This is the increase in supply current for each input at the specified voltage level other than $V_{CC}$ or GND.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

## DYNAMIC CHARACTERISTICS

(For test circuit, see Figure 1. All typical values are measured at $V_{CC}$ = 3.3V and $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | TEMP | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Low to High Propagation Delay | $t_{PLH}$ | nDn to nQn, see Figure 2 | $V_{CC}$ = 2.7V | +25℃ | | 3.4 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 3.4 | | |
| High to Low Propagation Delay | $t_{PHL}$ | nDn to nQn, see Figure 2 | $V_{CC}$ = 2.7V | +25℃ | | 3.8 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 3.5 | | |
| Low to High Propagation Delay | $t_{PLH}$ | nLE to nQn, see Figure 3 | $V_{CC}$ = 2.7V | +25℃ | | 3.6 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 3.6 | | |
| High to Low Propagation Delay | $t_{PHL}$ | nLE to nQn, see Figure 3 | $V_{CC}$ = 2.7V | +25℃ | | 4 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 4 | | |
| Off-State to High Propagation Delay | $t_{PZH}$ | $n\overline{OE}$ to nQn, see Figure 4 | $V_{CC}$ = 2.7V | +25℃ | | 5.3 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 4.9 | | |
| Off-State to Low Propagation Delay | $t_{PZL}$ | $n\overline{OE}$ to nQn, see Figure 4 | $V_{CC}$ = 2.7V | +25℃ | | 5 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 4.9 | | |
| High to Off-State Propagation Delay | $t_{PHZ}$ | $n\overline{OE}$ to nQn, see Figure 4 | $V_{CC}$ = 2.7V | +25℃ | | 4.9 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 4.6 | | |
| Low to Off-State Propagation Delay | $t_{PLZ}$ | $n\overline{OE}$ to nQn, see Figure 4 | $V_{CC}$ = 2.7V | +25℃ | | 5.4 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 5.4 | | |
| High Set-Up Time | $t_{SUH}$ | nDn to nLE, see Figure 5 | $V_{CC}$ = 2.7V | +25℃ | | 0.3 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 0.3 | | |
| Low Set-Up Time | $t_{SUL}$ | nDn to nLE, see Figure 5 | $V_{CC}$ = 2.7V | +25℃ | | 0.3 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 0.3 | | |
| High Hold Time | $t_{HH}$ | nDn to nLE, see Figure 5 | $V_{CC}$ = 2.7V | +25℃ | | 0.2 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 0.2 | | |
| Low Hold Time | $t_{HL}$ | nDn to nLE, see Figure 5 | $V_{CC}$ = 2.7V | +25℃ | | 0.2 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 0.2 | | |
| High Pulse Width | $t_{WH}$ | nLE, see Figure 3 | $V_{CC}$ = 2.7V | +25℃ | | 1.5 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | +25℃ | | 1.5 | | |

## TEST CIRCUIT




Test conditions are given in Table 1.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_O$ of the pulse generator.

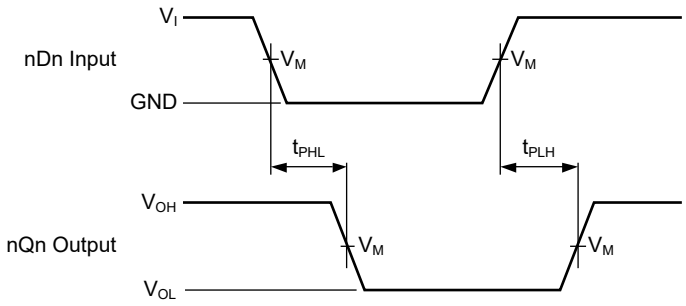
$V_{EXT}$ = External voltage for measuring switching times.

**Figure 1. Test Circuit for Measuring Switching Times**

**Table 1. Test Conditions**

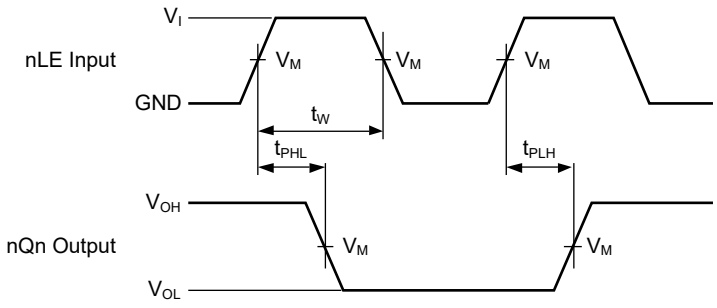
| SUPPLY VOLTAGE | INPUT | | | | LOAD | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $f_I$ | $t_W$ | $t_R$, $t_F$ | $C_L$ | $R_L$ | $t_{PHZ}$, $t_{PZH}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PLH}$, $t_{PHL}$ |
| 2.7V to 3.6V | 2.7V | ≤ 10MHz | 500ns | ≤ 2.5ns | 50pF | 500Ω | GND | 6V | open |

## WAVEFORMS




Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

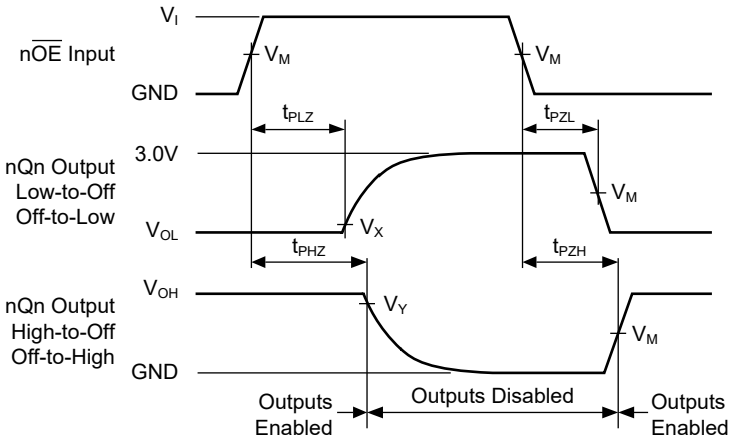
**Figure 2. Input (nDn) to Output (nQn) Propagation Delays**




Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

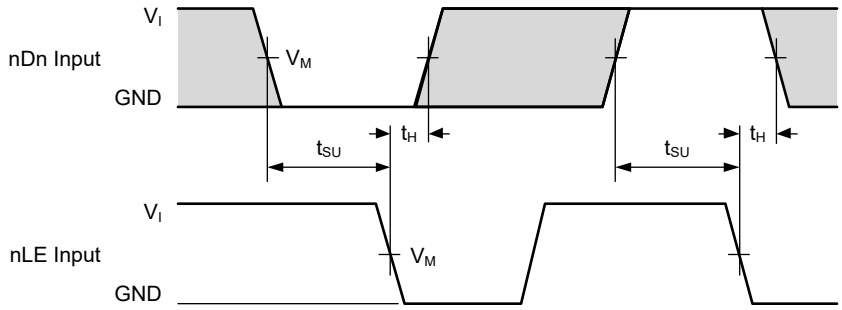
**Figure 3. Latch Enable Input Pulse Width and the Latch Enable Input to Output Propagation Delays**

## WAVEFORMS (continued)




Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Figure 4. Enable and Disable Times**




Test conditions are given in Table 1.
Measurement points are given in Table 2.
The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 5. Data Set-Up and Hold Times for the nDn Input to the nLE Input**

**Table 2. Measurement Points**

| SUPPLY VOLTAGE | INPUT | | OUTPUT | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 2.7V to 3.6V | 2.7V | 1.5V | 1.5V | $V_{OL}$ + 0.3V | $V_{OH}$ - 0.3V |

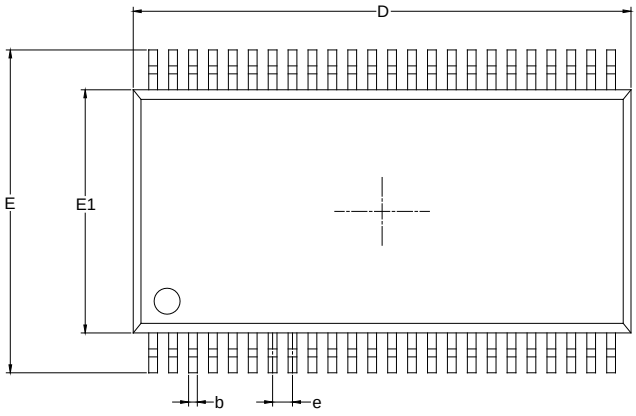
# REVISION HISTORY

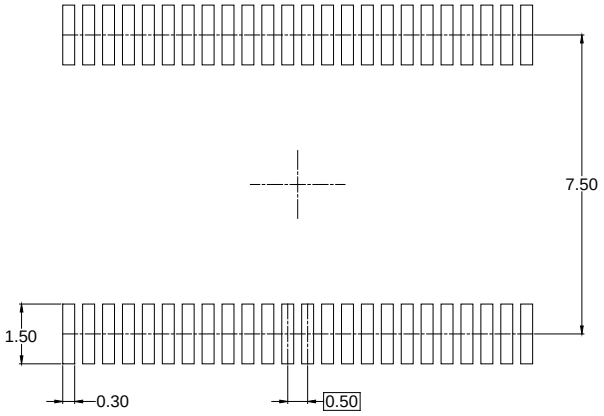
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (MARCH 2021) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

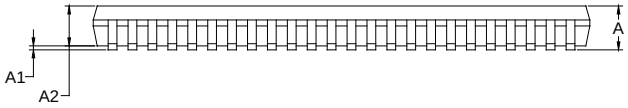
# PACKAGE OUTLINE DIMENSIONS

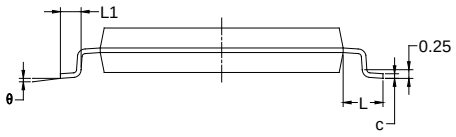
## TSSOP-48




**RECOMMENDED LAND PATTERN** (Unit: mm)

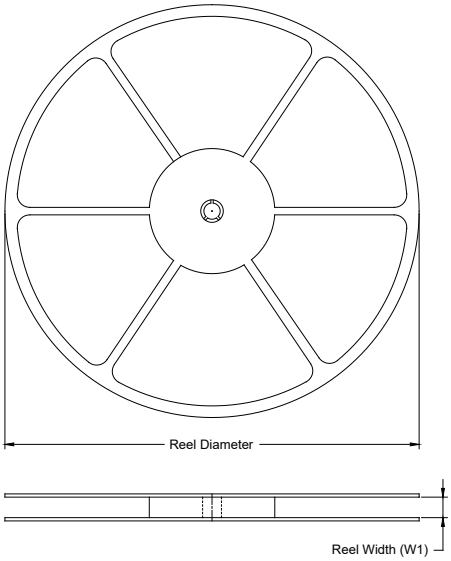


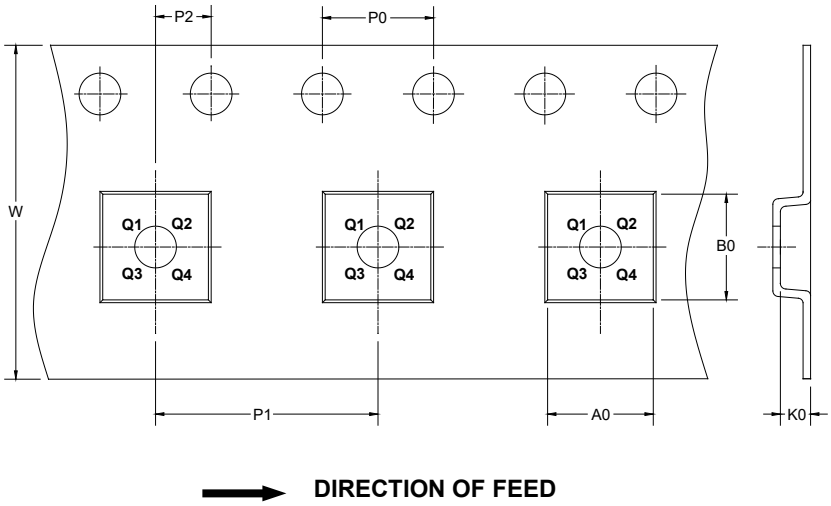

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | | | 1.20 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.85 | 0.95 | 1.05 |
| b | 0.18 | | 0.26 |
| c | 0.15 | | 0.19 |
| D | 12.40 | 12.50 | 12.60 |
| E | 7.90 | 8.10 | 8.30 |
| E1 | 6.00 | 6.10 | 6.20 |
| e | 0.50 BSC | | |
| L | 1.00 REF | | |
| L1 | 0.45 | | 0.75 |
| θ | 0° | | 8° |

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS




DIRECTION OF FEED

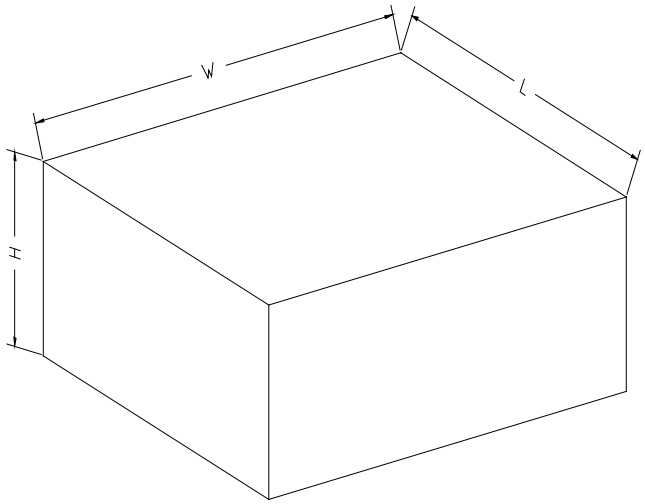
NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP-48 | 13” | 24.4 | 8.60 | 13.00 | 1.80 | 4.0 | 12.0 | 2.0 | 24.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002