SGM25701
Positive High-Voltage Hot Swap and Inrush Current Controller with Power-Limiting

GENERAL DESCRIPTION

The SGM25701 is a positive hot swap controller that allows a board to be safely inserted or removed from a live backplane. Inrush current control function can effectively reduce the voltage drop on the power supply rail.

The SGM25701 offers programmable power-limiting and current limit to ensure that the external MOSFET operates within its safe operating area (SOA) at all times.

The chip has a good output indication function when the V_{OUT} increases to within the 1.4V range of the V_{IN}.

Programmable under-voltage lockout or over-voltage lockout is used to turn off the device if the V_{IN} drops below or raises over a threshold value. The fault detection time and initial insertion delay time can also be adjusted by the user.

The SGM25701B will latch off when a fault is detected, while the SGM25701A will go into auto-retry mode.

SGM25701 is available in a Green MSOP-10 package.

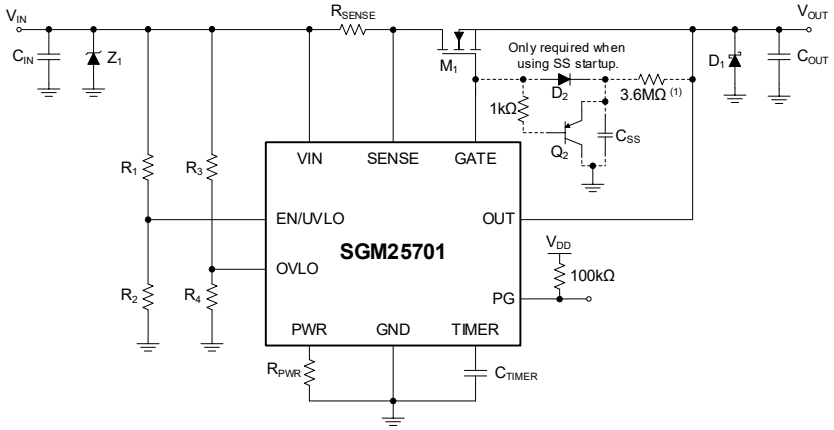
FEATURES

- **Wide Input Voltage Range: 9V to 70V**
- **Inrush Current Limit, PCB can be Safely Inserted into Live Equipment**
- **External Device Programming Maximum Loss Limit**
- **Programmable Current Limit**
- **Adjustable Under-Voltage Lockout (EN/UVLO)**
- **Adjustable Over-Voltage Lockout (OVLO)**
- **Open-Drain for Good Output Indication**
- **Quick Cut-Off Function when Severe Over-Current Occurs**
- **Configure Charge Pump/Gate Driver for External N-MOSFET**
- **The Setting of the Insertion Time Allowing the Ringing and Transient Recovery Process after the System Connected**
- **Adjustable Fault Timing to Prevent False Shutdown**
- **Behavior after Fault:**
  - **SGM25701A: Auto-Retry**
  - **SGM25701B: Latch-Off**
- **Available in a Green MSOP-10 Package**

APPLICATIONS

24V/48V Industrial System
Server Backplane System
Solid State Circuit Breaker
Base Station

TYPICAL APPLICATION



NOTE: 1. The resistance provides a stable leaking path for the GATE pin when the VIN is quickly pulled low in the case of repeated restarts.

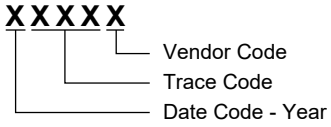
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25701A	MSOP-10	-40℃ to +125℃	SGM25701AXMS10G/TR	SGM004 XMS10 XXXXX	Tape and Reel, 4000
SGM25701B	MSOP-10	-40℃ to +125℃	SGM25701BXMS10G/TR	SGM095 XMS10 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN to GND (1) ..... -0.3V to 80V
SENSE, OUT and PG to GND ..... -0.3V to 80V
GATE to GND (1) ..... -0.3V to 80V
OUT to GND (1ms Transient) (2) ..... -1V to 80V
EN/UVLO to GND ..... -0.3V to 80V
OVLO to GND ..... -0.3V to 6V
VIN to SENSE ..... -0.3V to 0.3V
Package Thermal Resistance
MSOP-10, θ_{JA} ..... 147℃/W
MSOP-10, θ_{JB} ..... 94℃/W
MSOP-10, θ_{JC} ..... 52℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

NOTES:

1. When the chip is enabled, the voltage of GATE pin is generally 12.7V higher than the VIN pin voltage. Therefore, the absolute maximum rating of V_{IN} (80V) is only applicable when the chip is stopped, or since the absolute maximum rating of the GATE pin is also 80V, the 80V of V_{IN} is only applicable when the pin is momentarily surged.

2. An external MOSFET with V_{GS_TH} higher than V_{OUT} is required during -ve transients. This effectively prevents false turn-on of the MOSFET during -ve transients.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 9V to 70V
PG Voltage ..... 0V to 70V
Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

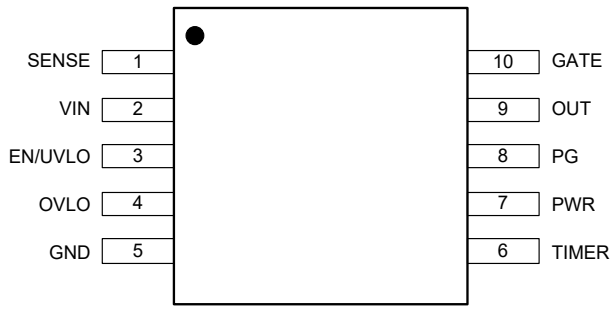
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



MSOP-10

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	SENSE	I	Current Sense Pin. The voltage from the input pin to this pin is measured by the current flowing into the sense resistor. When the detected voltage at the R_{SENSE} exceeds 55mV, it indicates that the circuit is in an overload state at this time, and the fault timer is started at this time.
2	VIN	I	Input Supply Voltage. It is recommended to place a small bypass capacitor close this pin.
3	EN/UVLO	I	Enable and Under-Voltage Lockout Pin. The EN/UVLO threshold is programmed by an external resistor divider. Internal hysteresis is controlled by a 19μA current source. The threshold of the turn-on voltage is set to 2.5V. It is also possible to control this pin for remote shutdown.
4	OVLO	I	Over-Voltage Lockout Pin. The over-voltage threshold is programmed by the resistor divider from the power supply to the OVLO terminal to GND. Hysteretic control is achieved through an internally programmed 19μA current source. The over-voltage shutdown threshold is set to 2.5V.
5	GND	-	Ground.
6	TIMER	I/O	Fault Timer Pin. An external capacitor between TIMER and GND pins provides the fault time delay and insertion delay time. The chip's restart time is also controlled by this capacitor.
7	PWR	I	Power-Limiting Programmable Pin. The R_{PWR} and R_{SENSE} determine the maximum allowable dissipation of the external MOSFET.
8	PG	O	Power Good Indicator Pin. The V_{DS} voltage of the external MOSFET determines its state.
9	OUT	I	Power Output Pin. Connect this pin to output (i.e., external MOSFET source). The chip monitors MOSFET V_{DS} voltage through this pin to limit the MOSFET power and control the PG signal accordingly.
10	GATE	O	Gate Drive Output. This pin is connected to the gate of the external MOSFET. During normal operation, the voltage on this pin will be 12.7V higher than the OUT pin.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, V_{IN} = 48V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VIN						
Input Current, Enabled	I_{IN_EN}	$V_{EN/UVLO}$ > 2.5V and V_{OVLO} < 2.5V		0.40	0.55	mA
Input Current, Disabled	I_{IN_DIS}	$V_{EN/UVLO}$ < 2.5V or V_{OVLO} > 2.5V		70	110	μA
Power-On Reset Threshold at VIN to Trigger Insertion Timer	POR_{IT}	V_{IN} increasing		7.6	8.1	V
Power-On Reset Threshold at VIN to Enable All Functions	POR_{EN}	V_{IN} increasing		8.4	9.0	V
POR_{EN} Hysteresis	POR_{EN_HYS}	V_{IN} decreasing		90		mV
OUT						
OUT Bias Current, Enabled	I_{OUT_EN}	V_{OUT} = V_{IN}, normal operation		6		μA
OUT Bias Current, Disabled (1)	I_{OUT_DIS}	Disabled, V_{OUT} = 0V, V_{SENSE} = V_{IN}		25		
EN/UVLO, OVLO						
EN/UVLO Threshold Voltage	$V_{EN/UVLO}$		2.4	2.5	2.6	V
EN/UVLO Hysteresis Current	$I_{EN/UVLO\_HYS}$	$V_{EN/UVLO}$ = 1V	12	19	26	μA
EN/UVLO Delay Time	$t_{EN/UVLO\_DLY}$	Delay to GATE high		15		μs
		Delay to GATE low		1		
EN/UVLO Bias Current	$V_{EN/UVLO\_BIAS}$	$V_{EN/UVLO}$ = 48V			1	μA
OVLO Threshold Voltage	V_{OVLO}		2.4	2.5	2.6	V
OVLO Hysteresis Current	I_{OVLO_HYS}	V_{OVLO} = 2.6V	12	19	26	μA
OVLO Delay Time	t_{OVLO_DLY}	Delay to GATE high		15		μs
		Delay to GATE low		1		
OVLO Bias Current	V_{OVLO_BIAS}	V_{OVLO} = 2.4V			1	μA
PWR						
Power-Limiting Sense Voltage (VIN - SENSE)	PWR_{LIM-1}	$V_{(SENSE - OUT)}$ = 48V, R_{PWR} = 150kΩ	19	25	31	mV
	PWR_{LIM-2}	$V_{(SENSE - OUT)}$ = 24V, R_{PWR} = 75kΩ		25		mV
PWR Pin Current	I_{PWR}	V_{PWR} = 2.5V		20		μA
GATE Pin						
Source Current	I_{GATE}	Normal operation, $V_{(GATE - OUT)}$ = 5V	10	16	22	μA
Sink Current		$V_{EN/UVLO}$ < 2.5V	1.8	2.1	2.4	mA
		$V_{(VIN - SENSE)}$ = 150mV or V_{IN} < POR_{IT}, V_{GATE} = 5V	55	85	115	mA
Gate Output Voltage in Normal Operation	V_{GATE}	GATE - OUT voltage	12.2	12.7	13.2	V

NOTE: 1. A 1MΩ resistor between OUT and SENSE pins determines the bias current (disabled) of V_{OUT}.

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, V_{IN} = 48V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit						
Threshold Voltage	V_{CL}	VIN - SENSE voltage	48.5	55.0	61.5	mV
Response Time	t_{CL}	VIN - SENSE stepped from 0mV to 80mV		10		μs
SENSE Input Current	I_{SENSE}	Enabled, V_{SENSE} = V_{OUT}		12		μA
		Disabled, V_{OUT} = 0V		70		
Circuit Breaker						
Threshold Voltage	V_{CB}	VIN - SENSE voltage	80	105	130	mV
Response Time	t_{CB}	VIN - SENSE stepped from 0mV to 150mV, time to GATE low, no load		0.4	1.2	μs
TIMER						
Upper Threshold	V_{TMRH}		3.85	4.00	4.15	V
Lower Threshold	V_{TMRL}	Restart cycles (SGM25701A)	1.20	1.25	1.30	
		End of 8th cycle (SGM25701A)		0.3		
		Re-enable Threshold (SGM25701B)		0.3		
Insertion Time Current	I_{TIMER}		3	5	7	μA
Sink Current, End of Insertion Time		V_{TIMER} = 2V	1.2	1.6	2.0	mA
Fault Detection Current			70	95	120	μA
Fault Sink Current			1.5	2.4	3.3	μA
Fault Restart Duty Cycle	DC_{FAULT}			0.43		%
Fault to GATE Low Delay	t_{FAULT}	TIMER pin reaches 4V		1		μs
PG						
Threshold Measured at SENSE - OUT	PG_{TH}	Decreasing	0.8	1.4	2.0	V
		Increasing, relative to decreasing threshold	0.8	1.4	2.0	
Output Low Voltage	PG_{VOL}	I_{SINK} = 2mA		85	150	mV
Off Leakage Current	PG_{IOH}	V_{PG} = 70V			2	μA

FUNCTIONAL BLOCK DIAGRAM

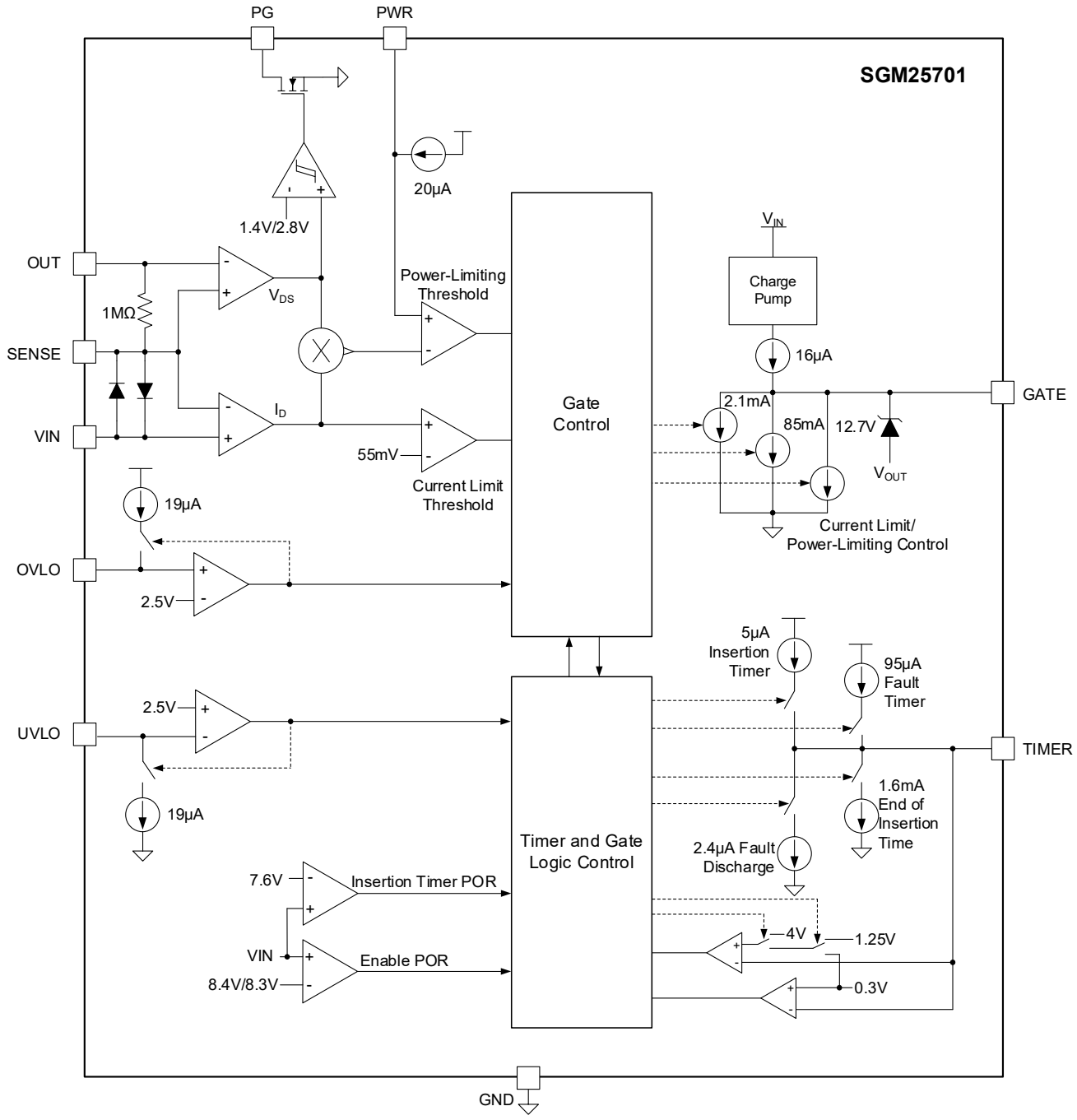
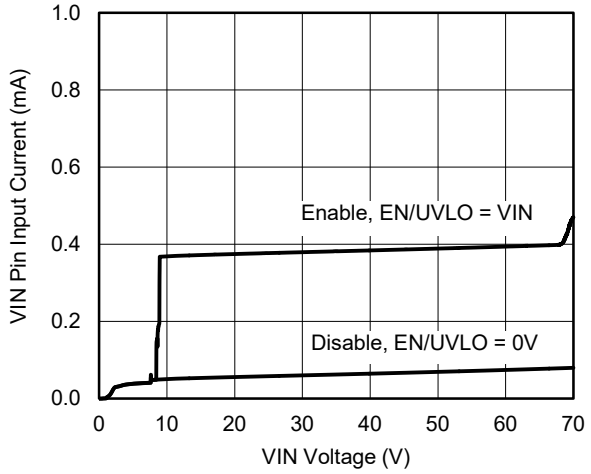


Figure 2. Block Diagram

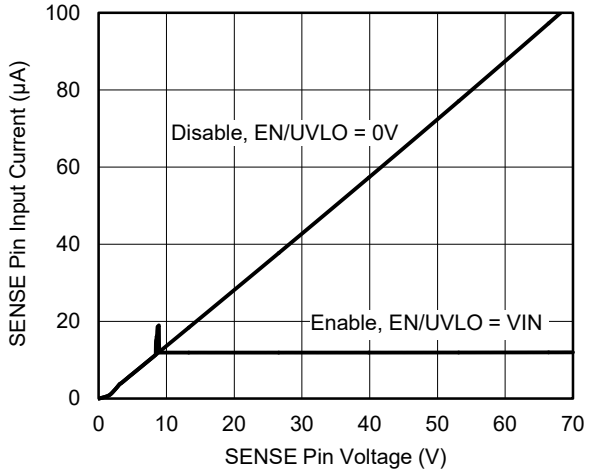
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃ and V_{IN} = 48V, unless otherwise noted.

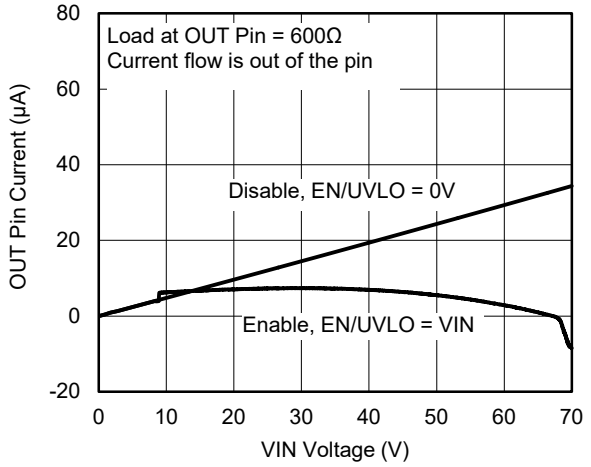
VIN Pin Input Current vs. VIN Voltage



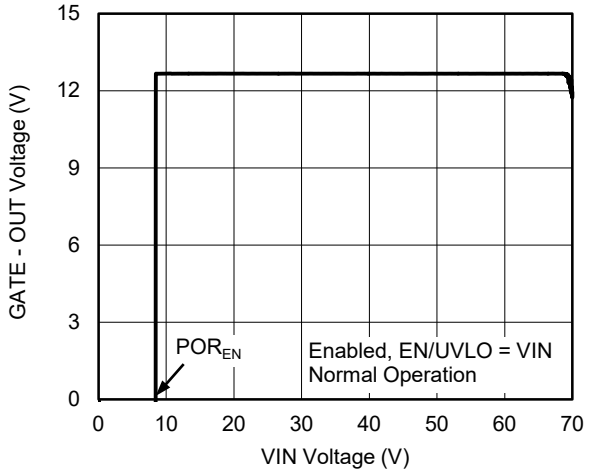
SENSE Pin Input Current vs. SENSE Pin Voltage



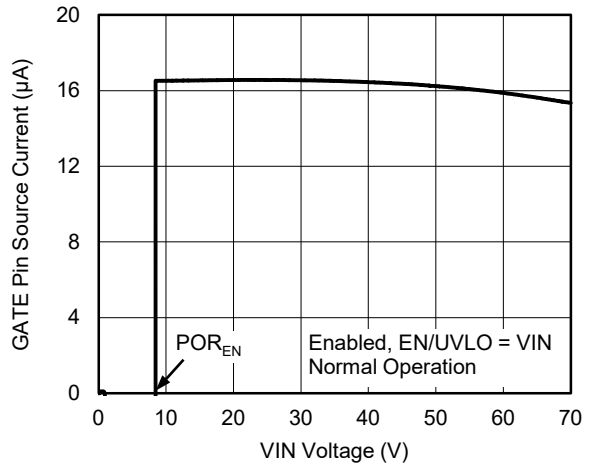
OUT Pin Current vs. VIN Voltage



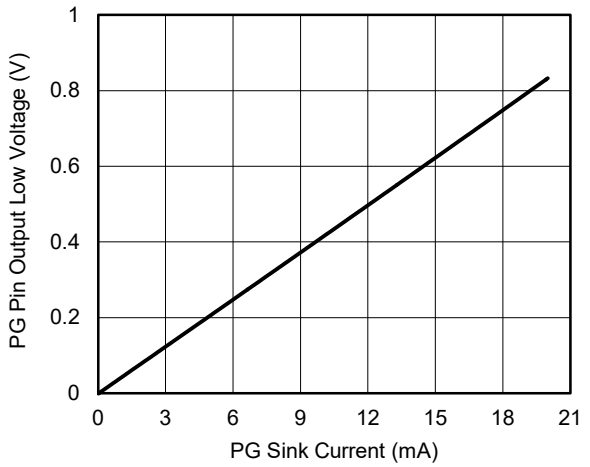
GATE Pin Voltage vs. VIN Voltage



GATE Pin Source Current vs. VIN Voltage



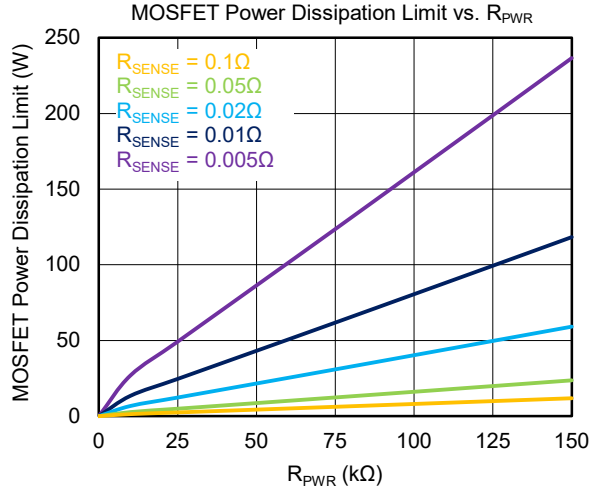
PG Pin Output Low Voltage vs. Sink Current



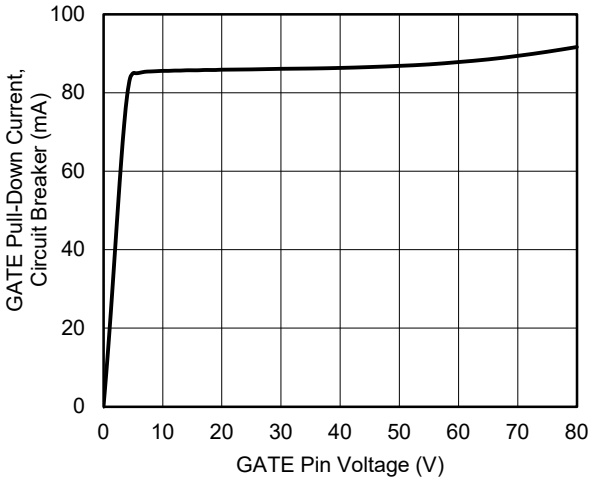
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_{IN} = 48V, unless otherwise noted.

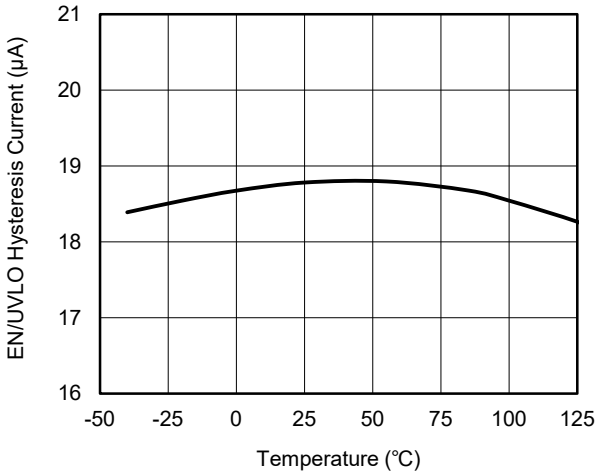
MOSFET Power Dissipation Limit vs. R_{PWR}



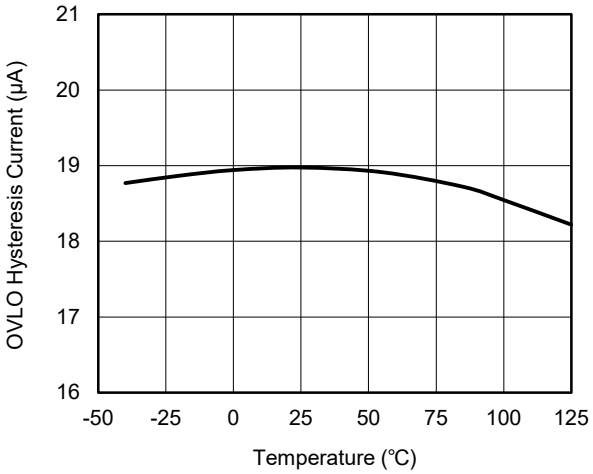
GATE Pull-Down Current, Circuit Breaker vs. GATE Pin Voltage



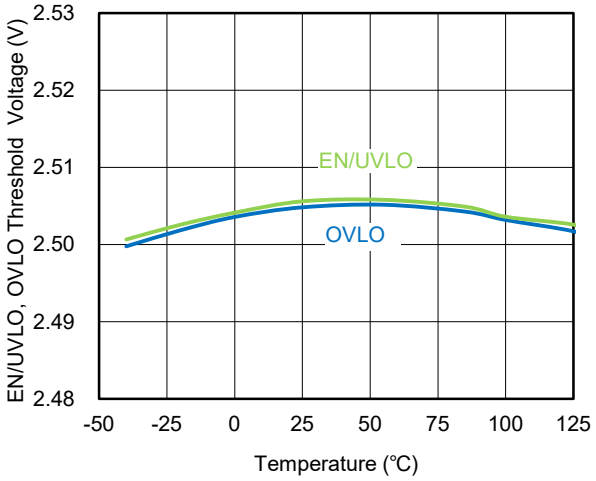
EN/UVLO Hysteresis Current vs. Temperature



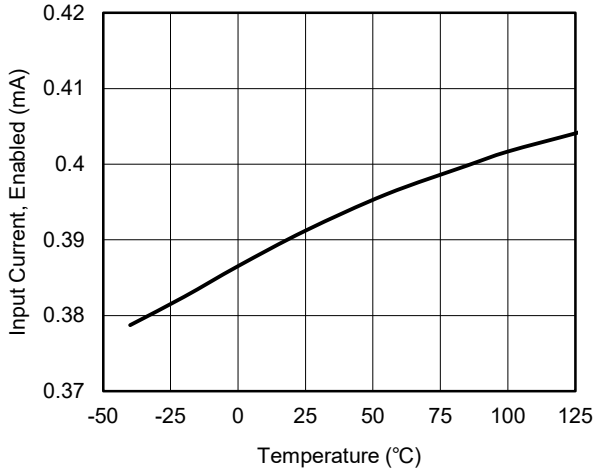
OVLO Hysteresis Current vs. Temperature



EN/UVLO, OVLO Threshold Voltage vs. Temperature



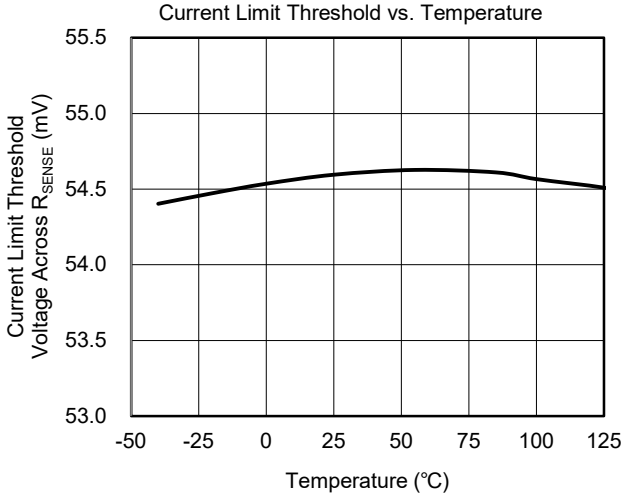
Input Current, Enabled vs. Temperature



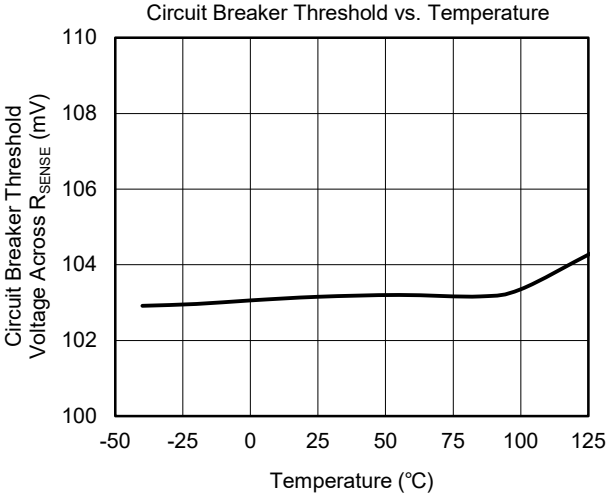
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_{IN} = 48V, unless otherwise noted.

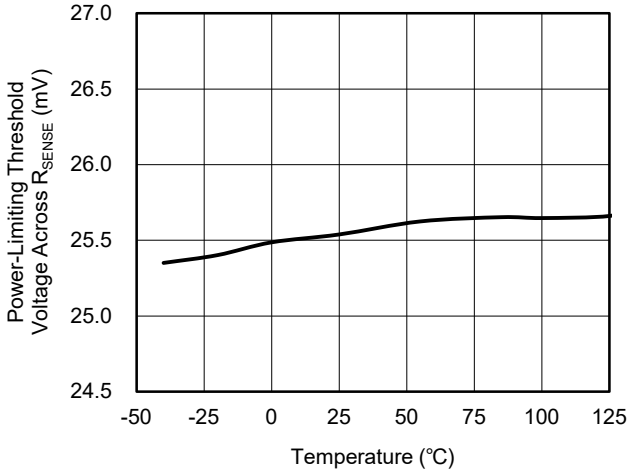
Current Limit Threshold vs. Temperature



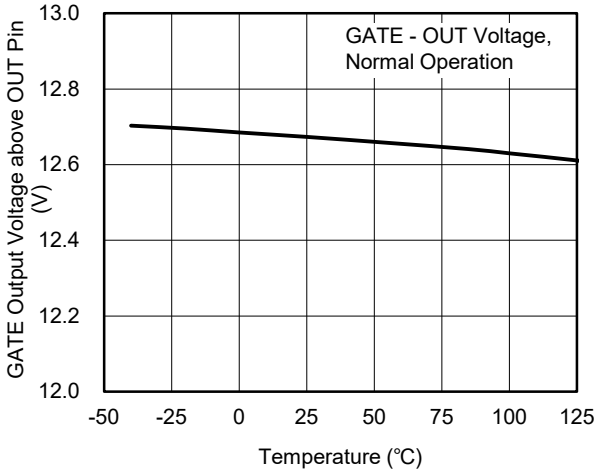
Circuit Breaker Threshold vs. Temperature



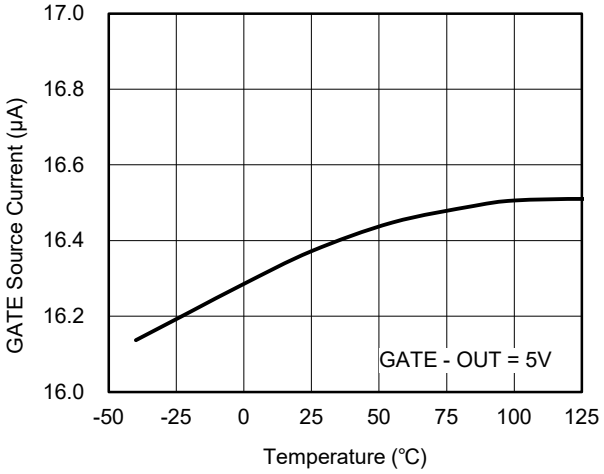
Power-Limiting Threshold vs. Temperature



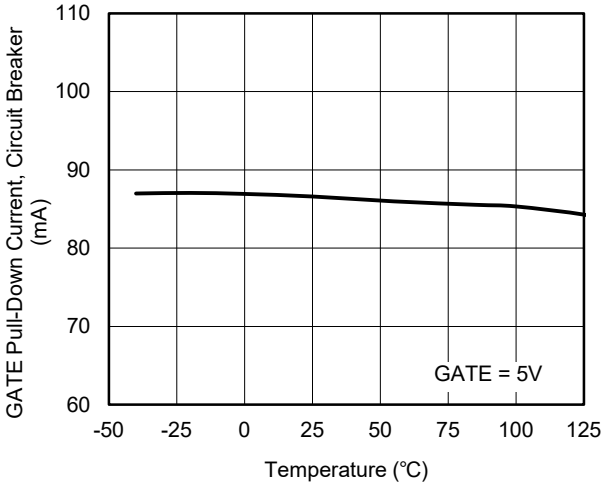
GATE Output Voltage vs. Temperature



GATE Source Current vs. Temperature

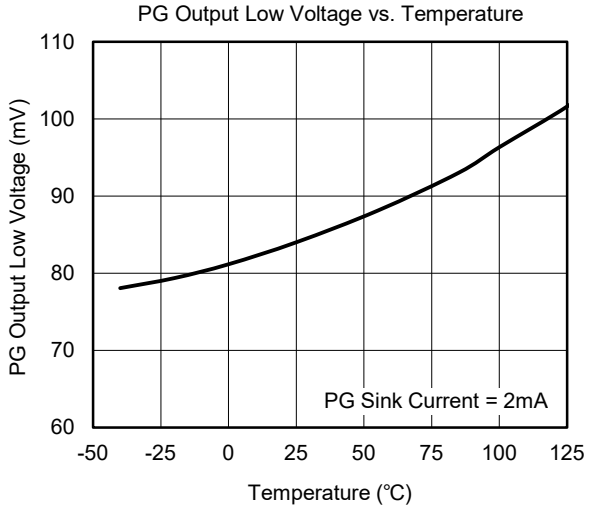


GATE Pull-Down Current, Circuit Breaker vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

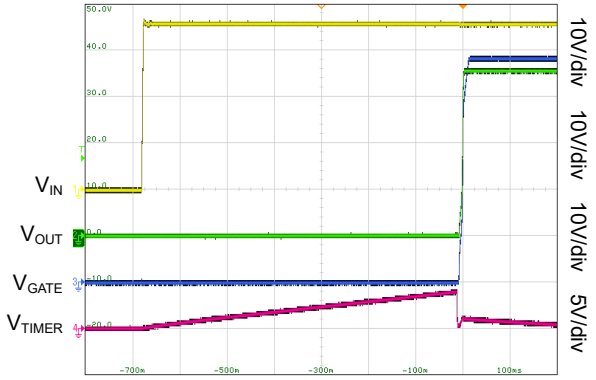
T_J = +25℃ and V_{IN} = 48V, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

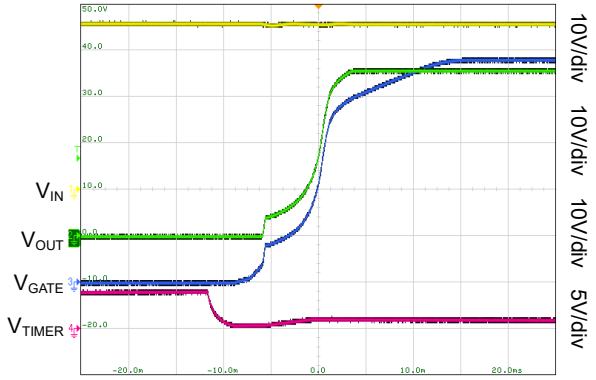
T_J = +25℃ and V_{IN} = 36V, unless otherwise noted.

Start-Up



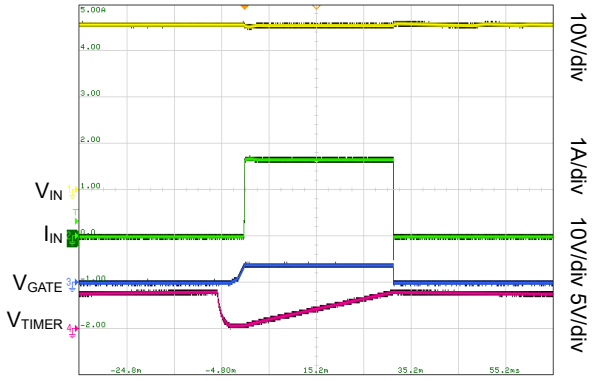
Time (100ms/div)

Start-Up (Zoomed In)



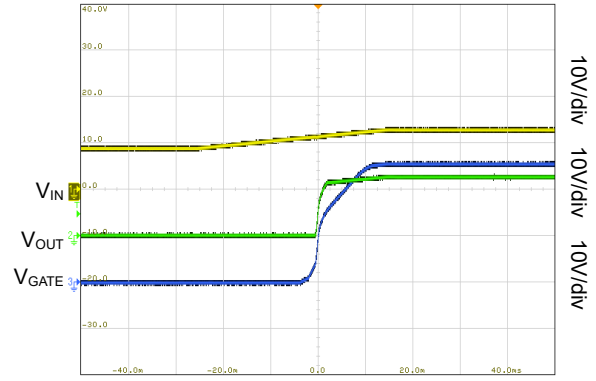
Time (5ms/div)

Start-Up into Short-Circuit



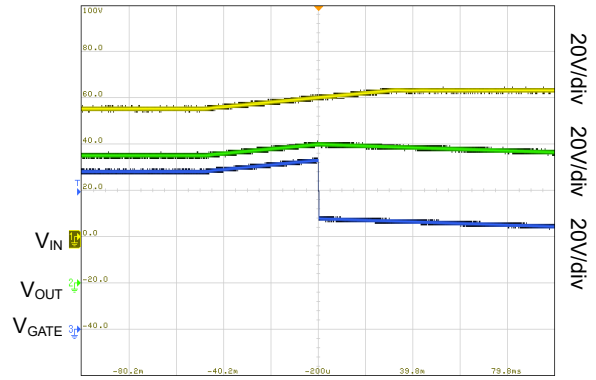
Time (10ms/div)

Under-Voltage Lockout



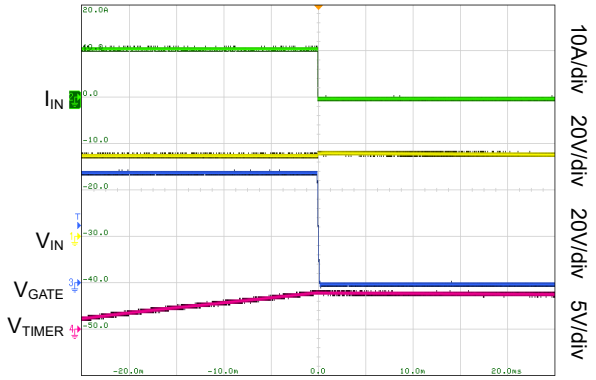
Time (10ms/div)

Over-Voltage Lockout



Time (20ms/div)

Gradual Over-Current

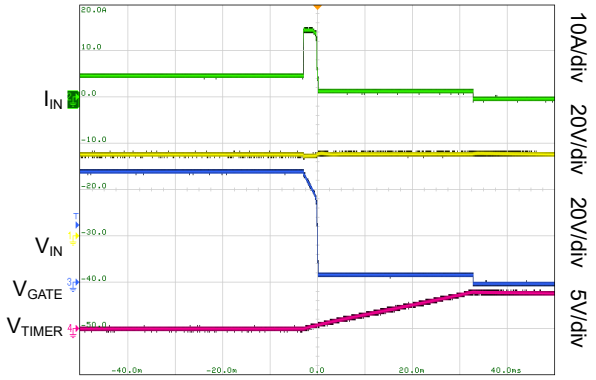


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

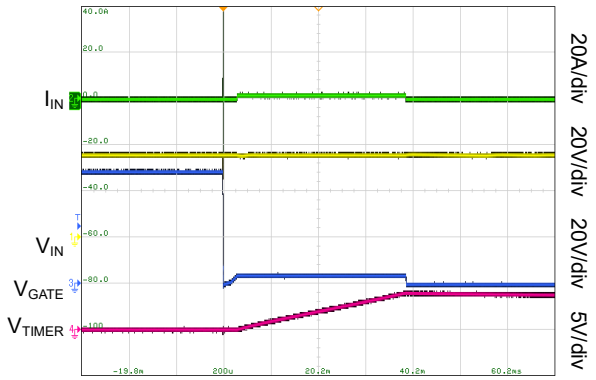
T_J = +25℃ and V_{IN} = 36V, unless otherwise noted.

Load Step



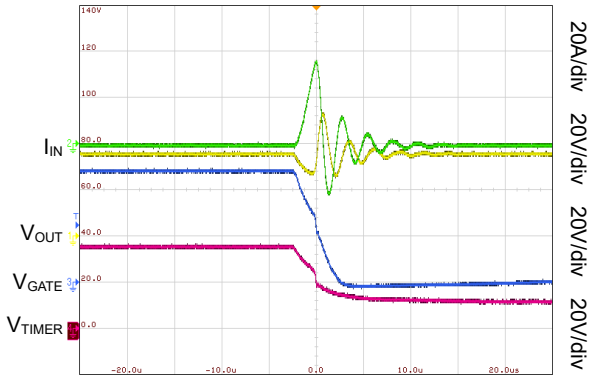
Time (10ms/div)

Hot-Short on Output



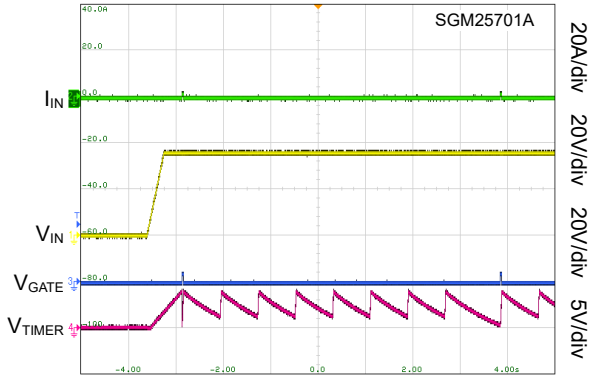
Time (10ms/div)

Hot-Short (Zoomed In)



Time (5μs/div)

Auto-Retry



Time (1s/div)

DETAILED DESCRIPTION

Overview

The SGM25701 is designed to limit the generated inrush current when the circuit card is plugged into and removed from the live backplane or hot power supply, reduce the voltage sag and dV/dt on the load during power-on, and avoid unnecessary reset and other impacts. The SGM25701 not only has current limit function, but also detects power dissipation when used in series to ensure the operations within SOA. Once the current limit or power-limiting exceeds the preset value, the SGM25701A components will repeatedly try to recover until the faults are removed, and the SGM25701B will latch off. When the input voltage range exceeds EN/UVLO and OVLO ranges, the device breaks during the period.

Current Limit

The device triggers over-current protection when the voltage on the R_{SENSE} reaches the current limit threshold of 55mV. In this event, the device limits the current in M_1 by controlling GATE pin, and the TIMER pin is active. If the current is lower than the threshold before the fault timeout period ends, the device recovers. Note that R_{SENSE} cannot be larger than 100mΩ.

Circuit Breaker

Once the load current rises rapidly, the current on R_{SENSE} may exceed the current limit value before the current limit control loop responds. When the current on R_{SENSE} exceeds two times the current limit value, M_1 is pulled down by the 85mA current source to turn off quickly, and the fault timeout starts timing until the voltage on R_{SENSE} drops below 105mV. If V_{TIMER} reaches 4V before current limit or power-limiting ceases, M_1 will be pulled off by the 2.1mA current source.

Power-Limiting

The power-limiting ensures that the power dissipation (MAX) of M_1 is within the SOA of the SGM25701. The device defines the power dissipation of the M_1 by sensing the V_{DS} of the M_1 and the drain current flowing through R_{SENSE}. The current and voltage values will be compared to the resistor that is used to program the power-limiting value on the PWR pin. The fault timer is activated if the power-limiting circuit is active.

EN/UVLO and OVLO

M_1 starts to work when the power supply voltage (V_{IN}) operates between the under-voltage lockout value and the over-voltage lockout value programmed by the resistor network (R_1, R_2, R_3 and R_4). When the input supply voltage is lower than the EN/UVLO threshold, the 19μA current sink inside the EN/UVLO is enabled, the current source inside the OVLO is turned off, and M_1 is kept off by the 2.1mA current source pull-down of the GATE pin. As the input supply voltage increases, when $V_{EN/UVLO}$ exceeds 2.5V, its internal 19μA current sink turns off to increase the EN/UVLO voltage, providing a threshold of hysteresis when M_1 is enabled by the 16μA current source at GATE pin. The EN/UVLO pin can be connected to VIN to set the minimum EN/UVLO level, when the V_{IN} reaches the power-on reset threshold (POR_{EN}), M_1 is enabled. When the power supply voltage rises so that the voltage on the OVLO pin exceeds 2.5V, M_1 is pulled down by the 2.1mA current source at GATE pin. At this time, the OVLO pin voltage is higher than 2.5V, the internal 19μA current source is turned on, and the V_{OVLO} is decreased to provide threshold hysteresis. Please refer to the application and implementation to calculate the resistance value of R_1 ~ R_4 to program the threshold.

DETAILED DESCRIPTION (continued)

Power Good Pin

The PG pin remains high during the turn-on period until the V_{IN} increases above ≅ 1V. At this time, as V_{IN} increases, PG continues to pull low. When the V_{OUT} increases to within 1.4V of the SENSE pin voltage, (V_{DS} < 1.4V), PG is switched high. If V_{DS} of M_1 increases above 2.8V, PG switches low. PG requires a pull-up resistor and the pull-up voltage (V_{PG}) may be as high as 70V for transient capability up to 80V. If PG requires a delay, please refer to Figure 3. Capacitor C_{PG} adds a delay to the rising edge in Figure 3 (1). The slew rate of the rising edge is determined by R_{PG1} + R_{PG2} and C_{PG}, and the slew rate of the falling edge is determined by R_{PG2} and C_{PG} in Figure 3 (2). Add a diode as shown in Figure 3 (3) to achieve an equal slope of rising edge and falling edge. For most applications, the typical values in Figure 3 (2) are recommended: R_{PG1} = 100kΩ, R_{PG2} = 0Ω, C_{PG} = 1μF.

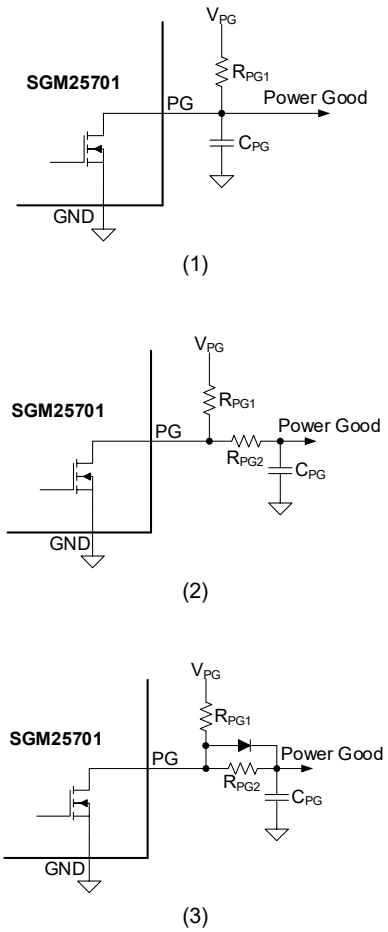


Figure 3. Adding Delay to the Power Good Output Pin

The SGM25701 has a power-up sequence that can be divided into 3 distinct parts: insertion time, inrush limit and normal operation. Once in normal operation, the TIMER and GATE pins depend on whether the output has a fault condition.

Power-Up Sequence

The SGM25701 has an input voltage range of 9V to 70V, and the transient input can reach 80V. Please refer to Figure 4 for details of this section. When the input voltage begins to increase, a strong pull-down 85mA current source inside the GATE pin prevents the Miller capacitance of the MOSFET from being charged. Furthermore, the TIMER pin is pulled low until the V_{IN} reaches the POR_{IT} threshold. At this time, between insertions, the C_{TIMER} begins to be charged by the internal 5μA current source when the M_1 is still turned off by the internal 2.1mA current source without being affected by V_{IN}. V_{IN} is allowed to stabilize gradually during the insertion time. When the voltage of the TIMER pin reaches 4V, the insertion time is over, and the charge on the C_{TIMER} is quickly discharged by the internal 1.6mA current source. After the insertion time, when the V_{IN} reaches the power-on reset threshold (POR_{EN}), the control circuit is enabled. If the input voltage exceeds the under-voltage lockout threshold, the 16μA current source inside the GATE pin starts to work and turns on M_1, and the V_{GS} of M_1 is limited to 12.7V by the internal Zener diode. When the OUT pin voltage increases, the SGM25701 detects the drain current and power dissipation of the M_1, and enables the current limit circuit and power-limiting circuit. During the inrush limit period, the C_{TIMER} is charged by the internal 95μA current source at the TIMER pin. If the power dissipation on M_1 and the input current decrease below their respective limit thresholds before the C_{TIMER} voltage value reaches 4V, the 95μA current source is turned off and the charge of the C_{TIMER} is discharged by the internal 2.4μA current sink.

When the OUT pin voltage increases to within 1.4V of the input voltage, the current limit interval is completed and the PG pin is pulled high. If the voltage of TIMER pin reaches 4V before the current limit or power-limiting ceases, the TIMER pin will be enabled and the GATE pin of M_1 will be pulled low by the internal 2.1mA current source and shut down until the next power-up sequence starts or the restart sequence ends.

DETAILED DESCRIPTION (continued)

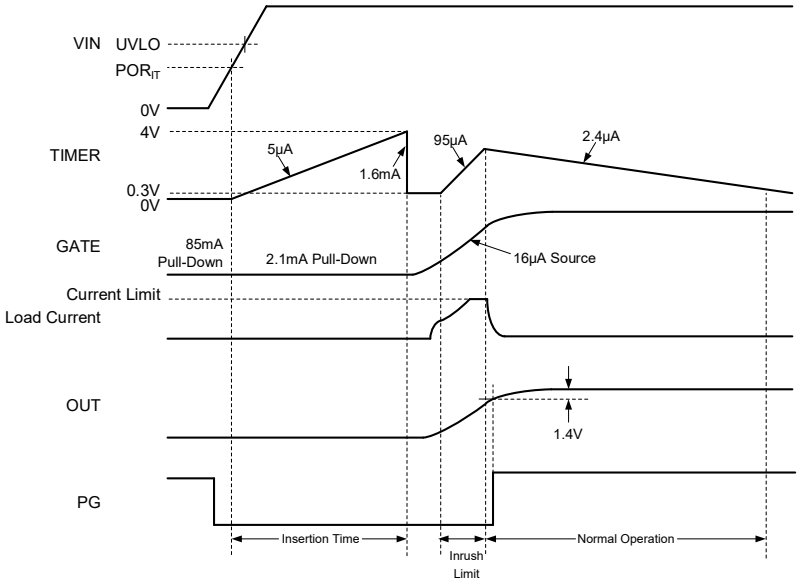


Figure 4. Power-Up Sequence (Power-Limiting Only)

Gate Control

An internal charge pump can provide an internal bias higher than the output voltage to boost the gate of the N-MOSFET. The V_{GS} of M_1 is limited to 12.7V by an internal Zener diode. During normal operation (see Figure 4), the GATE pin is charged to approximately 12.7V above the OUT pin by the internal 16μA current source. If the maximum gate-source voltage of the external N-MOSFET is less than 12.7V, a low voltage Zener diode with a forward current of at least 100mA must be added outside the device. A strong pull-down current source of 85mA for the initial operation of the device can prevent M_1 from being mis-turned through the drain-to-gate capacitance.

When the system is initially powered up, the GATE pin is pulled low by an internal 85mA current source to prevent misleading MOSFET on through the drain-gate capacitance. The GATE pin is pulled low by a 2.1mA current source in insertion time (see Figure 4) while the MOSFET is always turned off. During the following inrush limit time (see Figure 4), the voltage of the GATE pin is limited to the programmed current or power-limiting level when the TIMER pin is charged by the 95μA current source. If SGM25701 exits current limit or power-limiting state before the TIMER pin is charged to 4V, the circuit will enter normal operating mode and the TIMER will be discharged by the internal 2.4μA current. When the TIMER pin is charged to 4V, and the device is still in current limit or power-limiting state, the load cannot be started properly. The GATE will continue to be pulled down by the 2.1mA until the end of the restart sequence (SGM25701A) or the start sequence initialization (SGM25701B). The GATE pin is also pulled down by the 2.1mA current source when the supply voltage is lower than EN/UVLO threshold voltage or above OVLO threshold voltage. Please refer to Figure 5 for the detailed structure.

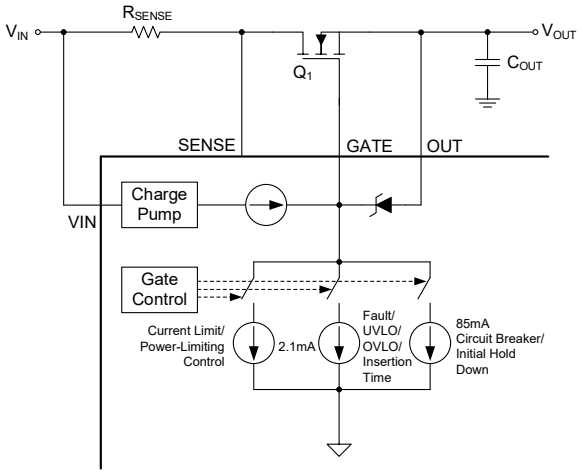


Figure 5. Gate Control

DETAILED DESCRIPTION (continued)

Shutdown Control

In addition, the remote control device can be turned off and safely started by connecting an open collector device or an open-drain device on the EN/UVLO pin, as shown in the Figure 6.

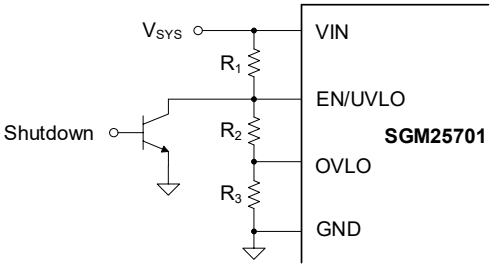


Figure 6. Shutdown Control

Fault Timer and Restart

When the current limit or power-limiting value is reached during the startup process, the GATE pin voltage is limited to regulate the load current and power dissipation. Then a 95μA current source will charge the TIMER, please refer to the Figure 8. If the current or power-limiting situation fades before the TIMER pin is charged to 4V, the device enters normal operation mode. Otherwise, the GATE pin of M_1 will be continuously pulled low by the 2.1mA current source. The TIMER pin is discharged by the 2.4μA current sink and enters a restart sequence of repeated charge and discharge (SGM25701A). After seven failure timeout cycles, the restart sequence ends when the voltage of the eighth descent ramp of the TIMER pin drops below 0.3V, and the 16μA current source of the GATE pin turns on M_1. If the fault persists, the restart sequence will be repeated.

The SGM25701B will latch the fault status after the fault detection timeout. The C_{TIMER} is discharged by a 2.4μA current sink. The GATE pin is pulled low by a 2.1mA current source until the power-up sequence is reset by cycling the input voltage, or the UVLO pin is momentarily pulled below 2.5V by a control signal, as shown in Figure 7. The voltage of the TIMER pin must be less than 0.3V to restart effectively.

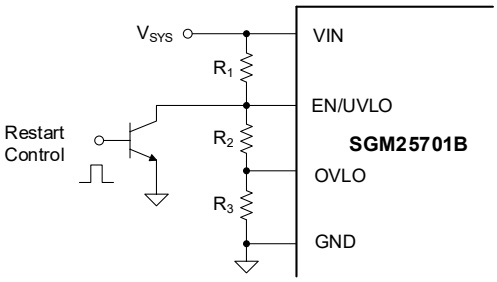


Figure 7. Latched Fault Restart Control

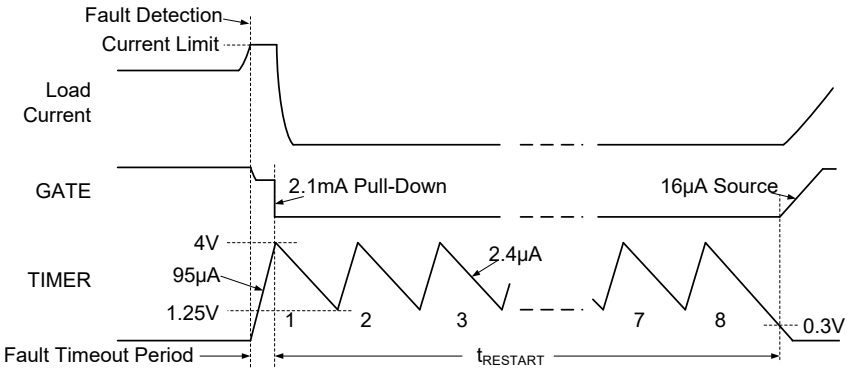


Figure 8. Restart Sequence (SGM25701A)

APPLICATION INFORMATION

The SGM25701 is a hot swap controller used for fault case protections and inrush current management. Consider startup, hot-short and start-into-short scenarios in detail before proceeding with applications.

In addition, for the safety of the equipment and systems, please carefully review the SOA (safe operating area) section of the choice of MOSFET. It is recommended to use the SGM25701 design calculator provided in the datasheet. The following design cases and calculation formulas can be used for reference.

Typical Application

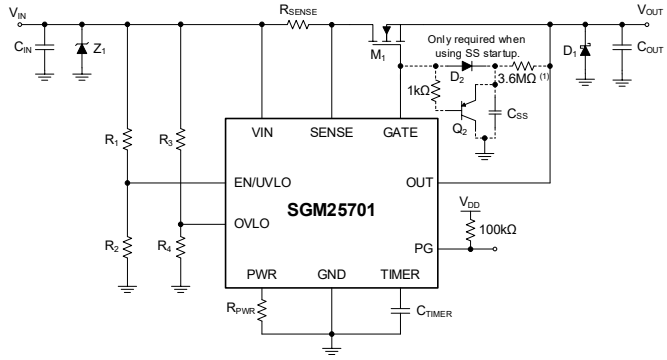


Figure 9. Typical Application Schematic (36V/11A)

Design Requirements

Table 1 lists the necessary parameters which are needed to know before designing. The power dissipation of the hot swap MOSFET during startup is stored in the output capacitor. Therefore, the V_{IN} and C_{OUT} value determine the stress of the MOSFET. The selection of sense resistor is determined by the maximum operating load current. Additionally, the maximum operating load current, ambient temperature, and thermal characteristics of the PCB ($R_{\theta CA}$), all affect the R_{DSON} requirements and the number of power MOSFETs used. The $R_{\theta CA}$ value is extremely sensitive to copper area and PCB layout. Note that the drain is not electrically grounded, so the ground plane does not help dissipate heat. The following example uses a value of 30℃/W, which is similar to SGM25701 EVB.

The test conditions for hot swap are needed to know before the test. The design must ensure that the MOSFET is safe even if the output is shorted. It is recommended not to carry the load until the MOSFET is successfully started. Loading the MOSFET too early may cause the startup failure.

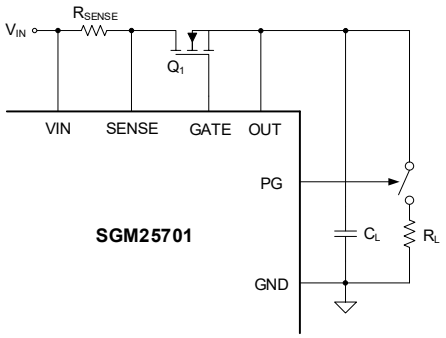


Figure 10. No Load Current during Turn-On

Table 1. Design Parameters

Parameter	Value
Input Voltage	24V to 48V
Operating Load Current (MAX)	11A
Lower EN/UVLO Threshold	22V
Upper EN/UVLO Threshold	24V
Lower OVLO Threshold	48V
Upper OVLO Threshold	50V
Load Capacitance (MAX)	1000μF
Ambient Temperature (MAX)	85℃
MOSFET $R_{\theta CA}$ (Function of Layout)	30℃/W
Pass Hot-Short on Output.	
Pass A Start into Short.	
The Load is Off until PG Asserted.	
A Hot Board cannot be Plugged Back in.	

APPLICATION INFORMATION (continued)

Detailed Design Procedure

Select R_{SENSE} and CL Setting

The device measures real-time current by monitoring the voltage across the R_{SENSE}. When the voltage across R_{SENSE} exceeds 55mV, the GATE pin is pulled low. Note the power and size of the R_{SENSE} and the selected over-current value. Use Equation 1 to calculate the appropriate sense resistance.

$$R_{SENSE} = \frac{V_{CL}}{I_{LIM}} = \frac{55mV}{11A} = 5m\Omega \quad (1)$$

Selecting the Hot Swap MOSFET(s)

Selecting the right MOSFET for hot swap applications is critical. Please ensure that the device meets the requirements as below:

- The V_{DS} of the MOSFET can withstand the maximum input voltage of the system along with the ringing introduced during transients.
- The SOA of the MOSFET can meet the following scenarios: startup, hot-short, and start-into-short.
- Try to keep the R_{DSON} as small as possible to avoid excessive temperature rise. It recommends a steady state of less than +125℃ for MOSFETs.
- The maximum continuous current must be greater than the maximum load current, and the drain pulse current must be greater than the threshold current of the circuit breaker.

For the design, the KNB2710A is selected. The maximum steady state case temperature can be calculated as Equation 2 after selecting the MOSFET.

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DSON,MAX}(T_J) \quad (2)$$

Note that R_{DSON} is a strong function of junction temperature. According to the KNB datasheet, R_{DSON} is about 1.4× at 85℃. Equation 3 is used to calculate $T_{C,MAX}$.

$$T_{C,MAX} = 85℃ + 30℃/W \times (11A)^2 \times (1.4 \times 4.5m\Omega) = 107.87℃ \quad (3)$$

If the calculated temperature value of a single MOSFET is too high, the power dissipation can be dispersed by increasing the number of MOSFETs.

When using multiple MOSFETs in parallel, please use Equation 4 as below.

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times (\frac{I_{LOAD,MAX}}{\#\ of\ MOSFETs})^2 \times R_{DSON}\ (T_J) \quad (4)$$

Select Power-Limiting

It is usually best to use power-limiting to reduce stress on the MOSFET. However, when the power-limiting is set very low and the current flowing through the MOSFET is controlled, the voltage across the R_{SENSE} will very low. Equation 5 can be used to calculate the voltage across the R_{SENSE}.

$$V_{SENSE} = \frac{P_{LIM} \times R_{SENSE}}{V_{DS}} \quad (5)$$

V_{SENSE} below 5mV is not recommended to avoid low power-limiting accuracy. In this application, it can use Equation 6 to calculate the corresponding power-limiting value.

$$P_{LIM,MIN} = \frac{V_{SENSE,MIN} \times V_{IN,MAX}}{R_{SENSE}} = \frac{5mV \times 48V}{5m\Omega} = 48W \quad (6)$$

It can further calculate the corresponding minimum R_{PWR} at this power-limiting according to Equation 7.

$$R_{PWR} = 1.30 \times 10^5 \times R_{SENSE} \times (P_{LIM} - 1.18mV \times \frac{V_{DS}}{R_{SENSE}}) \quad (7)$$

Note that the minimum R_{PWR} corresponds to the V_{DS} = $V_{IN,MAX}$. It can be calculated by Equation 8.

$$R_{PWR} = 1.30 \times 10^5 \times 5m\Omega \times (48W - 1.18mV \times \frac{48V}{5m\Omega}) = 24k\Omega \quad (8)$$

For a more accurate power-limiting, select a power-limiting value lager than 48W. It can use a slightly larger resistance of 33kΩ, which sets a power-limiting of 62.1W.

APPLICATION INFORMATION (continued)

Set Fault Timer

Please ensure that the fault timer has enough time to ensure that it does not time out in the power-limiting or current limit operation during this period. If the device is running in current limit state from the start, the maximum startup time can be calculated by Equation 9.

$$t_{START,MAX} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM}} \quad (9)$$

For this example, the device enters a conversion from power-limiting to current limit during startup. The startup time can be estimated according to Equation 10.

$$t_{START} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN,MAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2} \right] = \frac{1000\mu F}{2} \times \left[\frac{(48V)^2}{62.1W} + \frac{62.1W}{(11A)^2} \right] = 18.81ms \quad (10)$$

Please note that the time calculated above is the ideal constant power conversion to constant current startup. Because power-limiting is a function of V_{DS}, the actual startup time will be longer than calculated time. In addition, it needs to consider errors introduced by some device specifications, such as C_{TIMER} and constant current source, power-limiting value, etc., and also needs an additional 50% time margin to ensure that the startup time does not time out. Therefore, use Equation 11 to determine the value of the fault timer capacitance.

$$C_{TIMER} = \frac{t_{FLT} \times I_{TIMER(TYP)}}{V_{TIMER(TYP)}} \times 1.5 = \frac{18.81ms \times 95\mu A}{4V} \times 1.5 = 670nF \quad (11)$$

The capacitor of 680nF with a slightly larger capacitance can be selected to calculate the programming time of the fault timer according to Equation 12.

$$t_{FLT} = \frac{C_{TIMER} \times V_{TIMER,TYP}}{I_{TIMER,TYP}} = \frac{680nF \times 4V}{95\mu A} = 28.6ms \quad (12)$$

If the system has not started successfully beyond this time, the SGM25701 will shut down the KNB2710A MOSFET.

Check MOSFET SOA

Once the power-limiting and timer capacitance values are selected, it is important to confirm the SOA characteristics of the MOSFET. SOA characteristics describe how long a MOSFET can safely operate at a certain current under a V_{DS}. In the worst case, the MOSFET operates in a power-limiting state all the time. The current flowing value is $P_{LIM}/V_{IN,MAX}$ and the duration is t_{FLT}. Taking this application as an example, it must ensure that the MOSFET may handle 1A at 48V for 28.9ms. Based on the SOA of the KNB2710A, it can handle 48V, 19A for 1ms and it can handle 48V, 5A for 100ms. Refer to Equations 13 to 15 to calculate the corresponding safe working period.

$$I_{SOA}(t) = a \times t^m \quad (13)$$

$$m = \frac{\ln \frac{I_{SOA}(t_1)}{I_{SOA}(t_2)}}{\ln(\frac{t_1}{t_2})} = \frac{\ln(\frac{19A}{5A})}{\ln(\frac{1ms}{100ms})} = -0.29 \quad (14)$$

$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{19A}{(1ms)^{-0.29}} = 19A \times (1ms)^{0.29} \quad (15)$$

$$I_{SOA}(28.9ms) = 19A \times (1ms)^{0.29} \times (28.9ms)^{-0.29} = 7.163A \quad (16)$$

Note that the current calculated above is an ideal calculation considering the MOSFET case temperature to be +25℃. A certain ambient temperature and thermal increase during operation can make the MOSFET more possible to hot-short. It can use Equation 17 to calculate the approximate current.

$$I_{SOA}(28.9ms, T_{C,MAX}) = I_{SOA}(28.9ms, 25℃) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{I_{J,ABSMAX} - 25℃} = 7.163A \times \frac{175℃ - 107.87℃}{175℃ - 25℃} = 3.21A \quad (17)$$

Based on this calculation, the MOSFET can handle 3.21A, 48V for 28.9ms at elevated case temperature. This value is larger than the 1.29A required for power-limiting startup, indicating that there is little risk of hot-short to the MOSFET during startup. It is recommended that the selected MOSFET may calculate an equivalent current value that exceeds the required value by 1.3× to provide sufficient margin.

APPLICATION INFORMATION (continued)

Set Under-Voltage and Over-Voltage Threshold

By setting the EN/UVLO and OVLO thresholds, SGM25701 turns on the main power MOSFET M_1 when the input voltage is within the normal operating range. Conversely, M_1 switches off, stopping the output current.

The four thresholds can be accurately calculated using the configuration shown in Figure 11.

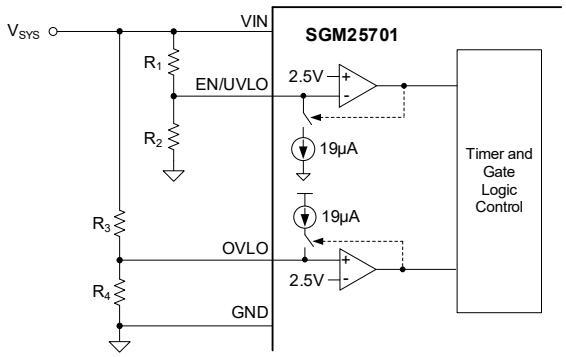


Figure 11. Programming the Four Thresholds

Use the following Equations 18 and 19 to calculate the upper and lower threshold of EN/UVLO.

$$R_1 = \frac{V_{UVH} - V_{UVL}}{19\mu A} = \frac{V_{UV(HYS)}}{19\mu A} \quad (18)$$

$$R_2 = \frac{2.5V \times R_1}{(V_{UVL} - 2.5V)} \quad (19)$$

Use the following Equations 20 and 21 to calculate the upper and lower threshold of OVLO.

$$R_3 = \frac{V_{OVH} - V_{OVL}}{19\mu A} = \frac{V_{OV(HYS)}}{19\mu A} \quad (20)$$

$$R_4 = \frac{2.5V \times R_3}{(V_{OVH} - 2.5V)} \quad (21)$$

V_{UVH} = 24V, V_{UVL} = 22V, V_{OVH} = 50V, and V_{OVL} = 48V. Therefore, $V_{UV(HYS)}$ = 2V and $V_{OV(HYS)}$ = 2V.

The resistor values are: R_1 = 100kΩ, R_2 = 13kΩ, R_3 = 100kΩ, and R_4 = 5.6kΩ.

Under the condition that R_1 - R_4 is calculated, the threshold voltage and hysteresis voltage are calculated using Equation 22 to Equation 27.

$$V_{UVH} = 2.5V + [R_1 \times (\frac{2.5V}{R_2} + 19\mu A)] \quad (22)$$

$$V_{UVL} = \frac{2.5V \times (R_1 + R_2)}{R_2} \quad (23)$$

$$V_{UV(HYS)} = R_1 \times 19\mu A \quad (24)$$

$$V_{OVH} = \frac{2.5V \times (R_3 + R_4)}{R_4} \quad (25)$$

$$V_{OVL} = 2.5V + [R_3 \times (\frac{2.5V}{R_4} - 19\mu A)] \quad (26)$$

$$V_{OV(HYS)} = R_3 \times 19\mu A \quad (27)$$

Input and Output Protection

The SGM25701 needs to connect voltage clamping devices on the input side under hot plug conditions. It is necessary to select an appropriate TVS as shown in Figure 1. When the hot plug circuit is suddenly pulled out of the socket under the load condition, TVS needs to suppress the voltage surge at this time. The principle of TVS selection is that there is a small leakage current at $V_{IN(MAX)}$, and it is clamped below the set voltage when the input surge voltage is large.

Component Values

Table 2 provides the selected device values under the condition of 36V/11A, and the application curve is also based on these device values.

Table 2. Component Values

Component	Value
R_{SENSE}	5mΩ
R_1	100kΩ
R_2	13kΩ
R_3	100kΩ
R_4	5.6kΩ
R_{PWR}	33kΩ
M_1	KNB2710A
Z_1	SMBJ70A-13-F
D_1	MBRS3100T3G
C_{TIMER}	680nF
C_{OUT}	1000μF

APPLICATION INFORMATION (continued)

Power Supply Recommendations

Generally speaking, SGM25701 can provide stable power supply with reliable performance. However, when other card slots on the backplane are inserted, the high frequency dynamics on the backplane will appear. When this happens in the system, it is recommended to place a capacitor of 1μF on the drain of MOSFET. This will reduce the common mode voltage between VIN and SENSE pins, which needs to be suppressed to prevent over-current shutdown.

PC Board Guidelines

SGM25701 should observe the following principles when laying PCB:

SGM25701 needs to be placed near the input connector to reduce the lead inductance from the connector to the power MOSFET.

The bypass capacitor of V_{IN} should be placed carefully. When MOSFET is turned off due to short-circuit, the input terminal has a very large dV/dt. When the capacitor is placed close to the VIN pin, the LC filter is formed due to the long routing from SENSE to VIN. At this time, a large voltage difference may be formed between VIN and SENSE. To prevent this, place the capacitor on the R_{SENSE} terminal instead of VIN terminal.

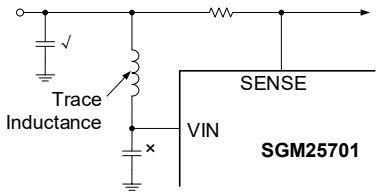


Figure 12. Layout Trace Inductance

- The R_{SENSE} needs to be close to the controller chip and use the Kelvin connection.
- The current path and return path from the input to the load side should be parallel and close to each other to reduce the loop inductance.
- GND of components around SGM25701 can be connected with each other and connected with GND pin of SGM25701. Then connect GND to the system ground uniformly. Do not separately connect the ground of the devices around the chip to the ground of the system with high current.
- PCB layout provides good heat dissipation conditions for MOSFET M_1 to reduce the junction temperature when it is turned on and off.

System Considerations

As shown in Figure 13, the normal operation of SGM25701 requires a capacitor on the backplane side. The capacitor with live backplane needs to absorb the input surge voltage generated when the controller cuts off the load. If there is no capacitance, TVS needs to be placed in the input measurement to prevent large voltage generated during voltage transient from exceeding the maximum rated value of VIN pin.

When the output of SGM25701 is inductive load, it is necessary to reverse parallel diode on the load side. When the load is cut off, a reverse path is provided for the current of the inductive load to prevent negative voltage from damaging the device.

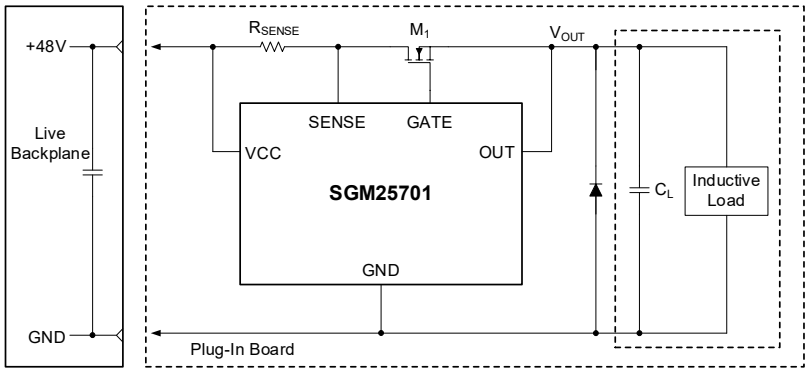


Figure 13. Output Diode Required for Inductive Loads

REVISION HISTORY

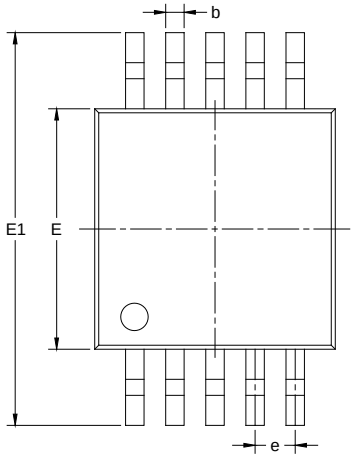
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

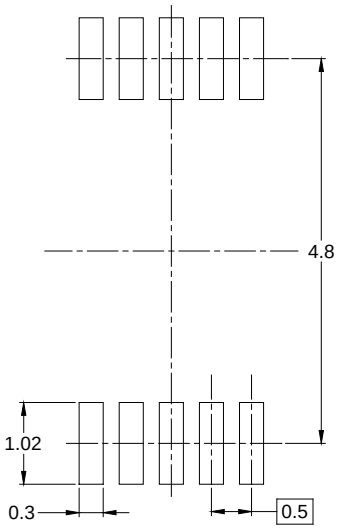
FEBRUARY 2023 – REV.A to REV.A.1	Page
Added SGM25701B Model	All

Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

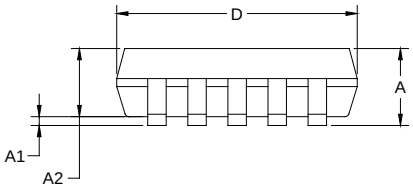
PACKAGE OUTLINE DIMENSIONS

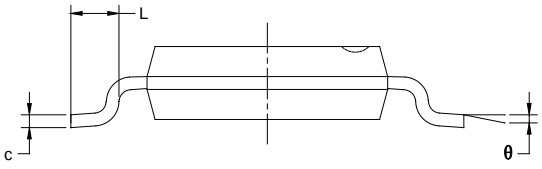
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



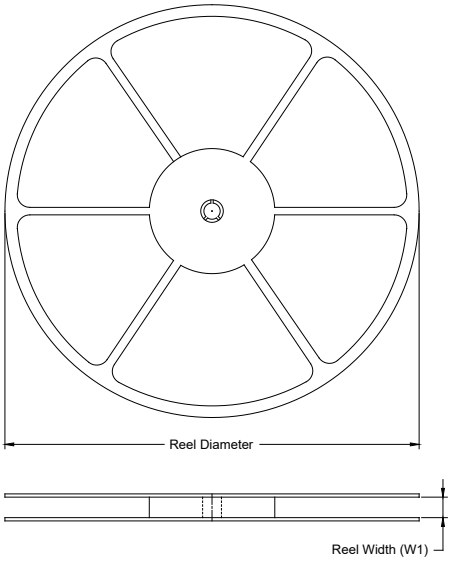


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

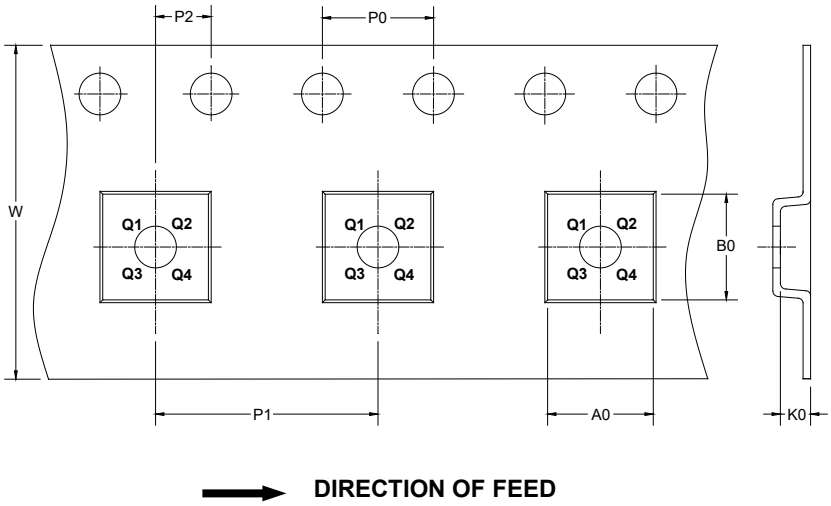
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

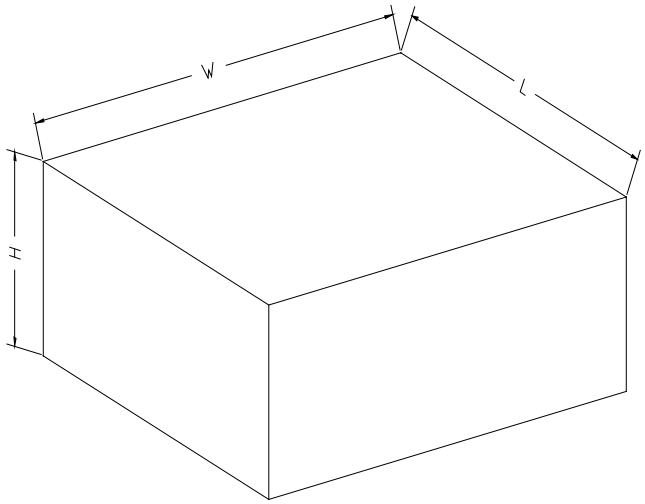
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002