

# AOCA32116E

20V Common-Drain Dual N-Channel MOSFET

## General Description

- Trench Power MOSFET technology
- Ultra low  $R_{SS(ON)}$
- Common drain configuration for design simplicity
- RoHS and Halogen-Free Compliant

## Product Summary

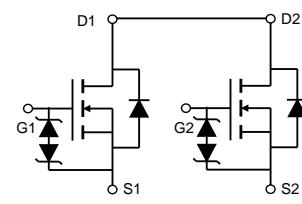
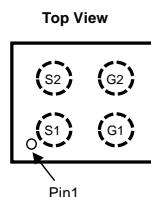
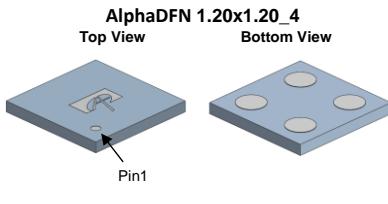
$V_{SS}$	20V
$R_{SS(ON)}$ (at $V_{GS}=4.5V$ )	< 36mΩ
$R_{SS(ON)}$ (at $V_{GS}=3.8V$ )	< 39mΩ
$R_{SS(ON)}$ (at $V_{GS}=3.1V$ )	< 44mΩ
$R_{SS(ON)}$ (at $V_{GS}=2.5V$ )	< 55mΩ

## Applications

- Battery protection switch
- Mobile device battery charging and discharging

## Typical ESD protection

HBM Class 2



## Orderable Part Number

Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOCA32116E	AlphaDFN 1.20x1.20_4	Tape & Reel	8000

## Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Rating	Units
Source-Source Voltage	$V_{SS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Source Current(DC) <sup>Note1</sup>	$I_S$   $T_A=25^\circ C$	6	A
Source Current(Pulse) <sup>Note2</sup>	$I_{SM}$	25	
Power Dissipation <sup>Note1</sup>	$P_D$   $T_A=25^\circ C$	1.7	W
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C

## Thermal Characteristics

Parameter	Symbol	Typical	Units
Maximum Junction-to-Ambient   $t \leq 10s$	$R_{JJA}$	65	°C/W
Maximum Junction-to-Ambient   Steady-State		75	°C/W

**Note 1.**  $I_S$  rated value is based on bare silicon. Mounted on 70mmx70mm FR-4 board.

**Note 2.** PW <10  $\mu s$  pulses, duty cycle 1% max.

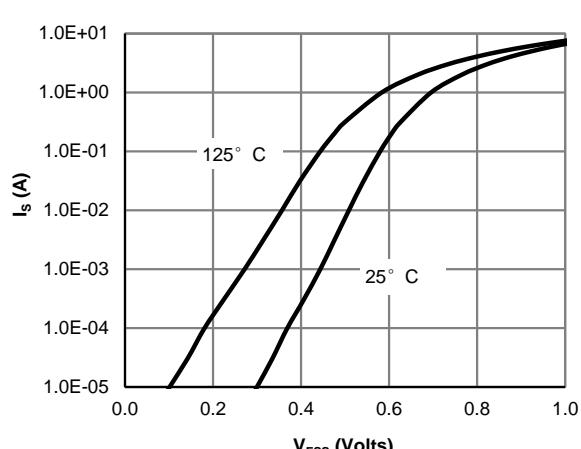
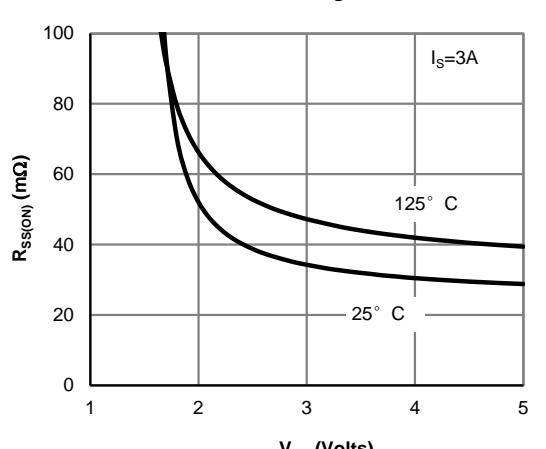
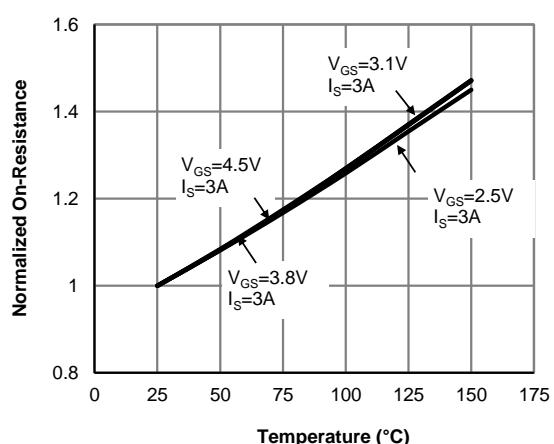
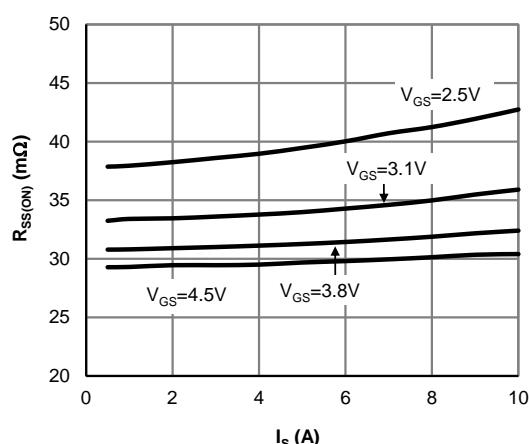
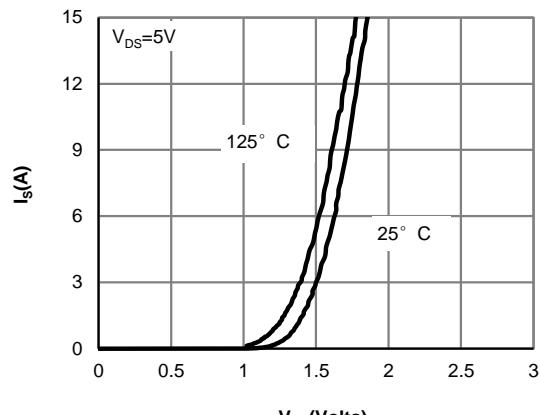
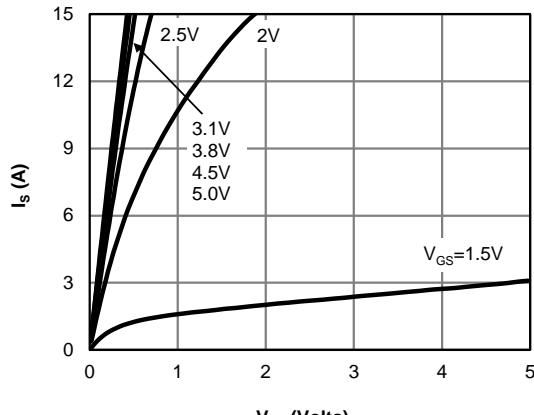
**Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$\text{BV}_{\text{SSS}}$	Source-Source Breakdown Voltage	$I_S=250\mu\text{A}, V_{GS}=0\text{V}$	Test Circuit 6	20		V
$I_{\text{SSS}}$	Zero Gate Voltage Source Current	$V_{SS}=20\text{V}, V_{GS}=0\text{V}$	Test Circuit 1		1	$\mu\text{A}$
				$T_J=55^\circ\text{C}$		5
$I_{GSS}$	Gate leakage current	$V_{SS}=0\text{V}, V_{GS}=\pm 12\text{V}$	Test Circuit 2			$\pm 10 \mu\text{A}$
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{SS}=V_{GS}, I_S=250\mu\text{A}$	Test Circuit 3	0.5	0.85	1.3
				$V_{GS}=4.5\text{V}, I_S=3\text{A}$	20	29.5
					28	36
					$T_J=125^\circ\text{C}$	50
$R_{SS(\text{ON})}$	Static Source to Source On-Resistance	$V_{GS}=3.8\text{V}, I_S=3\text{A}$	Test Circuit 4	21	31	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=3\text{A}$	Test Circuit 4	23	33.6	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_S=3\text{A}$	Test Circuit 4	26	38.6	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{SS}=5\text{V}, I_S=3\text{A}$	Test Circuit 3		20	S
$V_{FSS}$	Forward Source to Source Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$	Test Circuit 5		0.68	V
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}, V_{SS}=10\text{V}, f=1\text{MHz}$		410	520	$\text{pF}$
$C_{oss}$	Output Capacitance			50	72	$\text{pF}$
$C_{rss}$	Reverse Transfer Capacitance			14	48	$\text{pF}$
$R_g$	Gate resistance	$f=1\text{MHz}$			2	$\text{K}\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g$	Total Gate Charge	$V_{G1S1}=4.5\text{V}, V_{SS}=10\text{V}, I_S=3\text{A}$			5.5	$\text{nC}$
$t_{D(on)}$	Turn-On Delay Time	$V_{G1S1}=4.5\text{V}, V_{SS}=10\text{V}, R_L=3.3\Omega, R_{GEN}=3\Omega$			0.5	$\mu\text{s}$
$t_r$	Turn-On Rise Time				1.4	$\mu\text{s}$
$t_{D(off)}$	Turn-Off Delay Time		Test Circuit 8		1.9	$\mu\text{s}$
$t_f$	Turn-Off Fall Time				2.7	$\mu\text{s}$

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### TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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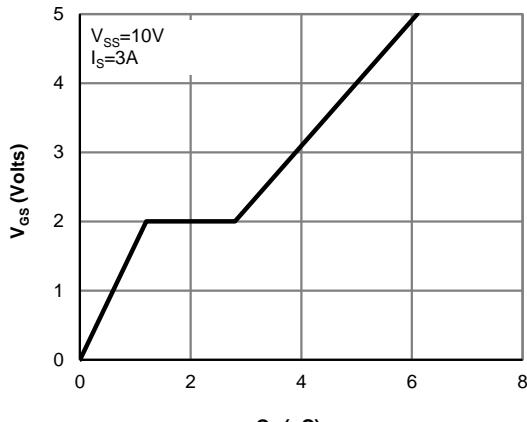


Figure 7: Gate-Charge Characteristics

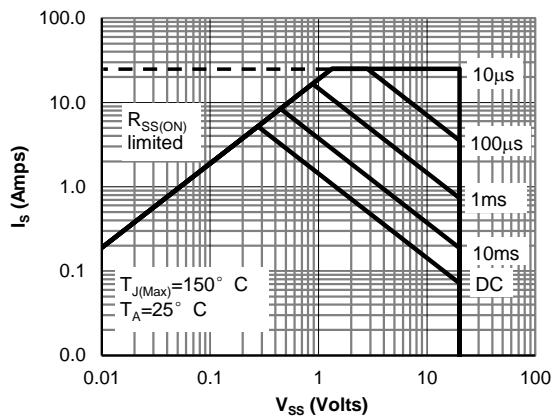


Figure 8: Maximum Forward Biased Safe Operating Area (Note1)

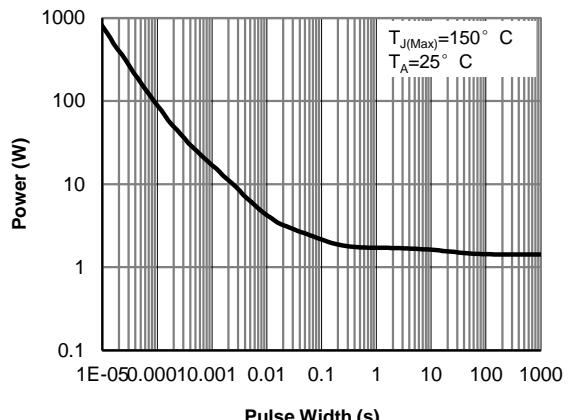


Figure 9: Single Pulse Power Rating Junction-to-Ambient (Note1)

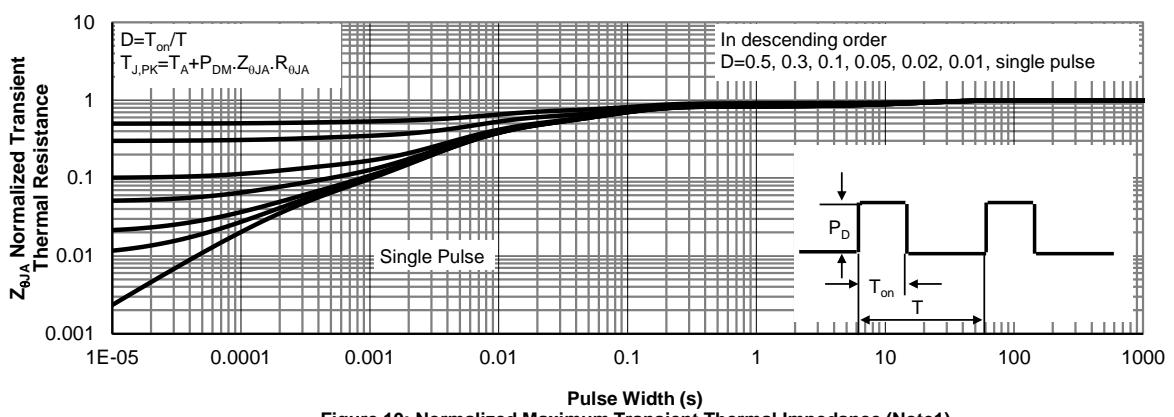
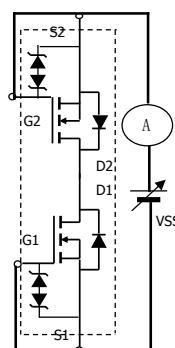
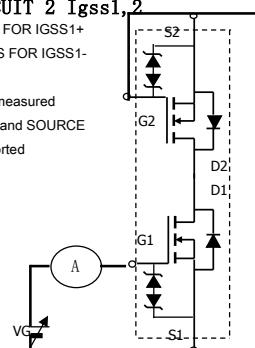


Figure 10: Normalized Maximum Transient Thermal Impedance (Note1)

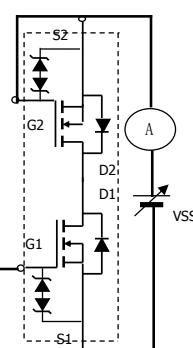
**TEST CIRCUIT 1 Isss**  
POSITIVE VSS FOR ISSS+  
NEGATIVE VSS FOR ISSS-



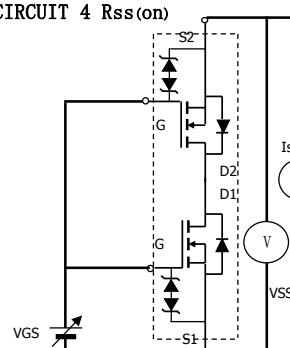
**TEST CIRCUIT 2 Igss1,2**  
POSITIVE VGS FOR IGSS1+  
NEGATIVE VGS FOR IGSS1-

**TEST CIRCUIT 3 Vgs(off)**

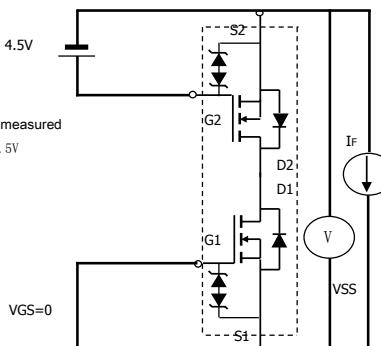
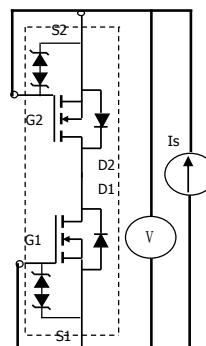
When FET1 is measured  
between GATE and SOURCE  
of FET2 are shorted

**TEST CIRCUIT 4 Rss(on)**

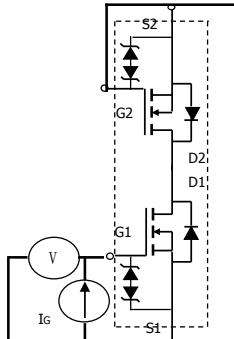
Vss/Is

**TEST CIRCUIT 5 VF(ss)1,2**

When FET1 measured  
FET2 VGS=4.5V

**TEST CIRCUIT 6 BVdss**POSITIVE VSS FOR ISSS+  
NEGATIVE VSS FOR ISSS-**TEST CIRCUIT 7 BVgs01,2**  
POSITIVE VSS FOR ISSS+  
NEGATIVE VSS FOR ISSS-

When FET1 is measured  
between GATE and SOURCE  
of FET2 are shorted

**TEST CIRCUIT 8**  
Switching time