FC6B21150L

Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

■ Features

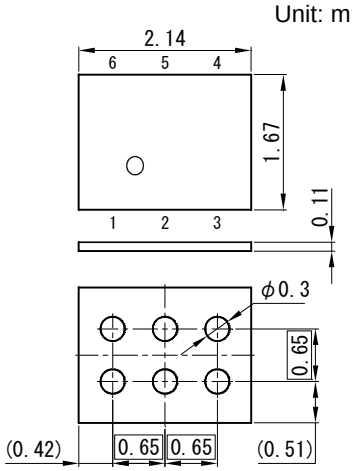
- Low source-source ON resistance:Rss(on) typ. = 4.0 mΩ（VGS = 4.5 V)
- CSP（Chip Size Package)
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

■ Marking Symbol: 16

■ Packaging

Embossed type (Thermo-compression sealing) : 10 000 pcs / reel (standard)

Unit: mm



1. Source1-1 (FET1)
2. Gate1 (FET1)
3. Source1-2 (FET1)
4. Source2-1 (FET2)
5. Gate2 (FET2)
6. Source2-2 (FET2)

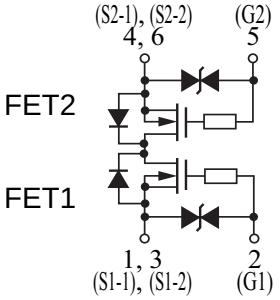
Panasonic	MLGA006-W-1721-RA
JEITA	—
Code	—

■ Absolute Maximum Ratings Ta = 25 °C

Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	12	V
Gate-source Voltage *3		VGS	±10.5	V
Source Current	DC *1	IS1	8	A
	DC *2	IS2	17	A
	Pulse *3	ISp	80	A
Total Power Dissipation	DC *1	PD1	0.45	W
	DC *2	PD2	2.1	W
Channel Temperature		Tch	150	°C
Storage Temperature Range		Tstg	-55 to +150	°C
Thermal resistance (ch-a)	DC *1	Rth1	278	°C/W
	DC *2	Rth2	59	°C/W

Note *1 Mounted on FR4 board
(25.4mm × 25.4mm × t1.0mm, 36μm Copper)
*2 Mounted on Ceramic substrate
(70 mm × 70 mm × t1.0 mm).
*3 t = 10 μs, Duty Cycle ≤ 1 %

Equivalent circuit



■ Electrical Characteristics Ta = 25 °C ± 3 °C

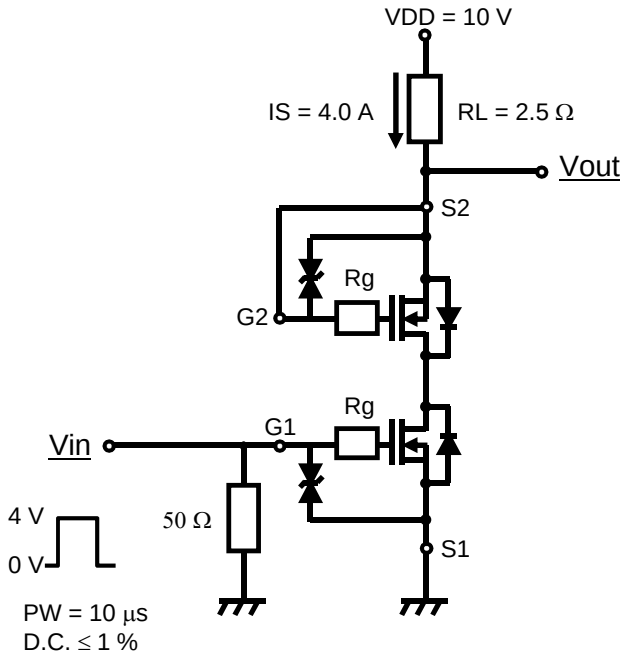
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
		VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 0.84 mA, VSS = 10 V	0.35	0.90	1.4	V
Source-source On-state Resistance	RSS(on)1	IS = 4.0 A, VGS = 4.5 V	3	4	5.1	mΩ
	RSS(on)2	IS = 4.0 A, VGS = 3.8 V	3.2	4.3	5.5	
	RSS(on)3	IS = 4.0 A, VGS = 3.1 V	3.5	4.8	6.8	
	RSS(on)4	IS = 4.0 A, VGS = 2.5 V	3.8	5.9	10	
Body Diode Forward Voltage	VF(s-s)	IF = 4.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 MHz		2760		pF
Output Capacitance *1	Coss			450		
Reverse Transfer Capacitance *1	Crss			390		
Turn-on delay Time *1,*2	td(on)	VDD = 10 V, VGS = 0 to 4.0 V		4.1		μs
Rise Time *1,*2	tr	IS = 4.0 A		5.2		
Turn-off delay Time *1,*2	td(off)	VDD = 10 V, VGS = 4.0 to 0 V		12.9		μs
Fall Time *1,*2	tf	IS = 4.0 A		8.3		
Total Gate Charge *1	Qg	VDD = 10 V		26		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4.0 V,		9		
Gate-drain Charge *1	Qgd	IS = 4.0 A		8		

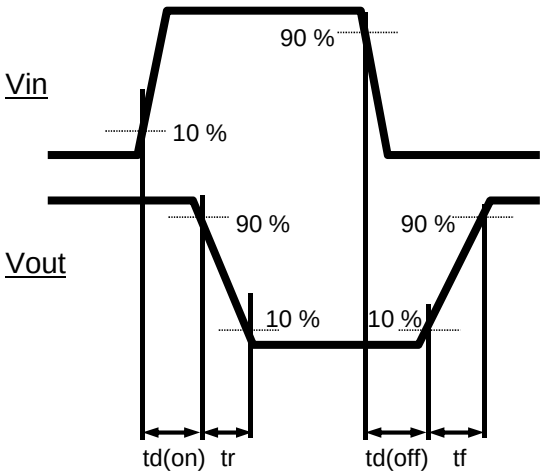
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

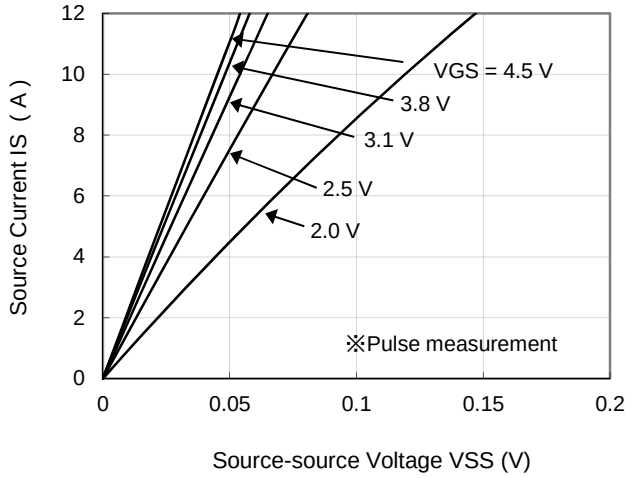
Note2:Measurement circuit



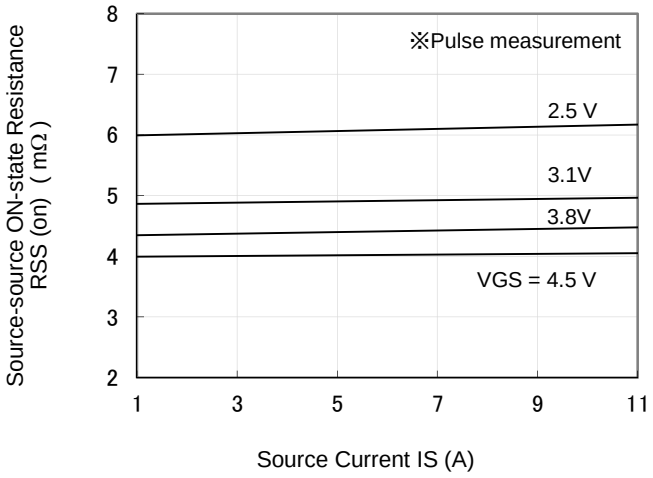


Technical Data (reference)

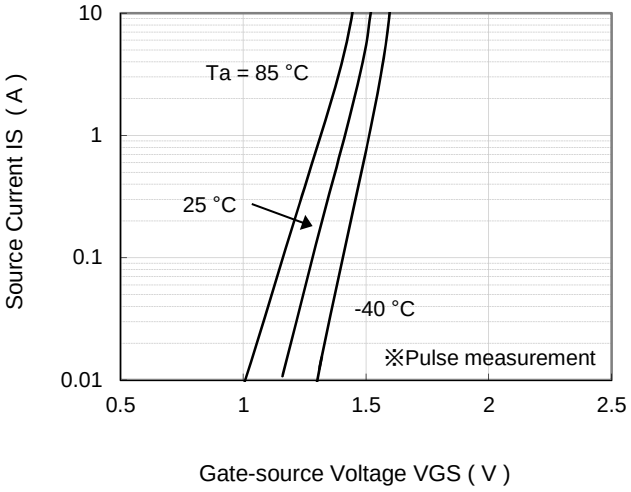
IS - VSS



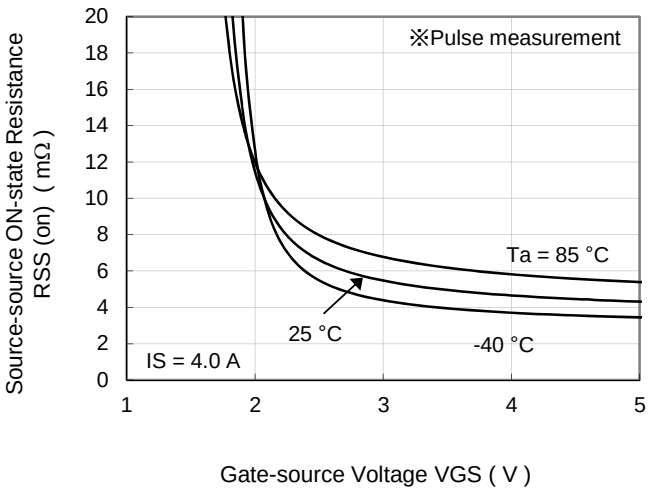
RSS(on) - IS



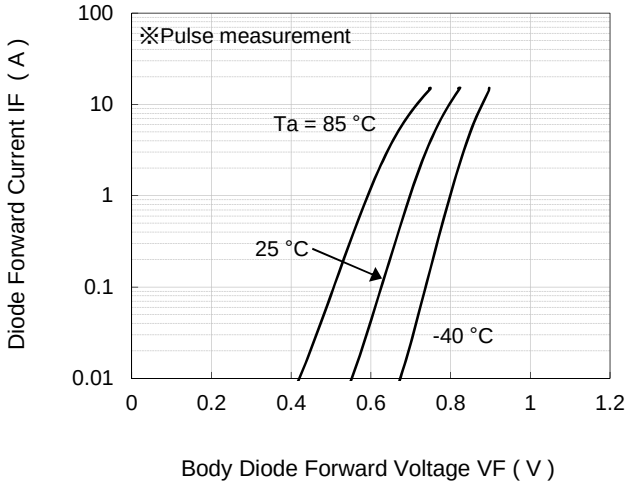
IS - VGS



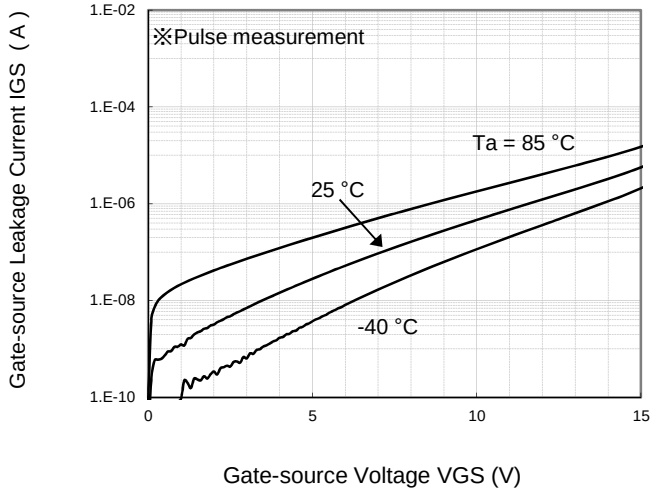
RSS(on) - VGS



IF - VF

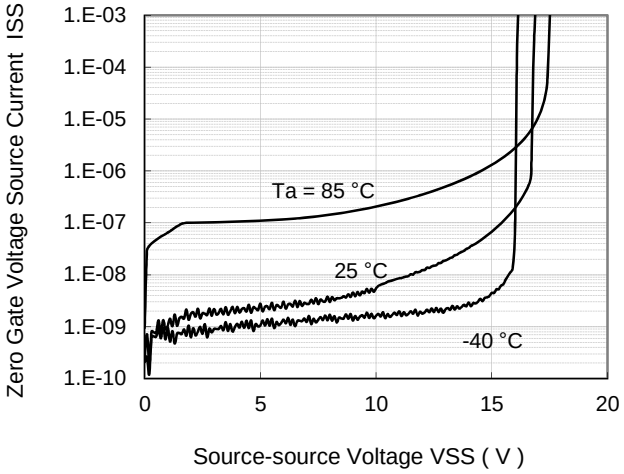


IGS - VGS

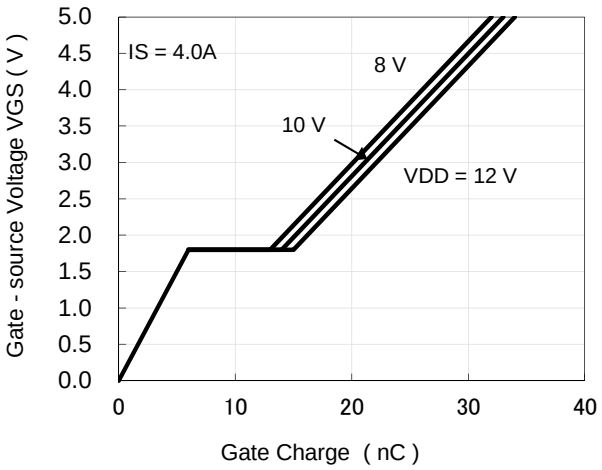


Technical Data (reference)

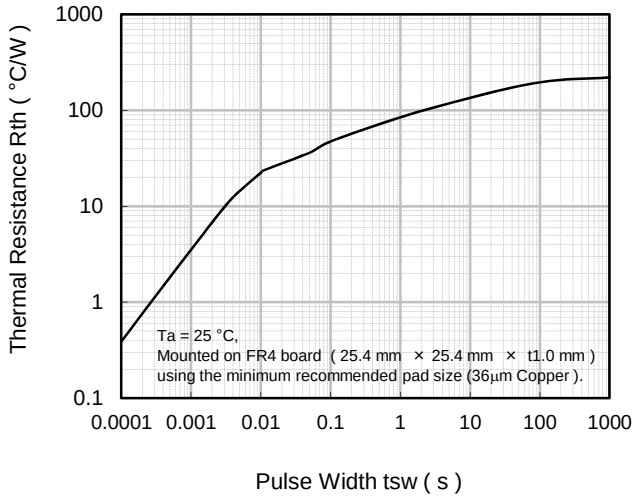
ISS - VSS



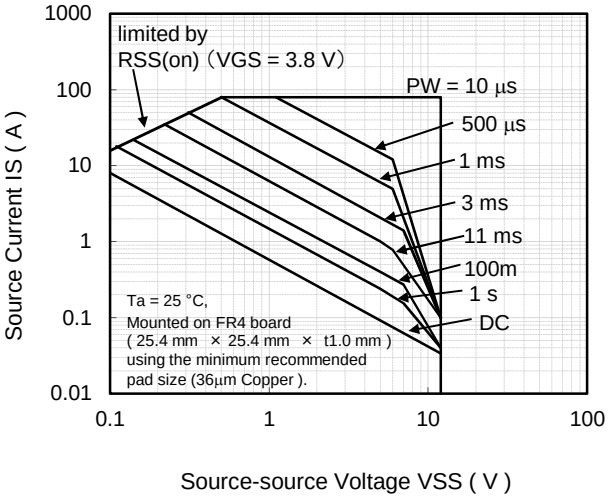
Dynamic Input/Output Characteristics



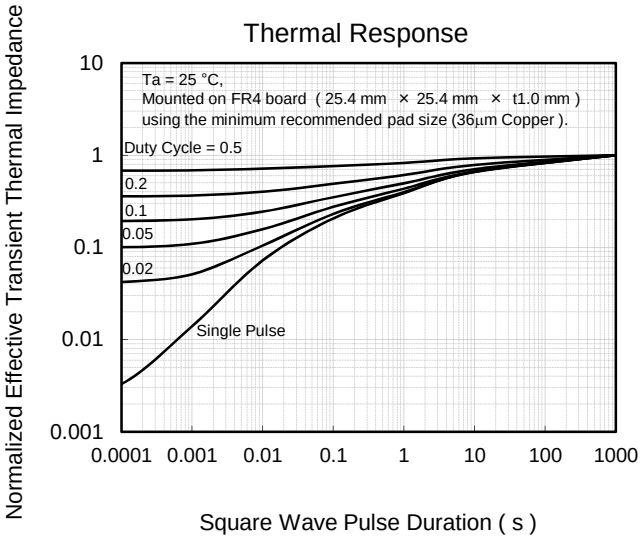
Rth - tsw



Safe Operating Area

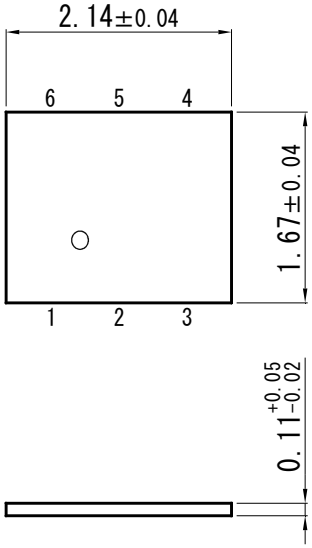


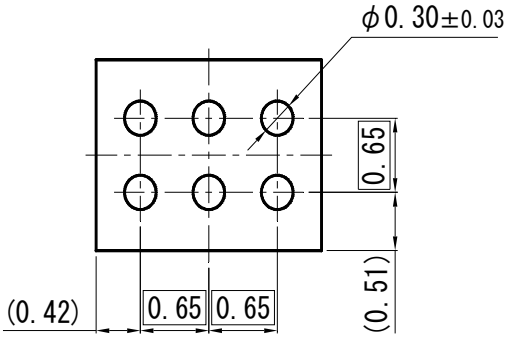
Thermal Response



MLGA006-W-1721-RA

Unit: mm





■ Land Pattern (Reference) (Unit: mm)