

SGM862 Dual-Channel, Low-Power, High-Accuracy Voltage Detector

GENERAL DESCRIPTION

The SGM862 family is a high-accuracy, low-power, and small size dual-channel voltage detector which can monitor two power rails respectively.

SENSEx is the input pin which can be programmed with an external resistor divider. There are four different hysteresis options of 0.6%, 1%, 5% or 10%.

OUTx is the open-drain corresponding output of SENSEx. OUTx goes low when the input voltage of SENSEx is lower than the falling threshold (V_{IT}) . OUTx goes high when the input voltage of SENSEx is higher than the rising threshold (V_{IT+}) . The internal hysteresis of SENSEx has glitch immunity and ensures stable operation.

The device has low quiescent current of 1.1µA (TYP), high accuracy and small size, which is particularly suitable for system-monitoring of low power and portable equipment.

The SGM862 is available in Green UTDFN-1.45×1-6AL and SOT-23-6 packages.

FEATURES

- **Supply Voltage Range: 1.65V to 6.5V**
- **High-Accuracy Threshold and Hysterisis:**
- **1.5% at** V_{DD} **= 1.65V to 3.3V**
- **1.7% at** V_{DD} **= 1.65V to 6.5V**
- **Low Quiescent Current: 1.1µA (TYP)**
- **Four Hysteresis Options: 0.6%, 1%, 5% and 10%**
- **Open-Drain Output**
- **Available in Green UTDFN-1.45×1-6AL and SOT-23-6 Packages**

APPLICATIONS

DSP or Microcontroller Notebooks and Tablet Computers Portable and Handheld Devices Battery-Powered Products Set-top Boxes Solid-State Drives (SSD) Building Automation Power Sequencing mput voltage of SENSEx is higher than the

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Portable and Handheld Devices

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Set-top Boxes

Solid-State Drives (SSD)

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Power Sequenci

Figure 1. Typical Application Circuit

TYPICAL APPLICATION

PACKAGE/ORDERING INFORMATION

MARKING INFORMATION

NOTE: X = Date Code. XX = Date Code. **UTDFN-1.45×1-6L SOT-23-6**

Date Code - Quarter Serial Number **YY X**

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

RECOMMENDED OPERATING CONDITIONS

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

PIN DESCRIPTION

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.65V to 6.5V, T_J = -40°C to +125°C, typical values are at V_{DD} = 3.3V and T_J = +25°C, unless otherwise noted.)

NOTE:

NOTE:
1. Outputs are undetermined below V
. POR.

TIMING REQUIRMENTS

(SENSEx transitions between 0V and 1.3V, R_{PU1} = R_{PU2} = 10kΩ, typical values are at V_{DD} = 3.3V and T_J = +25°C, unless otherwise noted.)

NOTE:

1. During power-on or a period that VDD transient is lower than V_{DD_MIN} , the outputs reflect the input conditions 730µs after VDD transitions through V_{DD $MIN.$

Figure 2. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

 T_J = +25°C with a 0.1µF capacitor beside VDD, unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 T_J = +25°C with a 0.1µF capacitor beside VDD, unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 T_J = +25°C with a 0.1µF capacitor beside VDD, unless otherwise noted.

FUNCTIONAL BLOCK DIAGRAM

Figure 3. SGM862 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM862 family is a high-accuracy, low-power, and small size dual-channel voltage detector with open-drain output.

SENSEx is the input pin which can be programmed with an external resistor divider. There are four different hysteresis options of 0.6%, 1%, 5% or 10%. As shown in [Table 1,](#page-9-0) OUTx goes low when the input voltage of SENSEx is lower than the falling threshold (V_{IT}) . OUTx goes high when the input voltage of SENSEx is higher than the rising threshold (V_{IT+}) . The internal hysteresis of SENSEx has glitch immunity and ensures stable operation.

The device can be used to monitor multiple voltage rails in applications or simultaneously monitor both early warning signal channel and reset signal channel in one system.

Table 1. SGM862 Truth Table

Inputs (SENSE1, SENSE2)

The SGM862 has two voltage detection comparators. The comparator input voltage is from 0V to 6.5V, which is independent of the device power supply voltage used. The no-inverting input of the comparator is connected to the external resistor divider. The inverting input of the comparator is connected to an internal threshold reference. When SENSEx voltage drops below V_{IT} , the corresponding OUTx is driven low. When SENSEx voltage rises above V_{IT+} , the corresponding OUTx is driven high. The hysteresis falling threshold prevents the comparator from being falsely triggered, and ensures stable operation.

In situations with extremely high noise and interference, it is recommended to place a 1nF to 10nF bypass capacitor at the input of the comparator to improve transient immunity and reduce the sensitivity of layout parasitism. In most cases, the decoupling capacitance is not required. See [Figure 2](#page-4-0) for more details.

Outputs (OUT1, OUT2)

The SGM862 is usually used in reset or power sequencing circuit, where the output is connected to the digital signal processor (DSP), microcontroller (μC) , microprocessor (CPU) and so on, or the output is connected to the DC/DC or LDO enable terminal to enable or disable the power converter.

OUT1 and OUT2 are two open-drain outputs of SGM862. A pull-up resistor is needed to connect a voltage rail, which can be up to 6.5V and is independent of the device power supply voltage (V_{DD}) . To choose a proper pull-up resistor, users should consider low-level output voltage (V_{ol}) , sink current capability and output leakage current $(I_{LKG\ OD})$. The open-drain output is convenient for the logic level compatibility. Another advantage of open-drain output is to implement wired and logic easily. OUT1 and OUT2 can be combined into one logic signal. The input (SENSE1, SENSE2) section has described how to assert or desserts the output. gnal channel and reset signal channel in one

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Device Functional Modes

Normal Operation ($V_{DD} \geq V_{DD-MIN}$ **)** Once the voltage on VDD rises above V_{DD-MIN} and lasts for t_{SD} , the OUTx starts to indicate the present state of corresponding SENSEx pins.

Power-On Reset (VDD < V_{POR})

Once the voltage on VDD is below V_{POR} which is the required voltage to pull the output to GND, the OUTx is undefined and unreliable for proper system operation.

APPLICATION INFORMATION

The SGM862 family is a dual-voltage detector with high accuracy. The monitored voltage, VDD voltage and output pull-up voltage can be flexibly used as independent voltages or connected to any other configuration.

Threshold Overdrive

Threshold overdrive is how much SENSEx exceeds the threshold V_{IT} , which is important to know because the larger the overdrive is, the faster the OUTX responses. V_{IT} is the threshold voltage in Equation 1. Use the percent of the sense voltage threshold to calculate the threshold overdrive.

$$
\\
$$
 Overdrive = | ($V_{\text{SENSE}}/V_{1T} - 1$) × 100% | (1)

 V_{IT} is V_{IT} when caculating the negative-going threshold overdrive. V_{IT} is V_{IT+} when caculating the positive-going threshold overdrive.

Sense Resistor Divider

Use Equation 2 to caculate the resistor divider values, which determines V_{MON} Use Equation 3 to caculate the target threshold voltage, which determines $V_{MON}P_{G}$.

$$
V_{MON_UV} = \left(1 + \frac{R_1}{R_2}\right) \times V_{IT-}
$$
 (2)

$$
V_{MON_PG} = \left(1 + \frac{R_1}{R_2}\right) \times V_{IT+}
$$
 (3)

SENSEx pins:

 R_1 is the upper divider resistor. R_2 is the lower divider resistor.

 V_{MON} is the target voltage for monitoring the under-voltage.

 $V_{MON\ PG}$ is the target voltage that monitors the output goes high during V_{MONx} rises.

Selecting the total resistance values of R_1 and R_2 determines that the current flowing through the divider about 100 times higher than the SENSEx input current. Meanwhile, choose the resistors values as high as possible to minimize current consumption which will not bring about obvious error to the resistance divider.

Power-Supply Recommendations

The input supply voltage of SGM862 ranges from 1.65V to 6.5V. A 0.1μF or greater ceramic capacitor close to VDD pin is recommended. VDD pin has a 7V absolute maximum rating. V_{IT} is V_{IT} , when caculating the positive-going
overdrive.
Power-Supply Recommendations
Existence diversition 2 to caculate the resistor divider values,
 V_{MON_UV} . Use Equation 3 to caculate
threshold voltage, wh **Power-Supply Recommendations**
The input supply voltage of SGM862 ranges.
Equation 3 to caculate
th determines V_{MON_PG}.
(2)
 $\frac{1}{2}$ x V_{IT}_ (2)
(2)

APPLICATION INFORMATION (Continued)

Monitoring Two Separate Rails

Figure 4. Monitoring Two Separate Rails Circuit

Table 2. Design Parameters

Detailed Design Procedure

The SGM862D is 10% hysterisis version and chosen finally. An open-drain output allows for the output to be pulled up to a voltage other than V_{DD} .

Use Equation 2 and Equation 3 to calculate the resistor divider values. For SENSE1, $R_1 = 1.72M\Omega$ and $R_2 =$ 1.18MΩ. While R_3 and R_4 of SENSE2 can be caculate through R_1 and R_2 in Equation 2 and Equation 3. Therefore, $R_3 = 1.42 M\Omega$ and $R_4 = 1.18 M\Omega$.

Application Curve

Time (500µs/div)

APPLICATION INFORMATION (Continued)

Early Warning Detection

Figure 5. Early Warning Detection Schematic

Table 3. Design Parameters

Detailed Design Procedure

The SGM862D is 10% hysterisis version and chosen finally.

Use Equation 4 to calculate the total resistor divider values. The minimum total resistance of the resistor network is calculated based on the current consumption specification. Choose the current approximately 1μA that flows through the resistor network. In this case, from low to high conversion, V_{MON} $_{PG2}$ is considered more important.

$$
R_{\text{total}} = \frac{V_{\text{MON_PG_2}}}{I} = \frac{3.9V}{1 \mu A} = 3.9 M \Omega
$$
 (4)

Use Equation 5 to calculate R_3 . V_{MON PG2} corresponds to V_{IT+} value in channel 2. Select the nearest 1% accuracy resistor value instead of the calculated. In this case, 1.18M Ω is the closest value for R₃.

$$
R_3 = \frac{V_{1T+}}{I} = \frac{1.182V}{1\mu A} = 1.182M\Omega
$$
 (5)

Use Equation 6 to calculate R_2 . Select the nearest 1% accuracy resistor value instead of the calculated. In this case, 200kΩ is the closest value for R_2 . In this case, from high-to-low conversion, $V_{MONUV-1}$ is considered more important.

 $=\frac{3.9MΩ}{eV}$ × 1.061V - 1.18MΩ = 199kΩ $=$ $\frac{10TAL}{10} \times$ TOTAL $2 \sqrt{11}$ T-3 MON_UV _1 R $R_2 = \frac{1.70 \text{ T} \cdot \text{N}}{1.70 \text{ T} \cdot \text{N}} \times V_{\text{NT}}$ - R V 3V (6) WHON_PG = 3.3V, V_{MON_PG} = 3.3V, V_{MON_PG} = 3.3V, V_{MON_PG} = 3.9V, V_{MON_PG} = 3.5V

Let **Design Procedure**

Use Equation 7 to calculate R_1 . Select the nearest 1% accuracy resistor value instead of the calculated. In this case, 2.55MΩ is the closest value for R_1 .

$$
R_1 = R_{\text{TOTAL}} - R_2 - R_3
$$

= 3.9 M Ω - 200k Ω - 1.18 M Ω = 2.52 M Ω (7)

Application Curve

LAYOUT

It is recommended to place the decoupling capacitor close to VDD, and place the bypass capacitor close to the SENSEx if the bypass capacitor is necessary.

Avoid long traces to power VDD. The VDD decoupling capacitor and parasitic inductance from long traces can form LC resonance and cause ringing with peak voltages, which may damage the device.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (JUNE 2023) to REV.A Page

Changed from product preview to production data...All

PACKAGE OUTLINE DIMENSIONS

UTDFN-1.45×1-6AL

NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

SOT-23-6

NOTES:

1. This drawing is subject to change without notice.

2. The dimensions do not include mold flashes, protrusions or gate burrs.

3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

CARTON BOX DIMENSIONS

NOTE: The picture is only for reference. Please make the object as the standard.

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