ADC128D818 12-Bit, 8-Channel, ADC System Monitor With Temperature Sensor, Internal – External Reference, and I²C Interface

1 Features

- 12-Bit Resolution Delta-Sigma ADC
- Local Temperature Sensing
- Configurable Single-Ended and/or Pseudo-Diff. Inputs
- 2.56-V Internal VREF or Variable External VREF
- WATCHDOG Window Comparators with Status and Mask Registers of All Measured Values
- Independent Registers for Storing Measured Values
- $\overline{\text{INT}}$ Output Notifies Microprocessor of Error Event
- I²C Serial Bus Interface Compatibility
- 9 Selectable Addresses
- TIME-OUT Reset Function to Prevent I²C Bus Lock-Up
- Individual Channel Shutdown to Limit Power Consumption
- Deep Shutdown Mode to Minimize Power Consumption
- TSSOP 16-Lead Package
- Key Specifications
  - ADC Resolution 12-Bit
  - Supply Voltage Range 3 V to 5.5 V
  - Total Unadjusted Error –0.45%/+0.2%
  - Integral Non-Linearity ±1 LSb
  - Differential Non-Linearity ±1 LSb
  - Operating Current 0.56 mA
  - Deep Shutdown Current 10 µA
  - Temperature Resolution °C/LSb
  - Temperature Accuracy (–40°C to 125°C) ±3°C
  - Temperature Accuracy (–25°C to 100°C) ±2°C

2 Applications

- Communications Infrastructure
- Thermal and Hardware Server Monitors
- System Monitors
- Industrial and Medical Systems
- Electronic Test Equipment and Instrumentation
- Power Supply Monitoring and Supervision

3 Description

The ADC128D818 I²C system monitor is designed for maximum flexibility. The system monitor can be configured for single-ended and/or pseudo-differential inputs. An onboard temperature sensor, combined with WATCHDOG window comparators, and an interrupt output pin, $\overline{\text{INT}}$, allow easy monitoring and out-of-range alarms for every channel. A high performance internal reference is also available to provide for a complete solution in the most difficult operating conditions.

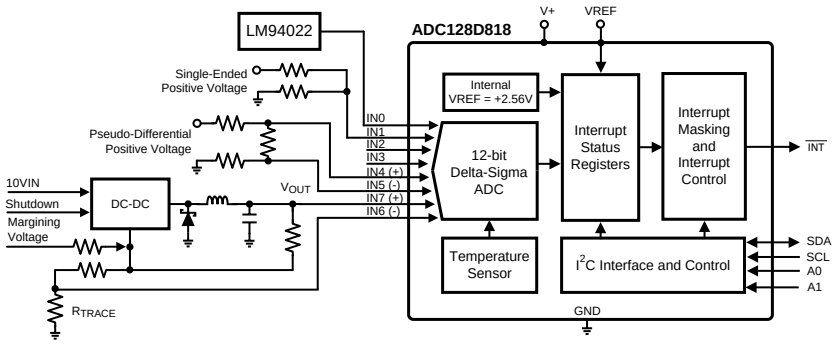
The ADC128D818's 12-bit delta-sigma ADC supports Standard Mode (Sm, 100 kbps) and Fast Mode (Fm, 400 kbps) I²C interfaces. The ADC128D818 includes a sequencer to control channel conversions and stores all converted results in independent registers for easy microprocessor retrieval. Unused channels can be shut down independently to conserve power.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC128D818	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed *Product Highlights* ... 1

Changes from Revision D (January 2011) to Revision E **Page**

- Changed layout of National Data Sheet to TI format ... 27

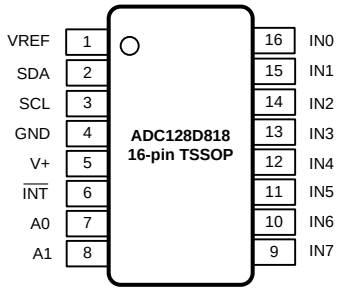
5 Description (continued)

The ADC can use either an internal 2.56-V reference or a variable external reference. An analog filter is included on the I^2C digital control lines to provide improved noise immunity. The device also includes a TIME-OUT reset function on SDA and SCL to prevent I^2C bus lock-up.

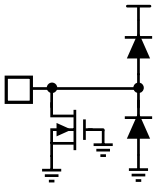
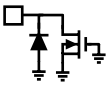
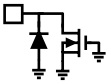
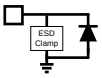
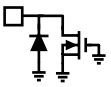
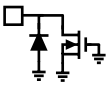
The ADC128D818 operates from 3-V to 5.5-V power supply voltage range, –40°C to 125°C temperature range, and the device is available in a 16-pin TSSOP package.

6 Pin Configuration and Functions

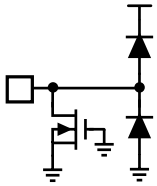
PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NO.	NAME	ESD STRUCTURE		
1	VREF		Analog Input	ADC external reference. ADC128D818 allows two choices for sourcing VREF: internal or external. If the 2.56-V internal VREF is used, leave this pin unconnected. If the external VREF is used, source this pin with a voltage between 1.25 V and V+. At Power-On-Reset (POR), the default setting is the internal VREF. Bypass with the parallel combination of 1-µF (electrolytic or tantalum) and 0.1-µF (ceramic) capacitors.
2	SDA		Digital I/O	Serial Bus Bidirectional Data. NMOS open-drain output. Requires external pullup resistor to function properly.
3	SCL		Digital Input	Serial Bus Clock. Requires external pullup resistor to function properly.
4	GND		GROUND	Internally connected to all of the circuitry.
5	V^+		POWER	3.0-V to 5.5-V power. Bypass with the parallel combination of 1-µF (electrolytic or tantalum) and 0.1-µF (ceramic) bypass capacitors.
6	$\overline{INT}$		Digital Output	Interrupt Request. Active Low, NMOS, open-drain. Requires external pullup resistor to function properly.
7	A0		Tri-Level Inputs	Tri-Level Serial Address pins that allow 9 devices on a single I^2C bus.
8	A1			

Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NO.	NAME	ESD STRUCTURE		
9	IN7		Analog Inputs	The full scale range will be controlled by the internal or external VREF. These inputs can be assigned as single-ended and/or pseudo-differential inputs.
10	IN6			
11	IN5			
12	IN4			
13	IN3			
14	IN2			
15	IN1			
16	IN0			

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)Æ(4)

	MIN	MAX	UNIT
Supply Voltage (V+)	6.0	6	V
Voltage on SCL, SDA, A0, A1, $\overline{INT}$	–0.3	6	V
Voltage on IN0-IN7, VREF	–0.3	(V^+ + 0.3)	V
Input Current at Any Pin(5)		±5	mA
Package Input Current(5)		±30	mA
Maximum Junction Temperature (T_{JMAX})(6)		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) All voltages are measured with respect to GND, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(4) For soldering specifications, SNOA549
(5) If the input voltage at any pin exceeds the power supply (that is, VIN < GND or VIN > V^+) but is less than the absolute maximum ratings, then the current at that pin must be limited to 5 mA. The 30 mA maximum package input current rating limits the number of pins that can safely exceed the power supply with an input current of 5 mA to six pins. Parasitic components and/or ESD protection circuitry are shown in the Pin Descriptions table.
(6) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, $R_{\theta JA}$ and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A) / R_{\theta JA}$.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
	Machine model	±300	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted[1])

	MIN	MAX	UNIT
Supply Voltage (V+)	3	5.5	V
Voltage on SCL, SDA, A0, A1, $\overline{INT}$	–0.05	5.5	V
Voltage on IN0-IN7, VREF	–0.05	(V^+ + 0.05)	V
Temperature Range for Electrical Characteristics	–40	125	°C
Operating Temperature	–40	125	°C

(1) All voltages are measured with respect to GND, unless otherwise specified.

7.4 Thermal Information

THERMAL METRIC[1]		ADC128D818 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 DC Electrical Characteristics

The following specifications apply for 3 V_{DC} ≤ V^+ ≤ 5.5 V_{DC} , External VREF = 2.56 V, unless otherwise specified. All limits T_A = T_J = 25°C unless otherwise specified[1].

PARAMETER		TEST CONDITIONS		MIN[2]	TYP[3]	MAX[2]	UNIT
POWER SUPPLY CHARACTERISTICS							
V^+	Supply Voltage				3.3 or 5		V
		T_A = T_J = T_{MIN} to T_{MAX}		3		5.5	
VREF	External Reference Voltage				2.56		V
		T_A = T_J = T_{MIN} to T_{MAX}		1.25		V+	
	Internal Reference Voltage				2.56		V
					23		ppm/°C
I^+	Supply Current (see *Power Management*).	Interface Inactive, V+ = 5.5 V, Mode 2	T_A = T_J = T_{MIN} to T_{MAX}			0.74	mA
		Interface Inactive, V+ = 3.6 V, Mode 2	T_A = T_J = T_{MIN} to T_{MAX}			0.56	mA
		Shutdown Mode, V+ = 5.5 V	T_A = T_J = T_{MIN} to T_{MAX}			0.65	mA
		Shutdown Mode, V+ = 3.6 V	T_A = T_J = T_{MIN} to T_{MAX}			0.48	mA
		Deep Shutdown Mode[4].	T_A = T_J = T_{MIN} to T_{MAX}			10	µA
TEMPERATURE-to-DIGITAL CONVERTER CHARACTERISTICS							
	Temperature Error	–40°C ≤ T_A ≤ +125°C	T_A = T_J = T_{MIN} to T_{MAX}			±3	°C
		–25°C ≤ T_A ≤ +100°C	T_A = T_J = T_{MIN} to T_{MAX}			±2	°C
	Resolution				0.5		°C
ANALOG-to-DIGITAL CONVERTER CHARACTERISTICS							
n	Resolution	12-bit with full-scale at VREF = 2.56 V.			0.625		mV

(1) Each input and output is protected by an ESD structure to GND, as shown in the . Input voltage magnitude up to 0.3 V above V^+ or 0.3 V below GND will not damage the ADC128D818. There are diodes that exist between some inputs and the power supply rails. Errors in the ADC conversion can occur if these diodes are forward biased by more than 50 mV. As an example, if V^+ is 4.5 V_{DC}, INx (where 0 ≤ x ≤ 7) must be ≤ 4.55 V_{DC} to ensure accurate conversions.
(2) Limits are ensured to AOQL (Average Outgoing Quality Level).
(3) Typicals are at T_J = T_A = 25°C and represent most likely parametric normal.
(4) Limit is specified by characterization.

DC Electrical Characteristics (continued)

The following specifications apply for 3 V_{DC} ≤ V^+ ≤ 5.5 V_{DC} , External VREF = 2.56 V, unless otherwise specified. All limits T_A = T_J = 25°C unless otherwise specified(1).

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
INL	Integral Non-Linearity	External VREF = 1.25 V, Pseudo-Differential, V+ = 3 V to 3.3 V.(4)			0.36		LSb
			$T_A = T_J = T_{MIN}$ to T_{MAX}	–1		1	
		External VREF = 2.56 V, Pseudo-Differential			1.58		LSb
		External VREF = 5 V, Pseudo-Differential, V+ = 5 V to 5.5 V.	$T_A = T_J = T_{MIN}$ to T_{MAX}	–2		4	
DNL	Differential Non-Linearity	See (5)			±0.25		LSb
			$T_A = T_J = T_{MIN}$ to T_{MAX}	–1		1	
TUE	Total Unadjusted Error(6)	Internal VREF, Single-Ended, V+ = 3 V to 3.6 V.	$T_A = T_J = T_{MIN}$ to T_{MAX}	–0.5		0.5	% of FS
		Internal VREF, Single-Ended, V+ = 4.5 V to 5.5 V(7).					
		Internal VREF, Pseudo-Differential, V+ = 3 V to 3.6 V or V+ = 4.5 V to 5.5 V(7).	$T_A = T_J = T_{MIN}$ to T_{MAX}	–0.3		0.5	% of FS
		External VREF = 1.25 V, Single-Ended, V+ = 3 V to 3.6 V.	$T_A = T_J = T_{MIN}$ to T_{MAX}	–0.6		0.1	% of FS
		External VREF = 2.56 V, Single-Ended, V+ = 3 V to 5.5 V.	$T_A = T_J = T_{MIN}$ to T_{MAX}				
		External VREF = 1.25 V, Pseudo-Differential, V+ = 3 V to 3.6 V.	$T_A = T_J = T_{MIN}$ to T_{MAX}	–0.45		0.2	% of FS
		External VREF = 2.56 V, Pseudo-Differential, V+ = 3 V to 5.5 V.	$T_A = T_J = T_{MIN}$ to T_{MAX}				
GE	Gain Error	Internal VREF, V+ = 3 V to 3.6 V.	$T_A = T_J = T_{MIN}$ to T_{MAX}	–0.25		0.45	% of FS
		Internal VREF, V+ = 4.5 V to 5.5 V(7)					
		External VREF = 1.25 V or 2.56 V, V+ = 3 V to 3.6 V.	$T_A = T_J = T_{MIN}$ to T_{MAX}	–0.45		0.2	% of FS
		External VREF = 2.56 V or 5 V, V+ = 4.5 V to 5.5 V.					
OE	Offset Error	Internal VREF, Pseudo-Differential,V+ = 4.5 V to 5.5 V(7).	$T_A = T_J = T_{MIN}$ to T_{MAX}	–0.15		0.2	% of FS
		External VREF = 1.25 V or 2.56 V, Single-Ended, V+ = 3 V to 3.6 V.	$T_A = T_J = T_{MIN}$ to T_{MAX}	–0.5		0.1	% of FS
		External VREF = 2.56 V or 5 V, Single-Ended, V+ = 4.5 V to 5.5 V					
		External VREF = 1.25 V or 2.56 V, Pseudo-Differential, V+ = 3 V to 3.6 V.	$T_A = T_J = T_{MIN}$ to T_{MAX}	–0.2		0.15	% of FS
		External VREF = 2.56 V or 5 V, Pseudo-Differential, V+ = 4.5 V to 5.5 V					

(5) Limit is specified by design.
(6) TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.
(7) The range is up to 7/8 of full scale.

DC Electrical Characteristics (continued)

The following specifications apply for 3 V_{DC} ≤ V^+ ≤ 5.5 V_{DC} , External VREF = 2.56 V, unless otherwise specified. All limits T_A = T_J = 25°C unless otherwise specified(1).

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
t_C	Continuous Conversion Mode	Each Enabled Voltage Channel			12		ms
		Internal Temperature Sensor			3.6		ms
	Low Power Conversion Mode	Enabled Voltage Channel(s) and Internal Temperature Sensor			728		ms
MULTIPLEXER / ADC INPUT CHARACTERISTICS							
R_{ON}	ON-Resistance				2		kΩ
			T_A = T_J = T_{MIN} to T_{MAX}			10	
I_{ON}	Input Current (On Channel Leakage Current)				±0.005		µA
I_{OFF}	Off Channel Leakage Current				±0.005		µA
DIGITAL OUTPUTS: $\overline{INT}$							
$V_{OUT(0)}$	Logical 0 Output Voltage	I_{OUT} = 5.0 mA at V^+ = 4.5 V, I_{OUT} = +3 mA at V^+ = +3 V	T_A = T_J = T_{MIN} to T_{MAX}			0.4	V
OPEN DRAIN SERIAL BUS OUTPUT: SDA							
$V_{OUT(0)}$	Logical 0 Output Voltage	I_{OUT} = 3.0 mA at V^+ = 4.5 V,	T_A = T_J = T_{MIN} to T_{MAX}			0.4	V
I_{OH}	High Level Output Current	V_{OUT} = V^+			0.005		µA
			T_A = T_J = T_{MIN} to T_{MAX}			1	
DIGITAL INPUTS: A0 and A1							
$V_{IN(1)}$	Logical 1 Input Voltage	T_A = T_J = T_{MIN} to T_{MAX}		0.9 × V+		5.5	V
V_{IM}	Logical Middle Input Voltage	T_A = T_J = T_{MIN} to T_{MAX}		0.43 × V+		0.57 × V+	
$V_{IN(0)}$	Logical 0 Input Voltage	T_A = T_J = T_{MIN} to T_{MAX}		GND – 0.05		0.1 × V+	V
SERIAL BUS INPUTS: SCL and SDA							
$V_{IN(1)}$	Logical 1 Input Voltage	T_A = T_J = T_{MIN} to T_{MAX}		0.7 × V^+		5.5	v
$V_{IN(0)}$	Logical 0 Input Voltage	T_A = T_J = T_{MIN} to T_{MAX}		GND – 0.05		0.3 × V^+	V
V_{HYST}	Hysteresis Voltage	V^+ = 3.3 V			0.67		V
		V^+ = 5.5 V			1.45		V
ALL DIGITAL INPUTS: SCL, SDA, A0, A1							
$I_{IN(1)}$	Logical 1 Input Current	V_{IN} = V^+			– 0.005		µA
			T_A = T_J = T_{MIN} to T_{MAX}	−1			
$I_{IN(0)}$	Logical 0 Input Current	V_{IN} = 0 V_{DC}			0.005		µA
			T_A = T_J = T_{MIN} to T_{MAX}			1	
C_{IN}	Digital Input Capacitance				20		pF

7.6 AC Electrical Characteristics

The following specifications apply for +3.0 V_{DC} ≤ V^+ ≤ +5.5 V_{DC} , unless otherwise specified. All limits T_A = T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
SERIAL BUS TIMING CHARACTERISTICS						
t_1	SCL (Clock) Period	T_A = T_J = T_{MIN} to T_{MAX}	2.5		100	µs
t_2	Data In Set-up Time to SCL High	T_A = T_J = T_{MIN} to T_{MAX}	100			ns
t_3	Data Out Stable After SCL Low	T_A = T_J = T_{MIN} to T_{MAX}	0			ns
t_4	SDA Low Set-up Time to SCL Low (start)	T_A = T_J = T_{MIN} to T_{MAX}	100			ns
t_5	SDA High Hold Time After SCL High (stop)	T_A = T_J = T_{MIN} to T_{MAX}	100			ns
$t_{TIME-OUT}$	SCL or SDA time low for I^2C bus reset	T_A = T_J = T_{MIN} to T_{MAX}	25		35	ms

(1) Limits are ensured to AOQL (Average Outgoing Quality Level).
(2) Typicals are at T_J = T_A = 25°C and represent most likely parametric normal.

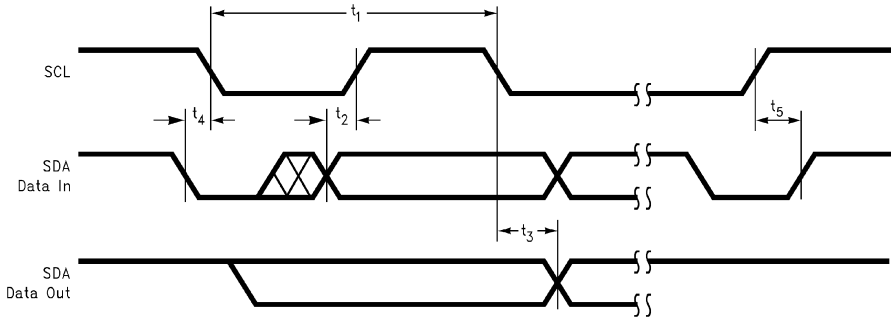


Figure 1. Serial Bus Timing Diagram

7.7 Typical Characteristics

The following typical performance plots apply for the internal VREF = 2.56 V, V+ = 3.3 V, Pseudo-Differential connection, unless otherwise specified. All limits $T_A = T_J = 25°C$ unless otherwise specified.

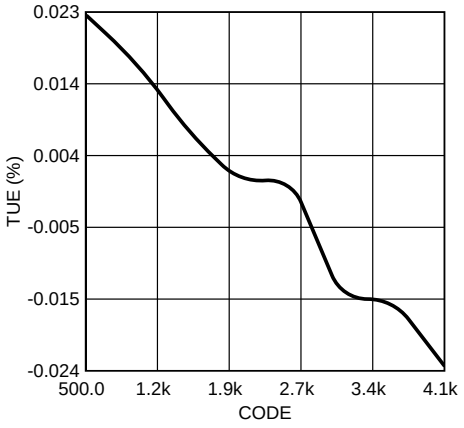


Figure 2. TUE vs. Code

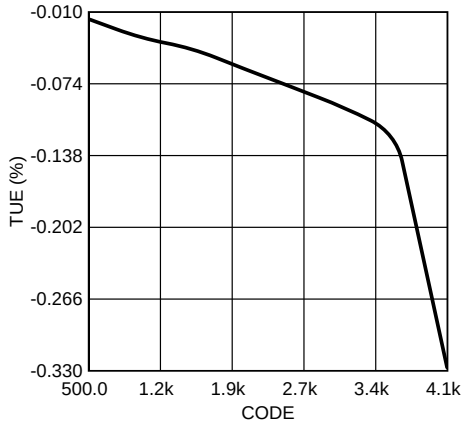


Figure 3. TUE vs. Code (External VREF = 1.25 V)

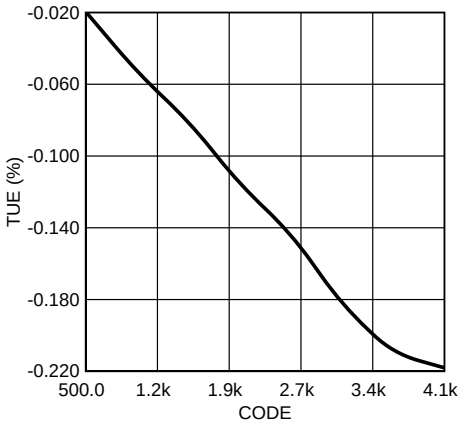


Figure 4. TUE vs. Code (External VREF = 2.56 V)

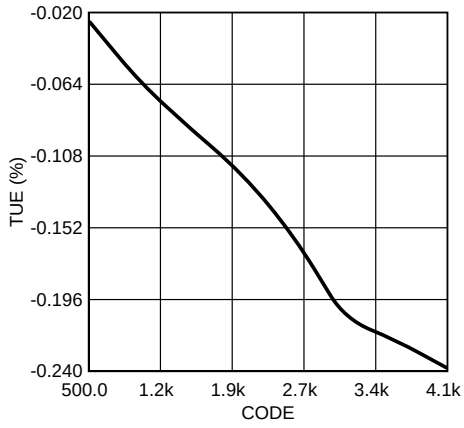


Figure 5. TUE vs. Code (External VREF = 5 V, V+ = 5 V)

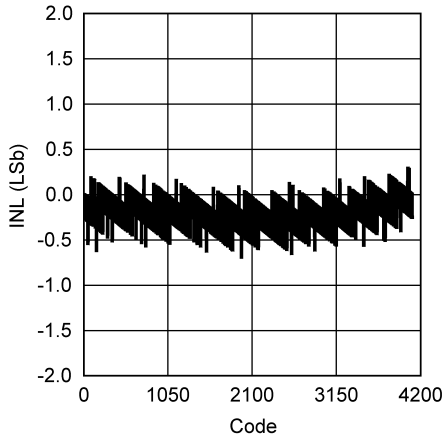


Figure 6. INL vs. Code (External VREF = 1.25 V for 1 Unit)

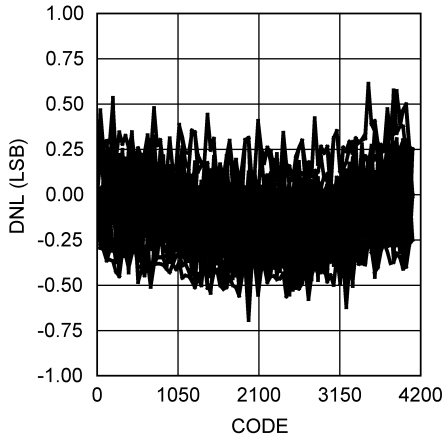


Figure 7. INL vs. Code (External VREF = 1.25 V for 28 Units)

Typical Characteristics (continued)

The following typical performance plots apply for the internal VREF = 2.56 V, V+ = 3.3 V, Pseudo-Differential connection, unless otherwise specified. All limits $T_A = T_J = 25°C$ unless otherwise specified.

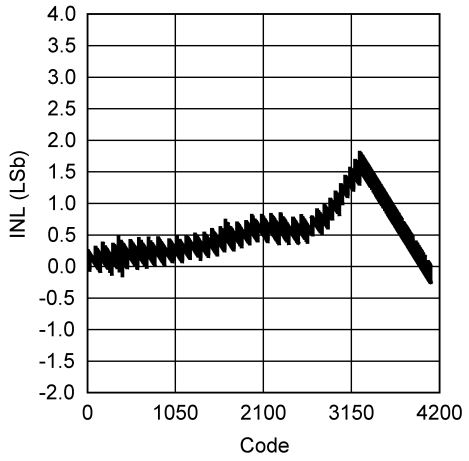


Figure 8. INL vs. Code (External VREF = 2.56 V for 1 Unit)

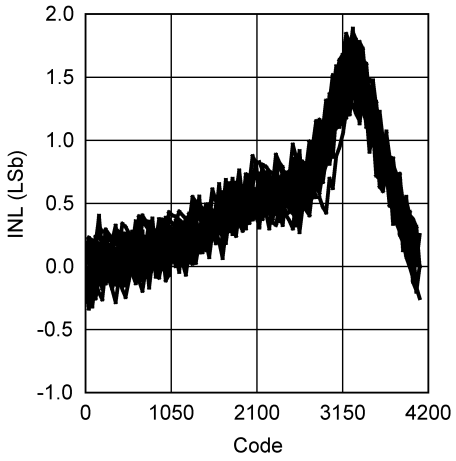


Figure 9. INL vs. Code (External VREF = 2.56 V for 28 Units)

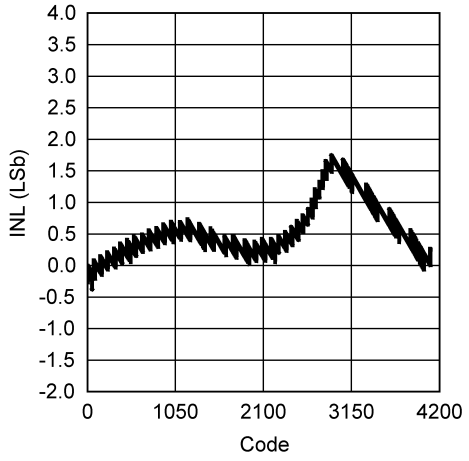


Figure 10. INL vs. Code (External VREF = 5 V, V+ = 5 V for 1 Unit)

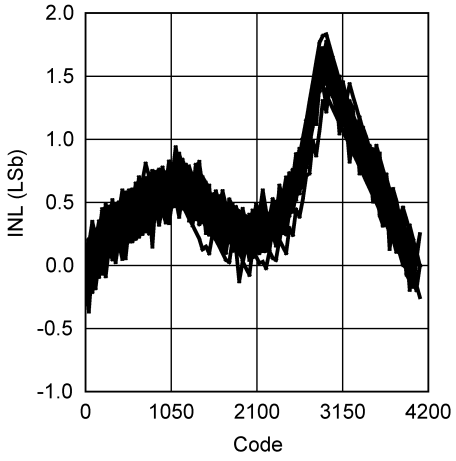


Figure 11. INL vs. Code (External VREF = 5 V, V+ = 5 V for 28 Units)

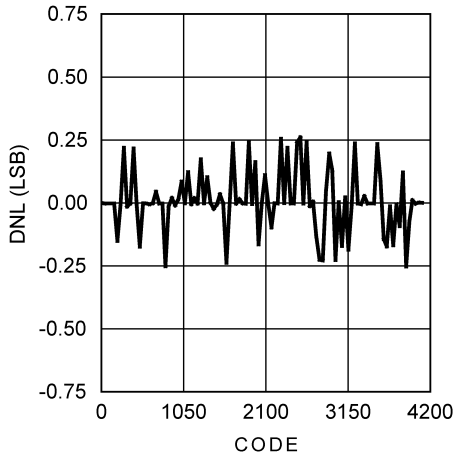


Figure 12. DNL vs. Code (External VREF = 2.56 V for 1 Unit)

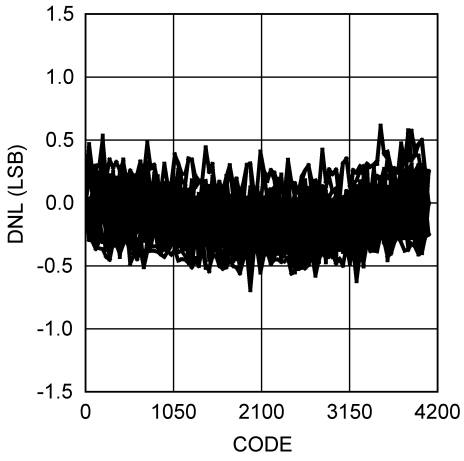


Figure 13. DNL vs. Code (External VREF = 2.56 V for 28 Units)

Typical Characteristics (continued)

The following typical performance plots apply for the internal VREF = 2.56 V, V+ = 3.3 V, Pseudo-Differential connection, unless otherwise specified. All limits $T_A = T_J = 25°C$ unless otherwise specified.

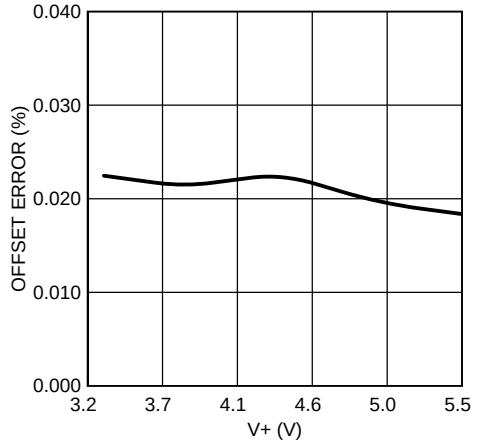


Figure 14. Offset Error vs. V+

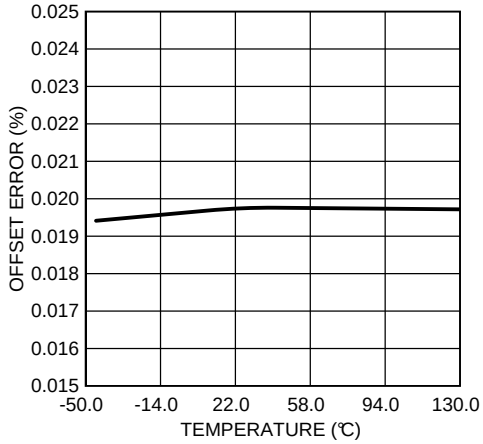


Figure 15. Offset Error vs. Temperature

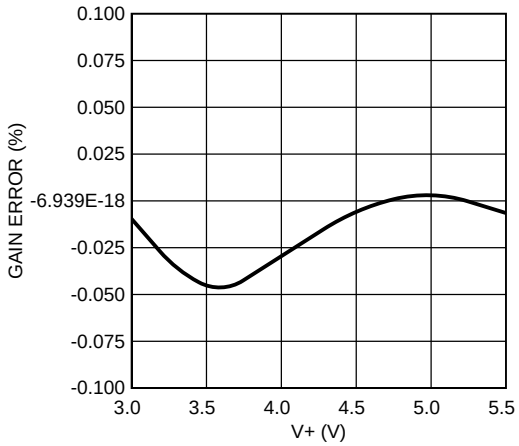


Figure 16. Gain Error vs. V+

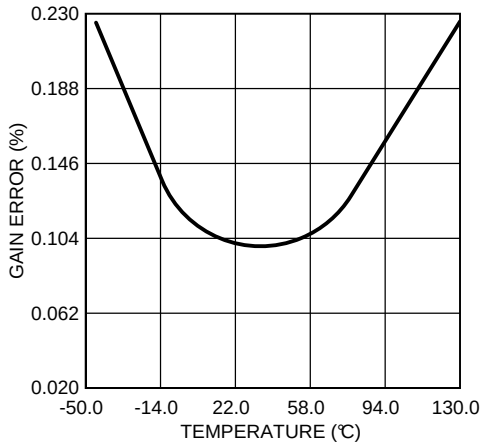


Figure 17. Gain Error vs. Temperature

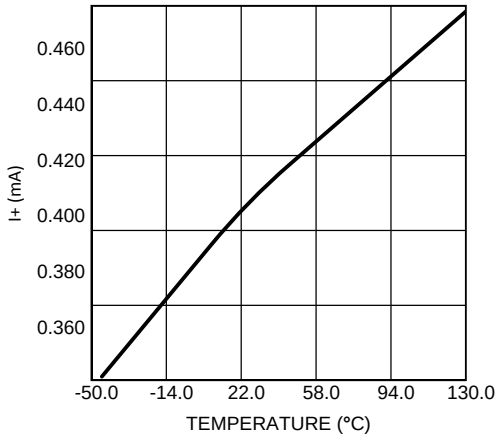


Figure 18. I+ vs. Temperature

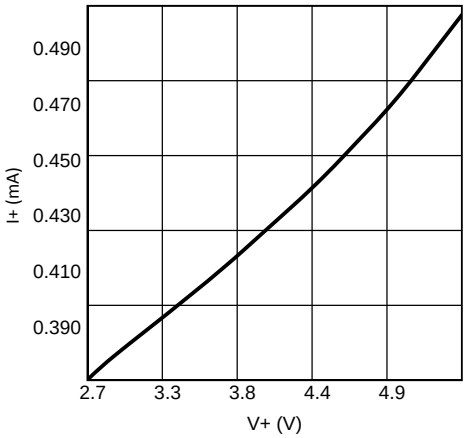


Figure 19. I+ vs. V+ Typical

A. Timing specifications are tested at the Serial Bus Input logic levels: V IN(0) = 0.3 × V + for a falling edge and V IN(1) = 0.7 × V + for a rising edge if the SCL and SDA edge rates are similar

Typical Characteristics (continued)

The following typical performance plots apply for the internal VREF = 2.56 V, V+ = 3.3 V, Pseudo-Differential connection, unless otherwise specified. All limits $T_A = T_J = 25°C$ unless otherwise specified.

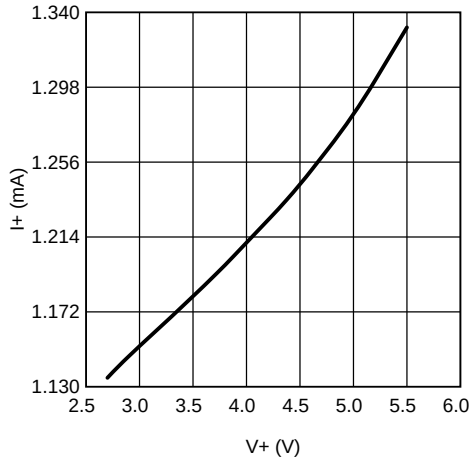


Figure 20. I+ vs. V+ for Voltage Conversion

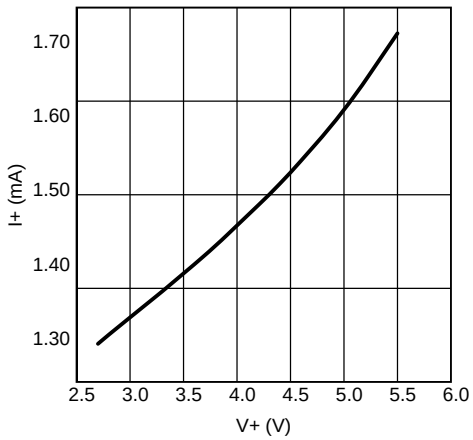


Figure 21. I+ vs. V+ for Temperature Conversion

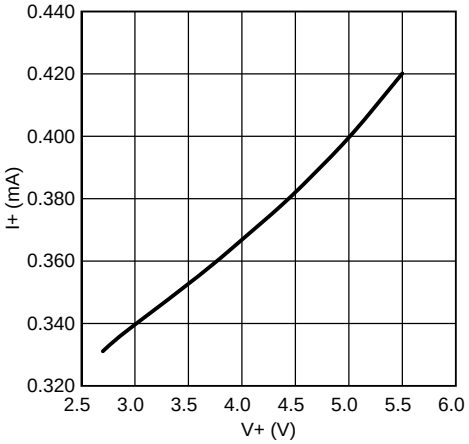


Figure 22. I+ vs. V+ in Shutdown Mode

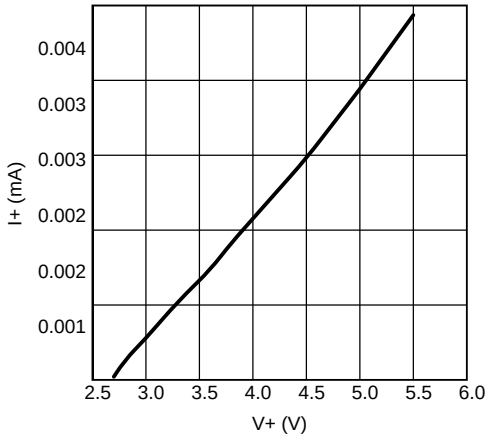


Figure 23. I+ vs. V+ in Deep Shutdown Mode

8 Detailed Description

8.1 Overview

The ADC128D818 provides 8 analog inputs, a temperature sensor, a delta-sigma ADC, an external or internal VREF option, and WATCHDOG registers on a single chip. An I^2C Serial Bus interface is also provided. The ADC128D818 can perform voltage and temperature monitoring for a variety of systems.

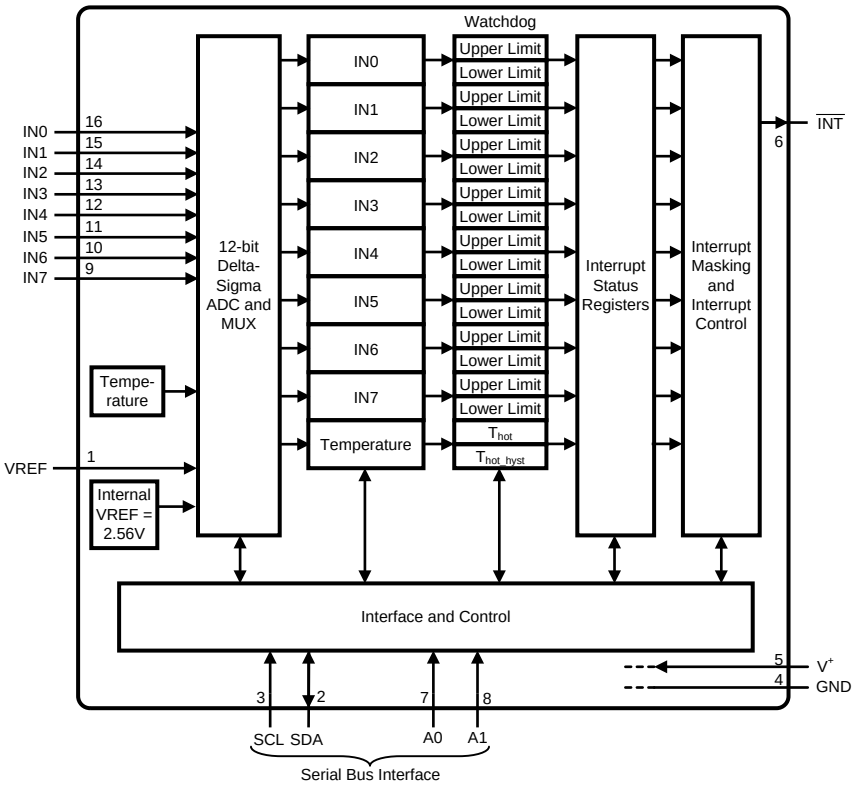
The ADC128D818 continuously converts the voltage input to 12-bit resolution with an internal VREF of 0.625-mV LSb (Least Significant bit) weighting, yielding input range of 0 V to 2.56 V. There is also an external VREF option that ranges from 1.25 V to V+. The analog inputs are intended to be connected to several power supplies present in a variety of systems. Eight inputs can be configured for single-ended and/or pseudo-differential channels. Temperature can be converted to a 9-bit two's complement word with resolutions of 0.5°C per LSb.

The ADC128D818 provides a number of internal registers. These registers are summarized in Table 19.

The ADC128D818 supports Standard Mode (Sm, 100 kbps) and Fast Mode (Fm, 400 kbps) I^2C interface modes of operation. ADC128D818 includes an analog filter on the I^2C digital control lines that allows improved noise immunity. The device also supports TIME-OUT reset function on SDA and SCL to prevent I^2C bus lock-up. Two tri-level address pins allow up to 9 devices on a single I^2C bus.

At start-up, ADC128D818 cycles through each measurement in sequence and continuously loops through the sequence based on the Conversion Rate Register (address 07h) setting. Each measured value is compared to values stored in the Limit Registers (addresses 2Ah - 39h). When the measured value violates the programmed limit, the ADC128D818 will set a corresponding interrupt bit in the Interrupt Status Registers (address 01h). An interrupt output pin, $\overline{INT}$, is also available and fully programmable.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Supply Voltage (V+)

The ADC128D818 operates with a supply voltage, V+, that has a range between 3 V to 5.5 V. Take care to bypass this pin with a parallel combination of 1-µF (electrolytic or tantalum) capacitor and 0.1-µF (ceramic) bypass capacitor.

8.3.2 Voltage References (VREF)

The reference voltage (VREF) sets the analog input range. The ADC128D818 has two options for setting VREF. The first option is to use the internal VREF, which is equal to 2.56 V. The second option is to source VREF externally through pin 1 of ADC128D818. In this case, the external VREF will operate in the range of 1.25 V to V+. The default VREF selection is the internal VREF. If the external VREF is preferred, use the *Advanced Configuration Register — Address 0Bh* to change this setting.

VREF source must have a low output impedance and needs to be bypassed with a minimum capacitor value of 0.1 µF. A larger capacitor value of 1 µF placed in parallel with the 0.1 µF is preferred. VREF of the ADC128D818, like all ADC converters, does not reject noise or voltage variations. Keep this in mind if VREF is derived from the power supply. Any noise and/or ripple from the supply that is not rejected by the external reference circuitry will appear in the digital results. The use of a reference source is recommended. The LM4040 and LM4050 shunt reference families as well as the LM4120 and LM4140 series reference families are excellent choices for a reference source.

8.3.3 Analog Inputs (IN0 - IN7)

The ADC128D818 allows up to 8 single-ended inputs or 4 pseudo-differential inputs as selected by the modes of operation. The input types are described in the next subsections.

8.3.3.1 Single-Ended Input

ADC128D818 allows a maximum of 8 single-ended inputs, where the source's voltage is connected to INx ($0 \le x \le 7$). The source's ground must be connected to ADC128D818's GND pin. In theory, INx can be of any value between 0V and (VREF-3LSb/2), where LSb = $VREF/2^{12}$.

To use the device single-endedly, refer to the *Modes of Operation* section and to bits [2:1] of the *Advanced Configuration Register — Address 0Bh*. Figure 24 shows the appropriate configuration for a single-ended connection.

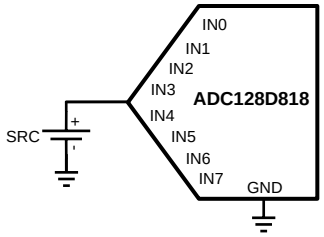


Figure 24. Single-Ended Configuration

8.3.3.2 Pseudo-Differential Input

Pseudo-differential mode is defined as the positive input voltage applied differentially to the ADC128D818, as shown in Figure 25. The input that is digitized is (ΔVIN = IN+ - IN–), where (IN+ - IN–) is (IN0-IN1), (IN3-IN2), (IN4-IN5), or (IN7-IN6). Be aware of this input configuration because the order is swapped. In theory, ΔVIN can be of any value between 0 V and (VREF – 3LSb/2), where LSb = $VREF/2^{12}$.

By using this pseudo-differential input, small signals common to both inputs are rejected. Thus, operation with a pseudo-differential input signal will provide better performance than with a single-ended input. See *Modes of Operation* for more information.

Feature Description (continued)

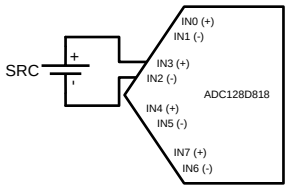


Figure 25. Pseudo-Differential Configuration

8.4 Device Functional Modes

8.4.1 Modes of Operation

ADC128D818 allows 4 modes of operation, as summarized in the following table. Set the desired mode of operation using the *Advanced Configuration Register — Address 0Bh*, bits [2:1]).

Table 1. Modes of Operation

CH.	MODE 0	MODE 1	MODE 2	MODE 3
1	IN0	IN0	IN0 (+) and IN1 (-)	IN0
2	IN1	IN1	IN3 (+) and IN2 (-)	IN1
3	IN2	IN2	IN4 (+) and IN5 (-)	IN2
4	IN3	IN3	IN7 (+) and IN6 (-)	IN3
5	IN4	IN4		IN4 (+) and IN5 (-)
6	IN5	IN5		IN7 (+) and IN6 (-)
7	IN6	IN6		
8	nc(1)	IN7		
Local Temp	Yes	No	Yes	Yes

(1) nc = No Connect

8.5 Programming

8.5.1 Interface

The Serial Bus control lines include the SDA (serial data), SCL (serial clock), and A0-A1 (Serial Bus Address) pins. The ADC128D818 can only operate as a slave. The SCL line only controls the serial interface, and all of other clock functions within ADC128D818 are done with a separate asynchronous internal clock.

When the Serial Bus Interface is used, a write will always consists of the ADC128D818 Serial Bus Address byte, followed by the Register Address byte, then the Data byte. Figure 26 and Figure 27 are two examples showing how to write to the ADC128D818.

There are two cases for a read:

1. If the Register Address is known to be at the desired address, simply read the ADC128D818 with the Serial Bus Address byte, followed by the Data byte read from the ADC128D818. Examples of this type of read can be seen in Figure 28 and Figure 29.
2. If the Register Address value is unknown, write to the ADC128D818 with the Serial Bus Address byte, followed by the desired Register Address byte. Then restart the Serial Communication with a Read consisting of the Serial Bus Address byte, followed by the Data byte read from the ADC128D818. See Figure 30 and Figure 31 for examples of this type of read.

Programming (continued)

The Serial Bus Address can be found in the next section, and the Register Address can be found in *Register Maps*. For more information on the I²C Interface, refer to NXP's "I²C-Bus Specification and User Manual", rev. 03.

8.5.1.1 Serial Bus Address

There are nine different configurations for the ADC128D818 Serial Bus Address, thus nine devices are allowed on a single I²C bus. Examples to set each address bit low, high, or to midscale can be found in *System Examples*. The Serial Bus Address can be set as follows:

Table 2. Serial Bus Address Table

A1	A0	SERIAL BUS ADDRESS [A6][A5][A4]...[A0]	SERIAL BUS ADDRESS (HEX)
LOW	LOW	001_1101b	1Dh
LOW	MID	001_1110b	1Eh
LOW	HIGH	001_1111b	1Fh
MID	LOW	010_1101b	2Dh
MID	MID	010_1110b	2Eh
MID	HIGH	010_1111b	2Fh
HIGH	LOW	011_0101b	35h
HIGH	MID	011_0110b	36h
HIGH	HIGH	011_0111b	37h

8.5.1.2 Time-out

The ADC128D818 I²C state machine resets to its idle state if either SCL or SDA is held low for longer than 35 ms. This feature also ensures that ADC128D818 will automatically release SDA after driving it low continuously for 25 to 35 ms, hence preventing I²C bus lock-up. The TIME-OUT feature should not be used when the device is operating in deep shutdown mode.

8.5.1.2.1 Example Writes and Reads

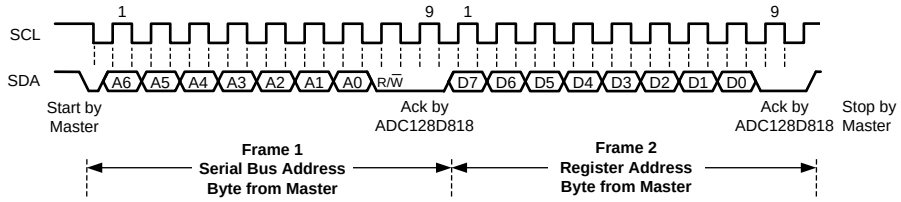


Figure 26. Serial Bus Interface Write Example 1 - Internal Address Register Set Only

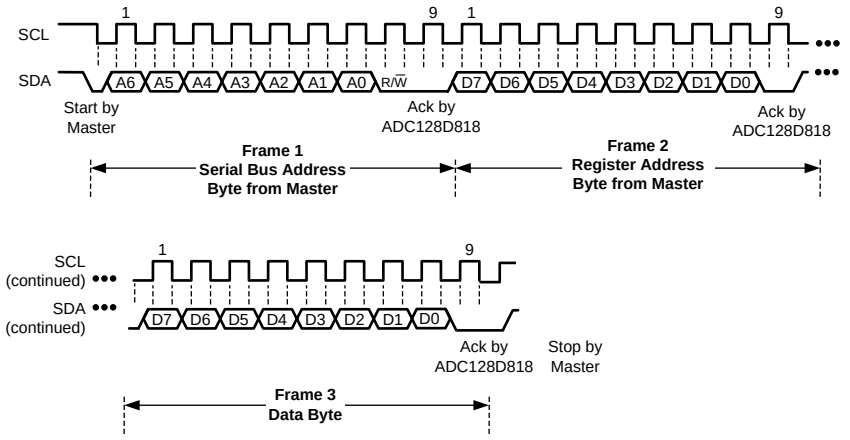


Figure 27. Serial Bus Interface Write Example 2 - Internal Address Register Set With Data Byte Write

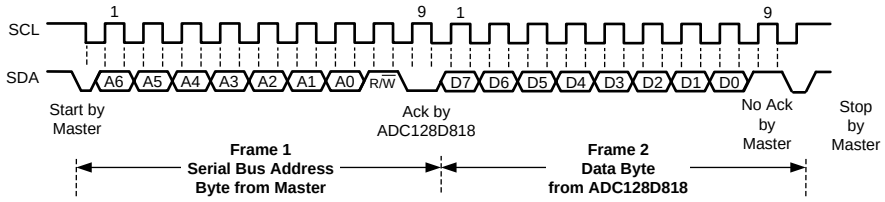


Figure 28. Serial Bus Interface Read Example 1 - Single Byte Read With Preset Internal Address Register

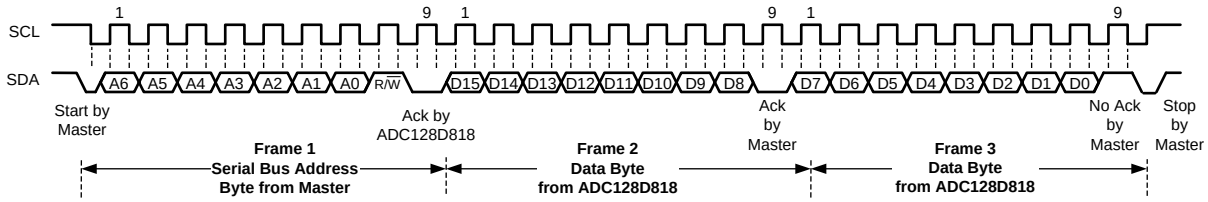


Figure 29. Serial Bus Interface Read Example 2 - Double Byte Read With Preset Internal Address Register

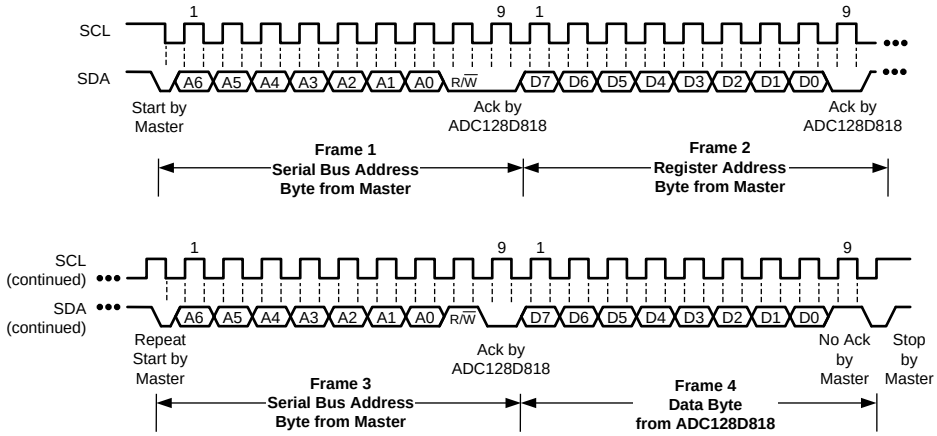


Figure 30. Serial Bus Interface Read Example 3 - Single Byte Read With Internal Address Set Using a Repeat Start

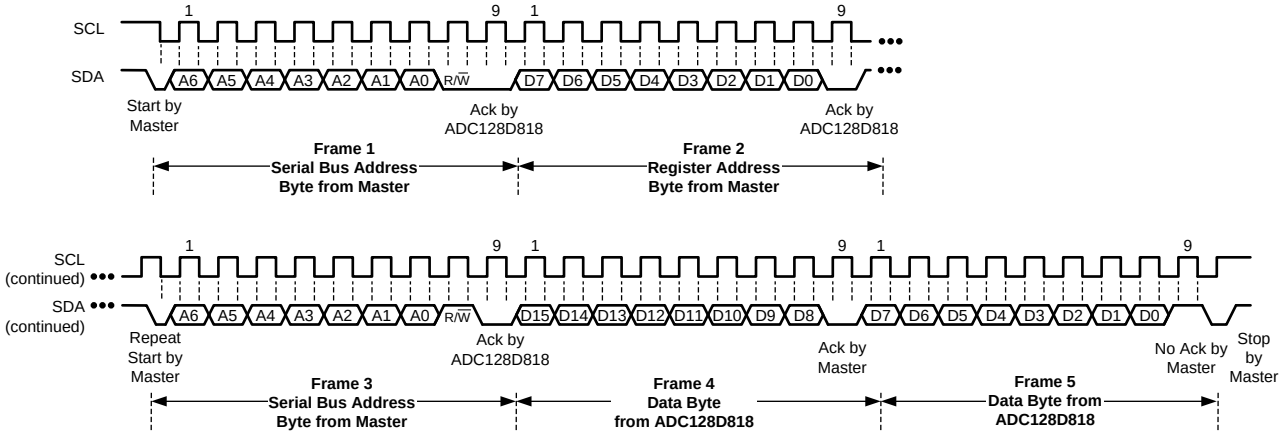


Figure 31. Serial Bus Interface Read Example 4 - Double Byte Read With Internal Address Set Using a Repeat Start

8.6 Register Maps

8.6.1 ADC128D818 Internal Registers

Table 3. ADC128D818 Internal Registers

REGISTER NAME	READ/ WRITE	REGISTER ADDRESS (HEX)	DEFAULT VALUE [7:0]	REGISTER DESCRIPTION	REGISTER FORMAT
Configuration Register	R/W	00h	0000_1000	Provides control and configuration	8-bit
Interrupt Status Register	R	01h	0000_0000	Provides status of each WATCHDOG limit or interrupt event	8-bit
Interrupt Mask Register	R/W	03h	0000_0000	Masks the interrupt status from propagating to $\overline{INT}$	8-bit
Conversion Rate Register	R/W	07h	0000_0000	Controls the conversion rate	8-bit
Channel Disable Register	R/W	08h	0000_0000	Disables conversion for each voltage or temperature channel	8-bit
One-Shot Register	W	09h	0000_0000	Initiates a single conversion of all enabled channels	8-bit
Deep Shutdown Register	R/W	0Ah	0000_0000	Enables deep shutdown mode	8-bit
Advanced Configuration Register	R/W	0Bh	0000_0000	Selects internal or external VREF and modes of operation	8-bit
Busy Status Register	R	0Ch	0000_0010	Reflects ADC128D818 'Busy' and 'Not Ready' statuses	8-bit
Channel Readings Registers	R	20h - 27h	- - -	Report the channels (voltage or temperature) readings	16-bit
Limit Registers	R/W	2Ah - 39h	- - -	Set the limits for the voltage and temperature channels	8-bit
Manufacturer ID Register	R	3Eh	0000_0001	Reports the manufacturer's ID	8-bit
Revision ID Register	R	3Fh	0000_1001	Reports the revision's ID	8-bit

8.6.2 Configuration Register — Address 00h

Default Value [7:0] = 0000_1000 binary

Table 4. Address 00h

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
ALL MODES			
0	Start	Read/Write	0: ADC128D818 in shutdown mode 1: Enable startup of monitoring operations
1	$\overline{\text{INT}}$_Enable	Read/Write	1: Enable the interrupt output pin, $\overline{\text{INT}}$
2	Reserved	Read Only	
3	$\overline{\text{INT}}$_Clear	Read/Write	1: Clear the interrupt output pin, $\overline{\text{INT}}$, without affecting the contents of Interrupt Status Registers. When this bit is set high, the device stops the round-robin monitoring loop.
4	Reserved	Read Only	
5	Reserved	Read Only	
6	Reserved	Read Only	
7	Initialization	Read/Write	1: Restore default values to the following registers: Configuration, Interrupt Status, Interrupt Mask, Conversion Rate, Channel Disable, One-Shot, Deep Shutdown, Advanced Configuration, Busy Status, Channel Readings, Limit, Manufacturer ID, Revision ID. This bit clears itself

8.6.3 Interrupt Status Register — Address 01h

Default Value [7:0] = 0000_0000 binary

Table 5. Address 01h

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
MODE 0			
0	IN0 Error	Read Only	1: A High or Low limit has been exceeded
1	IN1 Error	Read Only	1: A High or Low limit has been exceeded
2	IN2 Error	Read Only	1: A High or Low limit has been exceeded
3	IN3 Error	Read Only	1: A High or Low limit has been exceeded
4	IN4 Error	Read Only	1: A High or Low limit has been exceeded
5	IN5 Error	Read Only	1: A High or Low limit has been exceeded
6	IN6 Error	Read Only	1: A High or Low limit has been exceeded
7	Hot Temperature Error	Read Only	1: A High limit has been exceeded
MODE 1			
0	IN0 Error	Read Only	1: A High or Low limit has been exceeded
1	IN1 Error	Read Only	1: A High or Low limit has been exceeded
2	IN2 Error	Read Only	1: A High or Low limit has been exceeded
3	IN3 Error	Read Only	1: A High or Low limit has been exceeded
4	IN4 Error	Read Only	1: A High or Low limit has been exceeded
5	IN5 Error	Read Only	1: A High or Low limit has been exceeded
6	IN6 Error	Read Only	1: A High or Low limit has been exceeded
7	IN7 Error	Read Only	1: A High or Low limit has been exceeded
MODE 2			
0	IN0(+) and IN1(-) Error	Read Only	1: A High or Low limit has been exceeded
1	IN3(+) and IN2(-) Error	Read Only	1: A High or Low limit has been exceeded
2	IN4(+) and IN5(-) Error	Read Only	1: A High or Low limit has been exceeded
3	IN7(+) and IN6(-) Error	Read Only	1: A High or Low limit has been exceeded
4	Reserved	Read Only	
5	Reserved	Read Only	
6	Reserved	Read Only	

Table 5. Address 01h (continued)

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
7	Hot Temperature Error	Read Only	1: A High limit has been exceeded
MODE 3			
0	IN0 Error	Read Only	1: A High or Low limit has been exceeded
1	IN1 Error	Read Only	1: A High or Low limit has been exceeded
2	IN2 Error	Read Only	1: A High or Low limit has been exceeded
3	IN3 Error	Read Only	1: A High or Low limit has been exceeded
4	IN4(+) and IN5(-) Error	Read Only	1: A High or Low limit has been exceeded
5	IN7(+) and IN6(-) Error	Read Only	1: A High or Low limit has been exceeded
6	Reserved	Read Only	
7	Hot Temperature Error	Read Only	1: A High limit has been exceeded

8.6.4 Interrupt Mask Register — Address 03h

Default Value [7:0] = 0000_0000 binary

Table 6. Address 03h

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
MODE 0			
0	IN0 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
1	IN1 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
2	IN2 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
3	IN3 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
4	IN4 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
5	IN5 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
6	IN6 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
7	Temperature Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
MODE 1			
0	IN0 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
1	IN1 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
2	IN2 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
3	IN3 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
4	IN4 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
5	IN5 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
6	IN6 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
7	IN7 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
MODE 2			
0	IN0(+) and IN1(-) Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$

Table 6. Address 03h (continued)

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
1	IN3(+) and IN2(-) Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
2	IN4(+) and IN5(-) Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
3	IN7(+) and IN6(-) Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
4	Reserved	Read Only	
5	Reserved	Read Only	
6	Reserved	Read Only	
7	Temperature Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
MODE 3			
0	IN0 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
1	IN1 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
2	IN2 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
3	IN3 Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
4	IN4(+) and IN5(-) Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
5	IN7(+) and IN6(-) Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$
6	Reserved	Read Only	
7	Temperature Mask	Read/Write	1: Mask the corresponding interrupt status from propagating to the interrupt output pin, $\overline{INT}$

8.6.5 Conversion Rate Register — Address 07h

Default Value [7:0] = 0000_0000 binary

Table 7. Address 07h

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
0	Conversion Rate	Read/Write	Controls the conversion rate: 0: Low Power Conversion Mode 1: Continuous Conversion Mode Note: This register must only be programmed when the device is in shutdown mode, that is, when the 'START' bit of the 'Configuration Register' (address 00h) = 0
1–7	Reserved	Read Only	

8.6.6 Channel Disable Register — Address 08h

Default Value [7:0] = 0000_0000 binary

- This register must only be programmed when the device is in shutdown mode, that is, when the ‘START’ bit of the “Configuration Register’ (address 00h) = 0.
- Whenever this register is programmed, all of the values in the Channel Reading Registers and Interrupt Status Registers will return to their default values.

Table 8. Address 08h

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
MODE 0			
0	IN0 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.

Table 8. Address 08h (continued)

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
1	IN1 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
2	IN2 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed
3	IN3 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
4	IN4 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
5	IN5 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
6	IN6 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
7	Temperature Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
MODE 1			
0	IN0 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
1	IN1 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
2	IN2 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
3	IN3 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
4	IN4 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
5	IN5 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
6	IN6 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
7	IN7 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
MODE 2			
0	IN0(+) and IN1(-) Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
1	IN3(+) and IN2(-) Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
2	IN4(+) and IN5(-) Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
3	IN7(+) and IN6(-) Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
4	Reserved	Read Only	
5	Reserved	Read Only	
6	Reserved	Read Only	
7	Temperature Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
MODE 3			
0	IN0 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
1	IN1 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
2	IN2 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
3	IN3 Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.

Table 8. Address 08h (continued)

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
4	IN4(+) and IN5(-) Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
5	IN7(+) and IN6(-) Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.
6	Reserved	Read Only	
7	Temperature Disable	Read/Write	1: Conversions are skipped and disabled, value register reading will be 0, and error events will be suppressed.

8.6.7 One-Shot Register — Address 09h

Default Value [7:0] = 0000_0000 binary

Table 9. Address 09h

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
0	One-Shot	Write Only	1: Initiate a single conversion and comparison cycle when the device is in shutdown mode or deep shutdown mode, after which the device returns to the respective mode that it was in
1–7	Reserved	Read Only	

8.6.8 Deep Shutdown Register — Address 0Ah

Default Value [7:0] = 0000_0000 binary

Table 10. Address 0Ah

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
0	Deep Shutdown Enable	Read/Write	1: When 'START' = 0 (address 00h, bit 0), setting this bit high will place the device in deep shutdown mode
1–7	Reserved	Read Only	

8.6.9 Advanced Configuration Register — Address 0Bh

Default Value [7:0] = 0000_0000 binary

Note: Whenever the Advanced Configuration Register is programmed, all of the values in the Channel Reading Registers and Interrupt Status Registers will return to their default values.

Table 11. Address 0Bh

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION		
0	External Reference Enable	Read/Write	0: Selects the 2.56V internal VREF 1: Selects the variable external VREF		
1	Mode Select [0]	Read/Write	Mode Select [1]	Mode Select [0]	Mode
			0	0	Mode 0
			0	1	Mode 1
			1	0	Mode 2
2	Mode Select [1]		1	1	Mode 3
3–7	Reserved	Read Only			

8.6.10 Busy Status Register — Address 0Ch

Default Value [7:0] = 0000_0010 binary

Table 12. Address 0Ch

BIT	BIT NAME	READ/WRITE	BIT DESCRIPTION
0	Busy	Read Only	1: ADC128D818 is converting
1	Not Ready	Read Only	1: Waiting for the power-up sequence to end
2–7	Reserved	Read Only	

8.6.11 Channel Readings Registers — Addresses 20h – 27h

ADDRESS	REGISTER NAME	READ/WRITE	REGISTER DESCRIPTION
MODE 0			
20h	IN0 Reading	Read Only	Reading for this perspective channel
21h	IN1 Reading	Read Only	Reading for this perspective channel
22h	IN2 Reading	Read Only	Reading for this perspective channel
23h	IN3 Reading	Read Only	Reading for this perspective channel
24h	IN4 Reading	Read Only	Reading for this perspective channel
25h	IN5 Reading	Read Only	Reading for this perspective channel
26h	IN6 Reading	Read Only	Reading for this perspective channel
27h	Temperature Reading	Read Only	Reading for this perspective channel
MODE 1			
20h	IN0 Reading	Read Only	Reading for this perspective channel
21h	IN1 Reading	Read Only	Reading for this perspective channel
22h	IN2 Reading	Read Only	Reading for this perspective channel
23h	IN3 Reading	Read Only	Reading for this perspective channel
24h	IN4 Reading	Read Only	Reading for this perspective channel
25h	IN5 Reading	Read Only	Reading for this perspective channel
26h	IN6 Reading	Read Only	Reading for this perspective channel
27h	IN7 Reading	Read Only	Reading for this perspective channel
MODE 2			
20h	IN0(+) and IN1(-) Reading	Read Only	Reading for this perspective channel
21h	IN3(+) and IN2(-) Reading	Read Only	Reading for this perspective channel
22h	IN4(+) and IN5(-) Reading	Read Only	Reading for this perspective channel
23h	IN7(+) and IN6(-) Reading	Read Only	Reading for this perspective channel
24h	Reserved	Read Only	
25h	Reserved	Read Only	
26h	Reserved	Read Only	
27h	Temperature Reading	Read Only	Reading for this perspective channel
MODE 3			
20h	IN0 Reading	Read Only	Reading for this perspective channel
21h	IN1 Reading	Read Only	Reading for this perspective channel
22h	IN2 Reading	Read Only	Reading for this perspective channel
23h	IN3 Reading	Read Only	Reading for this perspective channel
24h	IN4(+) and IN5(-) Reading	Read Only	Reading for this perspective channel
25h	IN7(+) and IN6(-) Reading	Read Only	Reading for this perspective channel
26h	Reserved	Read Only	
27h	Temperature Reading	Read Only	Reading for this perspective channel

8.6.12 Limit Registers — Addresses 2Ah – 39h

Table 13. Addresses 2Ah – 39h

ADDRESS	REGISTER NAME	READ/WRITE	REGISTER DESCRIPTION
MODE 0			
2Ah	IN0 High Limit	Read/Write	High Limit
2Bh	IN0 Low Limit	Read/Write	Low Limit
2Ch	IN1 High Limit	Read/Write	High Limit
2Dh	IN1 Low Limit	Read/Write	Low Limit
2Eh	IN2 High Limit	Read/Write	High Limit
2Fh	IN2 Low Limit	Read/Write	Low Limit
30h	IN3 High Limit	Read/Write	High Limit
31h	IN3 Low Limit	Read/Write	Low Limit
32h	IN4 High Limit	Read/Write	High Limit
33h	IN4 Low Limit	Read/Write	Low Limit
34h	IN5 High Limit	Read/Write	High Limit
35h	IN5 Low Limit	Read/Write	Low Limit
36h	IN6 High Limit	Read/Write	High Limit
37h	IN6 Low Limit	Read/Write	Low Limit
38h	Temperature High Limit	Read/Write	High Limit
39h	Temperature Hysteresis Limit	Read/Write	Hysteresis Limit
MODE 1			
2Ah	IN0 High Limit	Read/Write	High Limit
2Bh	IN0 Low Limit	Read/Write	Low Limit
2Ch	IN1 High Limit	Read/Write	High Limit
2Dh	IN1 Low Limit	Read/Write	Low Limit
2Eh	IN2 High Limit	Read/Write	High Limit
2Fh	IN2 Low Limit	Read/Write	Low Limit
30h	IN3 High Limit	Read/Write	High Limit
31h	IN3 Low Limit	Read/Write	Low Limit
32h	IN4 High Limit	Read/Write	High Limit
33h	IN4 Low Limit	Read/Write	Low Limit
34h	IN5 High Limit	Read/Write	High Limit
35h	IN5 Low Limit	Read/Write	Low Limit
36h	IN6 High Limit	Read/Write	High Limit
37h	IN6 Low Limit	Read/Write	Low Limit
38h	IN7 High Limit	Read/Write	High Limit
39h	IN7 Low Limit	Read/Write	Low Limit
MODE 2			
2Ah	IN0(+) and IN1(-) High Limit	Read/Write	High Limit
2Bh	IN0(+) and IN1(-) Low Limit	Read/Write	Low Limit
2Ch	IN3(+) and IN2(-) High Limit	Read/Write	High Limit
2Dh	IN3(+) and IN2(-) Low Limit	Read/Write	Low Limit
2Eh	IN4(+) and IN5(-) High Limit	Read/Write	High Limit
2Fh	IN4(+) and IN5(-) Low Limit	Read/Write	Low Limit
30h	IN7(+) and IN6(-) High Limit	Read/Write	High Limit
31h	IN7(+) and IN6(-) Low Limit	Read/Write	Low Limit
32h	Reserved	Read Only	
33h	Reserved	Read Only	
34h	Reserved	Read Only	

Table 13. Addresses 2Ah – 39h (continued)

ADDRESS	REGISTER NAME	READ/WRITE	REGISTER DESCRIPTION
35h	Reserved	Read Only	
36h	Reserved	Read Only	
37h	Reserved	Read Only	
38h	Temperature High Limit	Read/Write	High Limit
39h	Temperature Hysteresis Limit	Read/Write	Hysteresis Limit
MODE 3			
2Ah	IN0 High Limit	Read/Write	High Limit
2Bh	IN0 Low Limit	Read/Write	Low Limit
2Ch	IN1 High Limit	Read/Write	High Limit
2Dh	IN1 Low Limit	Read/Write	Low Limit
2Eh	IN2 High Limit	Read/Write	High Limit
2Fh	IN2 Low Limit	Read/Write	Low Limit
30h	IN3 High Limit	Read/Write	High Limit
31h	IN3 Low Limit	Read/Write	Low Limit
32h	IN4(+) and IN5(-) High Limit	Read/Write	High Limit
33h	IN4(+) and IN5(-) Low Limit	Read/Write	Low Limit
34h	IN7(+) and IN6(-) High Limit	Read/Write	High Limit
35h	IN7(+) and IN6(-) Low Limit	Read/Write	Low Limit
36h	Reserved	Read Only	
37h	Reserved	Read Only	
38h	Temperature High Limit	Read/Write	High Limit
39h	Temperature Hysteresis Limit	Read/Write	Hysteresis Limit

8.6.13 Manufacturer ID Register — Address 3Eh

Default Value [7:0] = 0000_0001 binary

Table 14. Address 3Eh

ADDRESS	REGISTER NAME	READ/WRITE	REGISTER DESCRIPTION
3Eh	Manufacturer ID	Read Only	Manufacturer's ID always defaults to 0000_0001.

8.6.14 Revision ID Register — Addresses 3Fh

Default Value [7:0] = 0000_1001 binary

Table 15. Addresses 3Fh

ADDRESS	REGISTER NAME	READ/WRITE	REGISTER DESCRIPTION
3Fh	Revision ID	Read Only	Revision's ID always defaults to 0000_1001.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Digital Output (D_{OUT})

The digital output code for a 12-bit ADC can be calculated as:

$$D_{OUT} = [\Delta VIN / VREF] \times 2^{12} \quad (1)$$

For Equation 1, ΔVIN = INx – GND, where 0 ≤ x ≤ 7, for the single-ended configuration, and ΔVIN = (IN+ - IN–) for the pseudo-differential configuration. In theory, ΔVIN can be of any value between 0 V and (VREF-3LSb/2). Any ΔVIN value outside of this range will produce a digital output code of 0 or 4095. Figure 32 shows a theoretical plot of D_{OUT} vs. ΔVIN and some sample D_{OUT} calculation using Equation 1.

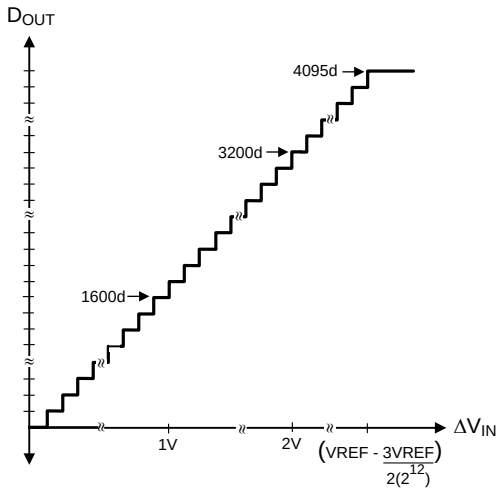
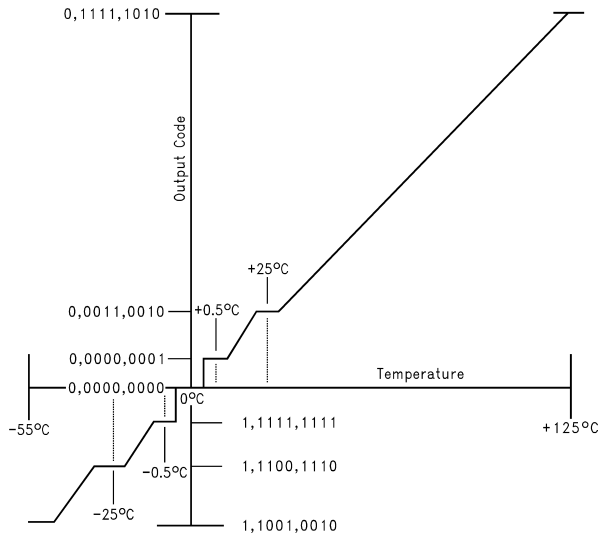


Figure 32. D_{OUT} vs ΔVIN for a 12-Bit ADC Assuming VREF = 2.56 V.

9.1.2 Temperature Measurement System

The ADC128D818 delta-V_{BE} type temperature sensor and delta-sigma ADC perform 9-bit two's-complement conversions of the temperature. This temperature reading can be obtained at the Temperature Reading Register (address 27h). This register is 16-bit wide, and thus, all 9 bits of the temperature reading can be read using a double byte read (Figure 29 or Figure 31). The following Figure 33 and Figure 33 show the theoretical output code (D_{OUT}) vs. temperature and some typical temperature-to-code conversions.

Application Information (continued)



(Non-Linear Scale for Clarity)

Figure 33. 9-Bit Temperature-to-Digital Transfer Function

Table 16. Temperature Registers Sample Temperatures

TEMP	DIGITAL OUTPUT (D_{OUT})		
	BINARY [MSb...LSb]	DECIMAL	HEX
+125°C	0 _1111_1010	250	0_FA
+25°C	0_0011_0010	50	0_32
+0.5°C	0_0000_0001	1	0_01
+0°C	0_0000_0000	0	0_00
−0.5°C	1_1111_1111	511	1_FF
−25°C	1_1100_1110	462	1_CE
−40°C	1_1011_0000	432	1_B0

In general, the easiest way to calculate the temperature (°C) is to use the following formulas:

If D_{OUT}[MSb] = 0: + Temp(°C) = D_{OUT}(dec) / 2 (2)

If D_{OUT}[MSb] = 1: – Temp(°C) = [2^9 – D_{OUT}(dec)] / 2 (3)

9.1.2.1 Temperature Limits

One of the ADC128D818 features is monitoring the temperature reading. This monitoring is accomplished by setting a temperature limit to the Temperature High Limit Register (T_{hot} , address 38h) and Temperature Hysteresis Limit Register (T_{hot_hyst}, address 39h). When the temperature reading > T_{hot}, an interrupt occurs. How this interrupt occurs will be explained in *Temperature Interrupt*.

Each temperature limit is represented by an 8-bit, two's complement word with a least significant bit (LSb) equal to 1°C. Table 17 shows some sample temperatures that can be programmed to the Temperature Limit Registers.

In general, use the following equations to calculate the digital code that represents the desired temperature limit:

If Temp Limit (°C) ≥ 0: Digital Code (dec) = Temp Limit(°C) (4)

If Temp Limit (°C) < 0: Digital Code (dec) = 2^8 – |Temp Limit(°C)| (5)

Table 17. Temperature Limit Registers Sample Temperatures

TEMP LIMIT	DIGITAL CODE		
	BINARY [MSb...LSb]	DECIMAL	HEX
+125°C	0111_1101	125	7D
+25°C	0001_1001	25	19
+1.0°C	0000_0001	1	01
+0°C	0000_0000	0	00
−1.0°C	1111_1111	255	FF
−25°C	1110_1111	231	E7
−40°C	1101_1000	216	D8

9.1.3 Interrupt Structure

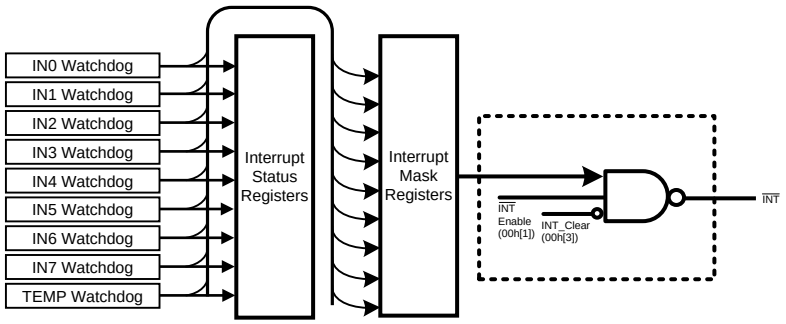


Figure 34. Interrupt Structure

Figure 34 shows the ADC128D818's Interrupt Structure.

NOTE

The number next to each bit name represents its register address and bit number. For example, 'INT_Clear' (00h[3]) refers to bit 3 of register address 00h.

9.1.3.1 Interrupt Output ($\overline{INT}$)

ADC128D818 generates an interrupt as a result of each of its internal WATCHDOG registers on the voltage and temperature channels. In general, $\overline{INT}$ becomes active when all three scenarios, as depicted in Figure 34, occur:

1. '$\overline{INT}$_Clear' (00h[3]) = 0.
2. '$\overline{INT}$_Enable' (00h[1]) = 1 to enable interrupt output.
3. The voltage reading > the voltage high limit or ≤ the voltage low limit, or the temperature reading > T_{hot}.

9.1.3.2 Interrupt Clearing

Reading the Interrupt Status Register (addresses 01h) will output the contents of the register and clear the register. When the Interrupt Status Register clears, the interrupt output pin, $\overline{INT}$, also clears until this register is updated by the round-robin monitoring loop.

Another method to clear the interrupt output pin, $\overline{INT}$, is setting '$\overline{INT}$_Clear' bit (address 00h, bit 3) = 1. When this bit is high, the ADC128D818 round-robin monitoring loop will stop.

9.1.3.3 Temperature Interrupt

One of the ADC128D818 features is monitoring the temperature reading. This monitoring is accomplished by setting a temperature limit to the Temperature High Limit Register (T_{hot} , address 38h) and Temperature Hysteresis Limit Register (T_{hot_hyst}, address 39h). These limit registers have an interrupt mode, shown in Figure 35, that operates in the following way: if the temperature reading > T_{hot}, an interrupt will occur and will remain active indefinitely until reset by reading the Interrupt Status Register (address 01h) or cleared by the 'INT_Clear' bit.

Once an interrupt event has occurred by crossing T_{hot}, then reset, an interrupt will occur again once the next temperature conversion has completed. The interrupts will continue to occur in this manner until the temperature reading is ≤ T_{hot_hyst} and a read of the Interrupt Status Register has occurred.

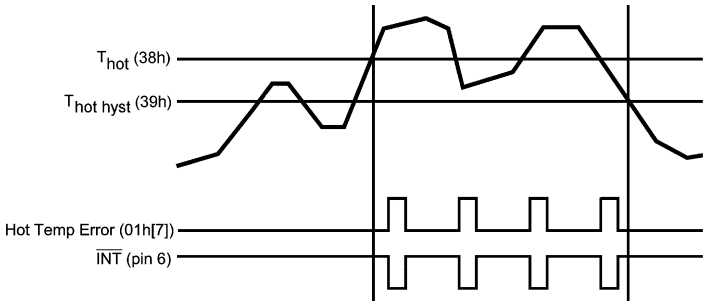


Figure 35. Temperature Response Structure
(Assuming the Interrupt Output Pin, INT, is Reset Before the Next Temperature Reading)

9.2 Typical Application

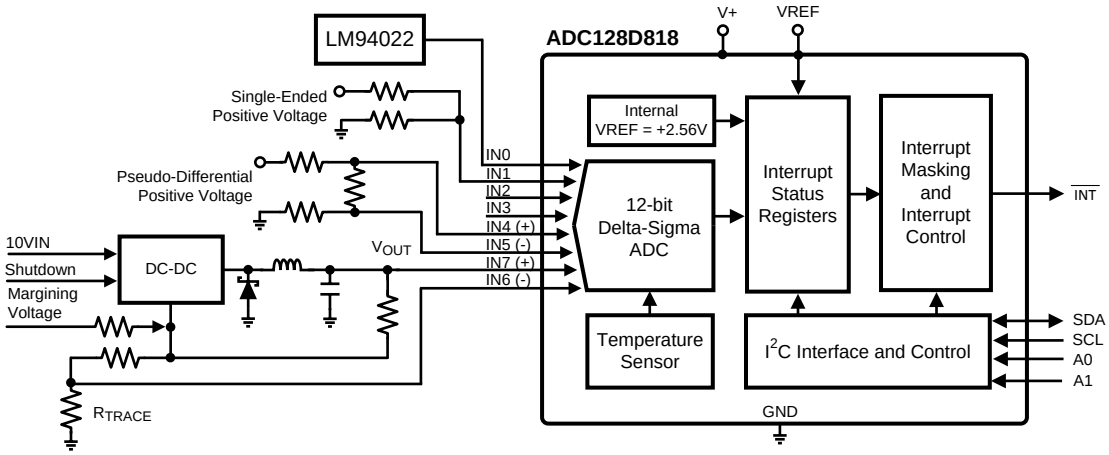


Figure 36. Hardware Monitor Application

9.2.1 Design Requirements

In this typical hardware monitor application, several different sources are being monitored by the ADC128D818. First, an external temperature sensor (LM94022) is being monitored. An external temperature sensor is frequently used to monitor ambient temperature of the system.

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Power Management

To understand the average supply current (I+), the conversion rates must be introduced. ADC128D818 has three types of conversion rates: Continuous Conversion Mode, Low Power Conversion Mode, and One Shot Mode. In the Low Power Conversion Mode, the device converts all of the enabled channels then enters shutdown mode; this process takes approximately 728 ms to complete. (More information on the conversion rate will be discussed in the *Conversion Rate Register — Address 07h* and *One-Shot Register — Address 09h* sections).

Each type of conversion produces a different average supply current. The supply current for a voltage conversion will be referred to as I+_VOLTAGE, a temperature conversion as I+_TEMP, and the shutdown mode as I+_SHUTDOWN. These values can be obtained from Typical Performance Characteristics plots.

In general, I+ is the average supply current while ADC128D818 is operating in the Low Power Conversion Mode with all of the available channels enabled. Its plot can be seen in *Typical Characteristics* and its equation, Equation 6.

$$I+ = [(0.0168)(b)(I^+\_VOLTAGE)] + [(4.932)(10^{-3})(a)(I^+\_TEMP)]$$
$$+ [1 – (4.932)(10^{-3})(a) – 0.0168(b)](I^+\_SHUTDOWN) \quad (6)$$

where

- a is the number of local temperature available.
- b is the number of ENABLED voltage channel.

Each mode of operation has a different "a" and "b" values. The following table shows the value for "a" and the maximum value for "b" for each mode.

Table 18. "A" and "B" Values

	a	b (MAX)
Mode 0	1	7
Mode 1	0	8
Mode 2	1	4
Mode 3	1	6

9.2.2.2 Using the ADC128D818

Table 19. ADC128D818 Internal Registers

REGISTER NAME	READ/ WRITE	REGISTER ADDRESS (HEX)	DEFAULT VALUE [7:0]	REGISTER DESCRIPTION	REGISTER FORMAT
Configuration Register	R/W	00h	0000_1000	Provides control and configuration	8-bit
Interrupt Status Register	R	01h	0000_0000	Provides status of each WATCHDOG limit or interrupt event	8-bit
Interrupt Mask Register	R/W	03h	0000_0000	Masks the interrupt status from propagating to $\overline{INT}$	8-bit
Conversion Rate Register	R/W	07h	0000_0000	Controls the conversion rate	8-bit
Channel Disable Register	R/W	08h	0000_0000	Disables conversion for each voltage or temperature channel	8-bit
One-Shot Register	W	09h	0000_0000	Initiates a single conversion of all enabled channels	8-bit
Deep Shutdown Register	R/W	0Ah	0000_0000	Enables deep shutdown mode	8-bit
Advanced Configuration Register	R/W	0Bh	0000_0000	Selects internal or external VREF and modes of operation	8-bit
Busy Status Register	R	0Ch	0000_0010	Reflects the ADC128D818 'Busy' and 'Not Ready' statuses	8-bit
Channel Readings Registers	R	20h - 27h	- - -	Report channels (voltage or temperature) readings	16-bit

Table 19. ADC128D818 Internal Registers (continued)

REGISTER NAME	READ/ WRITE	REGISTER ADDRESS (HEX)	DEFAULT VALUE [7:0]	REGISTER DESCRIPTION	REGISTER FORMAT
Limit Registers	R/W	2Ah - 39h	- - -	Set the limits for the voltage and temperature channels	8-bit
Manufacturer ID Register	R	3Eh	0000_0001	Reports the manufacturer's ID	8-bit
Revision ID Register	R	3Fh	0000_1001	Reports the revision's ID	8-bit

9.2.2.2.1 Quick Start

1. Power on the device, then wait for at least 33ms.
2. Read the Busy Status Register (address 0Ch). If the 'Not Ready' bit = 1, then increase the wait time until 'Not Ready' bit = 0 before proceeding to the next step.
3. Program the *Advanced Configuration Register — Address 0Bh*:
   – a. Choose to use the internal or external VREF (bit 0).
   – b. Choose the mode of operation (bits [2:1]).
4. Program the Conversion Rate Register (address 07h).
5. Choose to enable or disable the channels using the Channel Disable Register (address 08h).
6. Using the Interrupt Mask Register (address 03h), choose to mask or not to mask the interrupt status from propagating to the interrupt output pin, $\overline{INT}$.
7. Program the Limit Registers (addresses 2Ah – 39h).
8. Set the 'START' bit of the Configuration Register (address 00h, bit 0) to 1.
9. Set the '$\overline{INT}$_Clear' bit (address 00h, bit 3) to 0. If needed, program the '$\overline{INT}$_Enable' bit (address 00h, bit 1) to 1 to enable the $\overline{INT}$ output.

The ADC128D818 then performs a round-robin monitoring of enabled voltage and temperature channels. The sequence of items being monitored corresponds to locations in the Channel Readings Registers (except for the temperature reading). Detailed descriptions of the register map can be found at the end of this data sheet.

9.2.2.2.2 Poweron Reset (POR)

When power is first applied, the ADC128D818 performs a power on reset (POR) on several of its registers, which sets the registers to their default values. These default values are shown in Table 19 or in *Register Maps*.

Registers whose default values are not shown have power on conditions that are indeterminate.

9.2.2.2.3 Configuration Register (address 00h)

The Configuration Register (address 00h) provides all control to the ADC128D818. After POR, the 'START' bit (bit 0) is set low and the '$\overline{INT}$_Clear' bit (bit 3) is set high.

The Configuration Register has the ability to start and stop the ADC128D818, enable and disable the $\overline{INT}$ output, and set the registers to their default values.

- Bit 0, 'START', controls the monitoring loop of the ADC128D818. After POR, set this bit high to start conversion. Setting this bit low stops the ADC128D818 monitoring loop and puts the ADC128D818 in shutdown mode; thus, reducing power consumption. Even though this bit is set low, serial bus communication is possible with any register in the ADC128D818.
  – After an interrupt occurs, the $\overline{INT}$ pin will not be cleared if the user sets this bit low.
- Bit 1, '$\overline{INT}$_Enable', enables the interrupt output pin, $\overline{INT}$, when this bit is set high.
- Bit 3, '$\overline{INT}$_Clear', clears the interrupt output pin, $\overline{INT}$, when this bit is set high. When this bit is set high, the ADC128D818 monitoring function will stop. The content of the Interrupt Status Register (address 01h) will not be affected.
- Bit 7, 'INITIALIZATION', accomplishes the same function as POR, that is, it initializes some of the registers to their default values. This bit automatically clears after being set high. Setting this bit high, however, does not reset the Channel Readings Registers (addresses 20h - 27h) and the Limit Registers (addresses 2Ah - 39h). These registers will be indeterminate immediately after power on. If the Channel Readings Registers contain valid conversion results and/or the Limit Registers have been previously set, they will not be affected by this

bit.

9.2.2.2.4 Interrupt Status Register (address 01h)

Each bit in this read-only register indicates whether the voltage reading > the voltage high limit or ≤ the voltage low limit, or the temperature reading > the temperature high limit. For example, if "IN0 High Limit" register (address 2Ah) were set to 2 V and if IN0 reading (address 20h) were 2.56 V, then bit 'IN0 Error' would be 1, indicating that the voltage high limit has been exceeded.

9.2.2.2.5 Interrupt Mask Register (address 03h)

This register masks the interrupt status from propagating to the interrupt output pin, $\overline{INT}$. For example, if bit 'IN0 Mask' = 1, then the interrupt output pin, $\overline{INT}$, would not be pulled low even if an error event occurs at IN0.

9.2.2.2.6 Conversion Rate Register (address 07h)

There are three options for controlling the conversion rate. The first option is called the Low Power Conversion Mode, where the device converts all of the enabled channels then enters shutdown mode. This process takes approximately 728 ms to complete.

The second option is the Continuous Conversion Mode, where the device continuously converts the enabled channels, thus never entering shutdown mode. A voltage conversion takes 12.2 ms, and a temperature conversion takes 3.6 ms. For example, if operating in mode 2 and three voltage channels were enabled, then each round-robin monitor would take 40.2 ms (3 x 12.2ms + 3.6ms) to complete. Use the "Channel Disable Register" (address 08h) to disable the desired channel(s).

The third option is called the ON-Shot mode, which will be discussed in the next subsection.

9.2.2.2.7 One-Shot Register (address 09h)

The One-Shot register is used to initiate a single conversion and comparison cycle when the device is in shutdown mode or deep shutdown mode, after which the device returns to the respective mode it was in. The obvious advantage of using this mode is lower power consumption because the device is operating in shutdown or deep shutdown mode.

This register is not a data register, and it is the write operation that causes the one-shot conversion. The data written to this address is irrelevant and is not stored. A zero will always be read from this register.

9.2.2.2.8 Deep Shutdown Register (address 0Ah)

The ADC128D818 can be placed in deep shutdown mode, thus reducing more power consumption. The procedures for deep shutdown entrance are:

1. Enter shutdown by setting the ‘START’ bit of the “Configuration Register’ (address 00h, bit 0) to 0.
2. Enter deep shutdown by setting the ‘DEEP SHUTDOWN’ bit (address 0Ah, bit 0) to 1.
3. A one-shot conversion can be triggered by writing any values to register address 09h.

Deep Shutdown Exit Procedure:

1. Set the ‘DEEP SHUTDOWN’ bit to 0.

9.2.2.2.9 Channel Readings Registers (addresses 20h - 27h)

The channel conversion readings are available in registers 20h to 27h. Each register is 16-bit wide to accommodate the 12-bit voltage reading or 9-bit temperature reading. Conversions can be read at any time and will provide the result of the last conversion. If a conversion is in progress while a communication is started, that conversion will be completed, and the Channel Reading Registers will not be updated until the communication is complete.

9.2.3 Application Curve

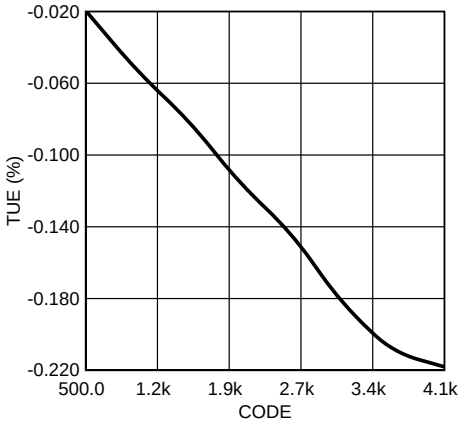


Figure 37. Total Unadjusted Error

9.3 System Examples

9.3.1 General Voltage Monitoring

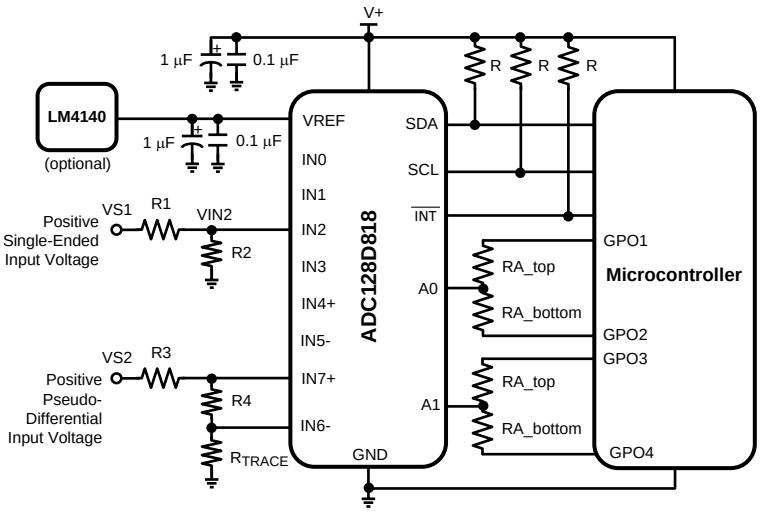


Figure 38. Typical Analog Input Application

A typical application for ADC128D818 is voltage monitoring. In this application, the inputs would most often be connected to linear power supplies of 2.5-V, 3.3-V, ±5-V and ±12-V inputs. These inputs must be attenuated with external resistors to any desired value within the input range. The attenuation is done with resistors R1 and R2 for the positive single-ended voltage, and R3 and R4 for the positive pseudo-differential voltage.

A typical single-ended application might select the input voltage divider to provide 1.9 V at the analog input of the ADC128D818. This is sufficiently high for good resolution of the voltage, yet leaves headroom for upward excursions from the supply of about 25%. To simplify the process of resistor selection, set the value of R2 first. Select a value for R2 between 10 kΩ and 100 kΩ. This is low enough to avoid errors due to input leakage currents yet high enough to protect both the inputs under and overdrive conditions as well as minimize loading of the source. Finally, calculate R1 to provide a 1.9-V input using simple voltage divider derived formula:

$$R1 = [(VS1 - VIN2) / VIN2] \times R2 \quad (7)$$

System Examples (continued)

Take care to bypass V+ with decoupling 0.1-µF ceramic capacitor and 1-µF tantalum capacitor. If using the external reference option, VREF must be connected to a voltage reference, such as the LM4140, and must also be decoupled to the ground plane by a 0.1-µF ceramic capacitor and a 1-µF tantalum capacitor. For both supplies, the 0.1-µF capacitor must be located as close as possible to the ADC128D818.

Since SDA, SCL, and $\overline{\text{INT}}$ are open-drain pins, they must have external pullup resistors to ensure that the bus is pulled high until a master device or slave device sinks enough current to pull the bus low. A typical pullup resistor, R, ranges from 1.1 kΩ to 10 kΩ. Refer to NXP's "I2C-Bus Specification and User Manual" for more information on sizing R.

Because there are two tri-level address pins (A0 and A1), up to 9 devices can share the same I^2C bus. A trick to set these serial addresses uses four GPO (general purpose output) pins from the master device as shown in the example diagram. Table 20 shows how to program these GPO pins.

Table 20. Setting Serial Bus Address Using GPO

A1	A0	GPO1	GPO2	GPO3	GPO4
LOW	LOW	Z	LOW	Z	LOW
LOW	MID	Z	LOW	HIGH	LOW
LOW	HIGH	Z	LOW	HIGH	Z
MID	LOW	HIGH	LOW	Z	LOW
MID	MID	HIGH	LOW	HIGH	LOW
MID	HIGH	HIGH	LOW	HIGH	Z
HIGH	LOW	HIGH	Z	Z	LOW
HIGH	MID	HIGH	Z	HIGH	LOW
HIGH	HIGH	HIGH	Z	HIGH	Z

9.3.2 Voltage Monitoring for Power Supplies

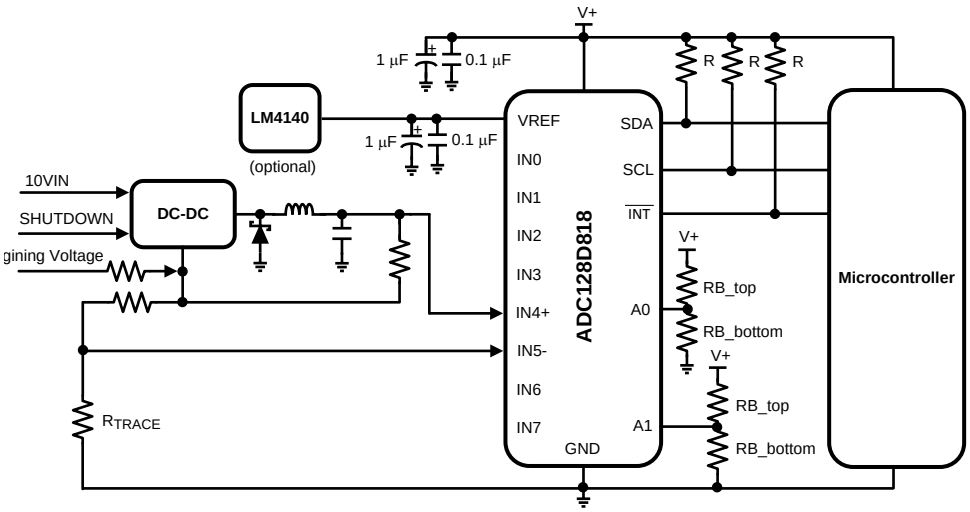


Figure 39. Power Supply Application

Figure 39 shows a more complete systems application using a DC–DC converter. Such configuration can be used in a power supply application. The point to make with this example diagram is the Serial Bus Address connections. The previous example shows A0 and A1 connected to four GPOs, but this example shows a simpler A0 and A1 connection using two resistor dividers. This connection accomplishes the same goal as the GPO connection, that is, it can set A0 and A1 high, low, or to midscale.

For example, to set A0 high, don't populate RB_bottom; to set A0 low, don't populate RB_top; and to set A0 to midscale, leave RB_top and RB_bottom as is and set them equal to each other. A typical RB value ranges from 1 kOhm to 10 kOhm.

9.3.3 Temperature Sensors

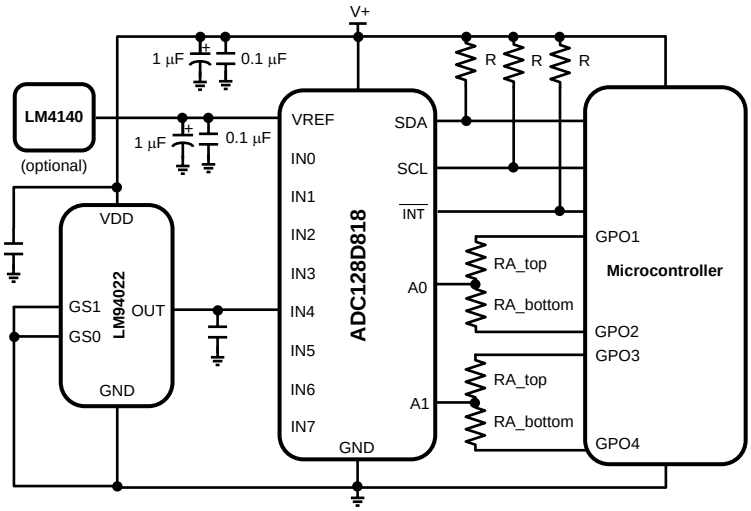


Figure 40. Temperature Sensor Applications

An external temperature sensor can be connected to any of ADC128D818's eight single-ended input for additional temperature sensing. One such temperature sensor can be TI's LM94022, a precision analog temperature sensor with selectable gains. The application diagram shows LM94022's gains (GS1 and GS0) both grounded indicating the lowest gain setting. Four possible gains can be set using these GS1 and GS0 pins.

According to the LM94022 data sheet (SNIS140), the voltage-to-temperature output plot can be determined using the method of linear approximation as follows:

$$V - V1 = (V2 - V1) / (T2 - T1) \times (T - T1)$$

where

- V is in mV
- T is in °C
- V1 and T1 are the coordinates of the lowest temperature
- and T2 and V2 are the coordinates of the highest temperature. (8)

For example, to determine the equation of a line over a temperature range of 20°C to 50°C, first find V1 and V2 relative to those temperatures, then use Equation 8 to find the transfer function.

$$V - 925\ mV = (760\ mV - 925\ mV) / (50°C - 20°C) \times (T - 20°C) \quad (9)$$

$$V = (-5.50\ mV/°C) \times T + 1035\ mV \quad (10)$$

For more information and explanation of this example, refer to the LM94022 (SNIS140) data sheet.

9.3.4 Bridge Sensors

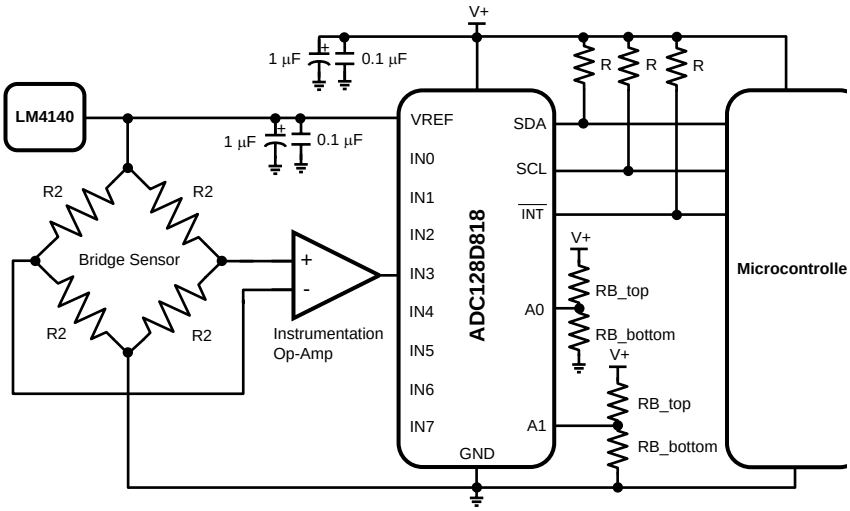


Figure 41. Bridge Sensor Application

ADC128D818 is perfect for transducer applications such as pressure sensors. These sensors measure pressure of gases or liquids and produce a pressure-equivalent voltage at their outputs. Figure 41 shows a typical connection of a pressure sensor, represented by the bridge sensor.

Most pressure sensor has a low sensitivity characteristic, which means its output is typically in the millivolts range. Because of that reason, an op-amp, such as an instrumentation amplifier, can be used for the gain stage.

The positive aspect of this configuration is its ratiometric connection. A ratiometric connection is when the ADC's VREF and GND are connected to the bridge sensor's voltage references. With a ratiometric configuration, external VREF accuracy can be ignored.

10 Power Supply Recommendations

The ADC128D818 operates with a supply voltage, V+, that has a range between 3 V to 5.5 V. Take care to bypass this pin with a parallel combination of 1-µF (electrolytic or tantalum) capacitor and 0.1-µF (ceramic) bypass capacitor.

The reference voltage (VREF) sets the analog input range. The ADC128D818 has two options for setting VREF. The first option is to use the internal VREF, which is equal to 2.56 V. The second option is to source VREF externally through pin 1 of ADC128D818. In this case, the external VREF will operate in the range of 1.25 V to V+. The default VREF selection is the internal VREF. If the external VREF is preferred, use the *Advanced Configuration Register — Address 0Bh* to change this setting.

VREF source must have a low output impedance and needs to be bypassed with a minimum capacitor value of 0.1 µF. A larger capacitor value of 1 µF placed in parallel with the 0.1 µF is preferred. VREF of the ADC128D818, like all ADC converters, does not reject noise or voltage variations. Keep this in mind if VREF is derived from the power supply. Any noise and/or ripple from the supply that is not rejected by the external reference circuitry will appear in the digital results. The use of a reference source is recommended. The LM4040 (SLOS746) and LM4050 (SNOS455) shunt reference families as well as the LM4120 (SNVS049) and LM4140 (SNVS053) series reference families are excellent choices for a reference source.

11 Layout

11.1 Layout Guidelines

Analog inputs will provide best accuracy when referred to the GND pin or a supply with low noise. A separate, low-impedance ground plane for analog ground, which provides a ground point for the voltage dividers and analog components, will provide best performance but is not mandatory. Analog components such as voltage dividers must be located physically as close as possible to the ADC128D818.

11.2 Layout Example

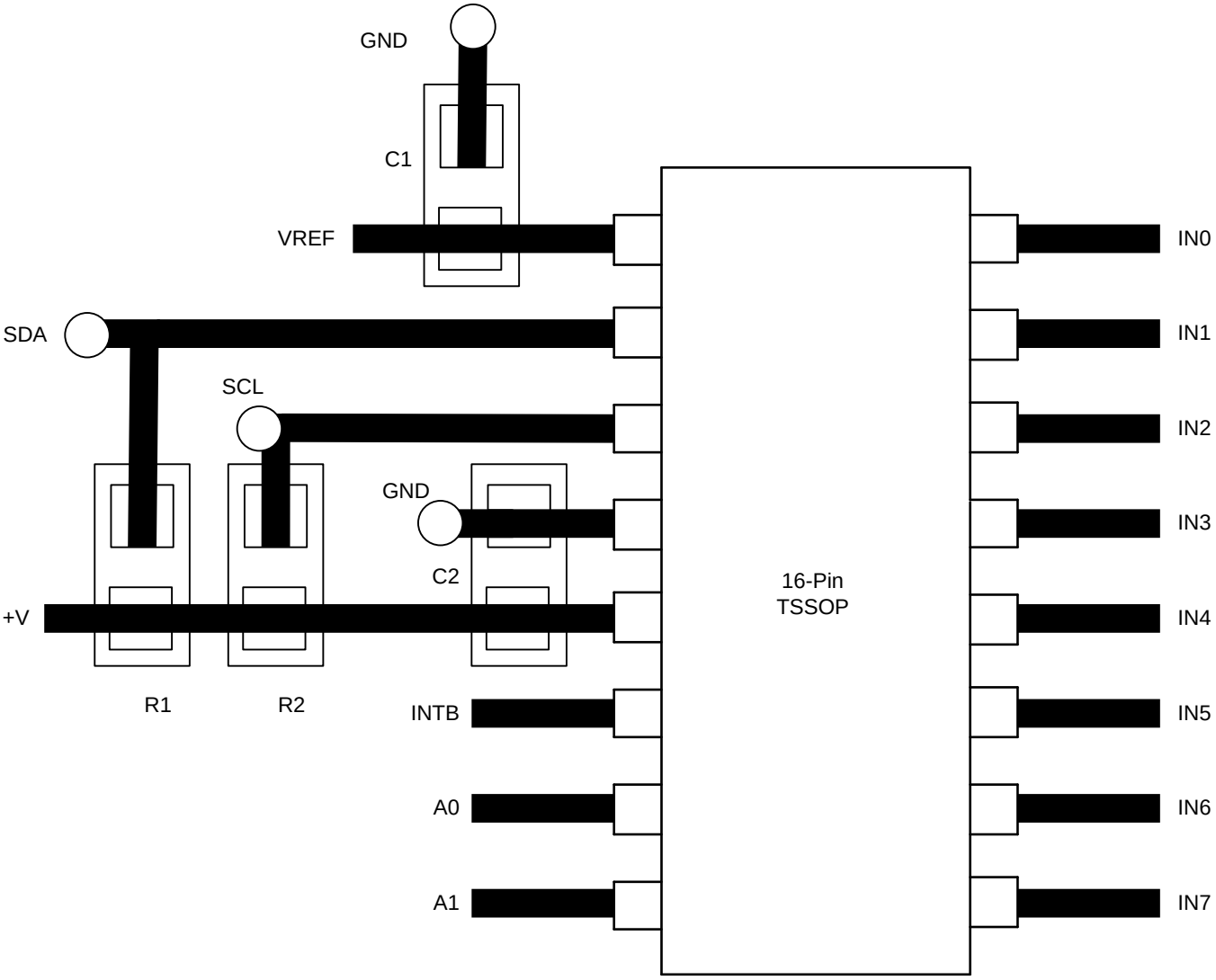


Figure 42. Sample Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *LM94022/22Q 1.5V, SC70, Multi-Gain Analog Temp Sensor w/Class-AB Output*, SNIS140
- *LM4040-EP Precision Micropower Shunt Voltage Reference*, SLOS746
- *LM4050-N/LM4050-N-Q1 Precision Micropower Shunt Voltage Reference*, SNOS455
- *LM4120 Precision Micropower Low Dropout Voltage Reference*, SNVS049
- *LM4140 High Precision Low Noise Low Dropout Voltage Reference*, SNVS053

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC128D818CIMT/NOPB	ACTIVE	TSSOP	PW	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	128D818 CIMT	Samples
ADC128D818CIMTX/NOPB	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	128D818 CIMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

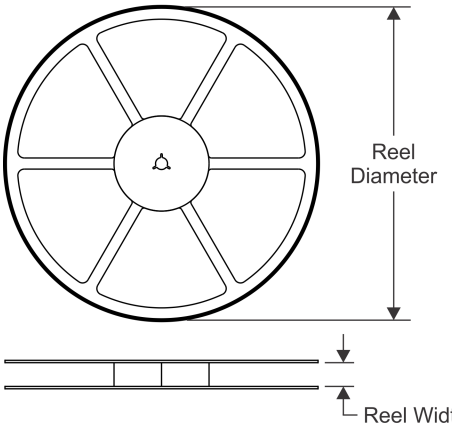
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

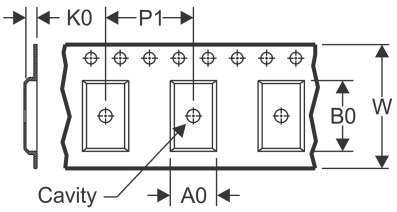
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

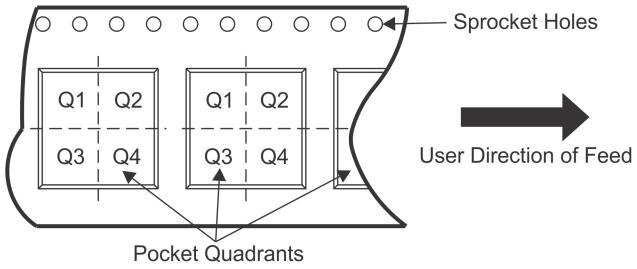


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



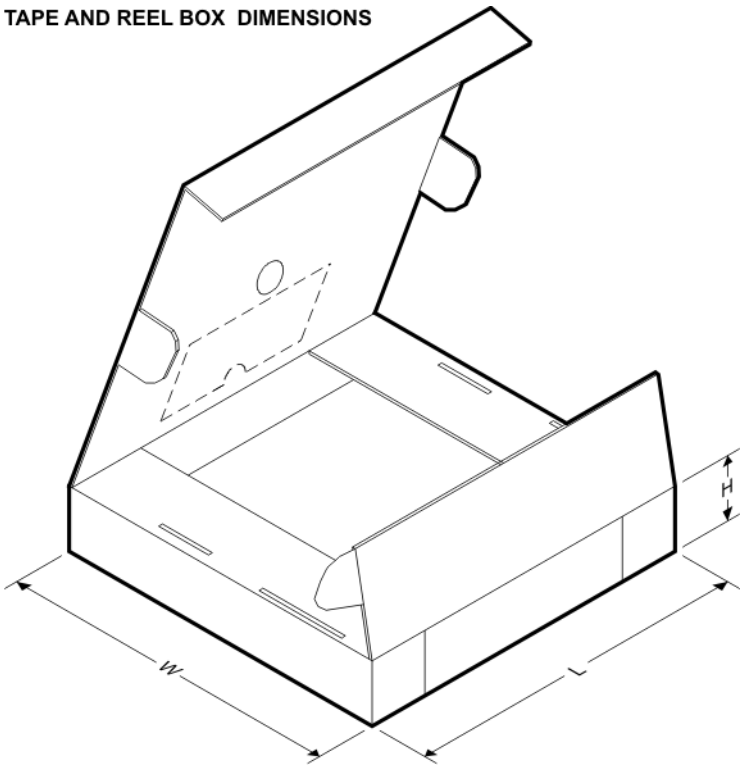
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC128D818CIMTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

8-Jul-2018

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

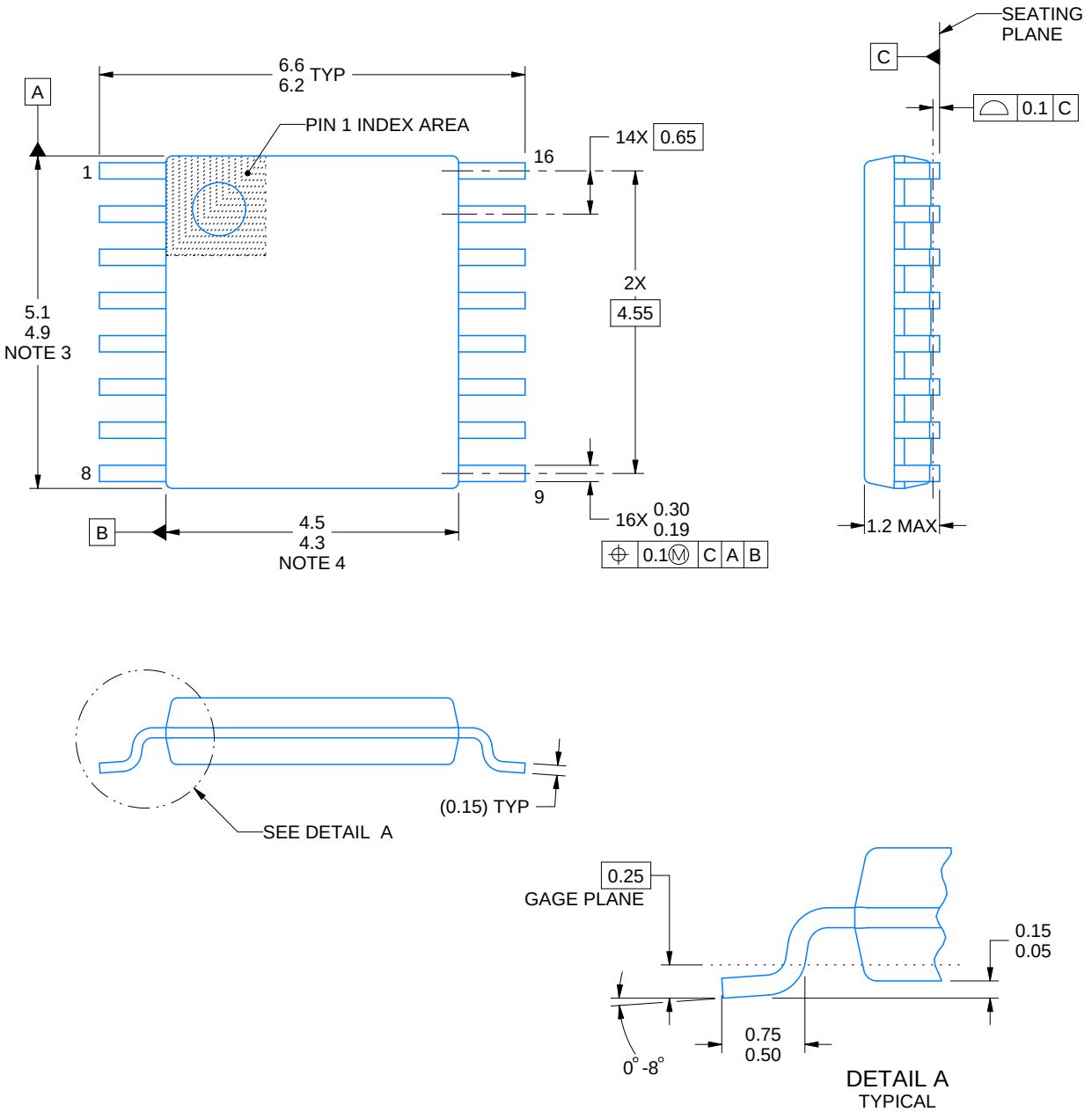
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC128D818CIMTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

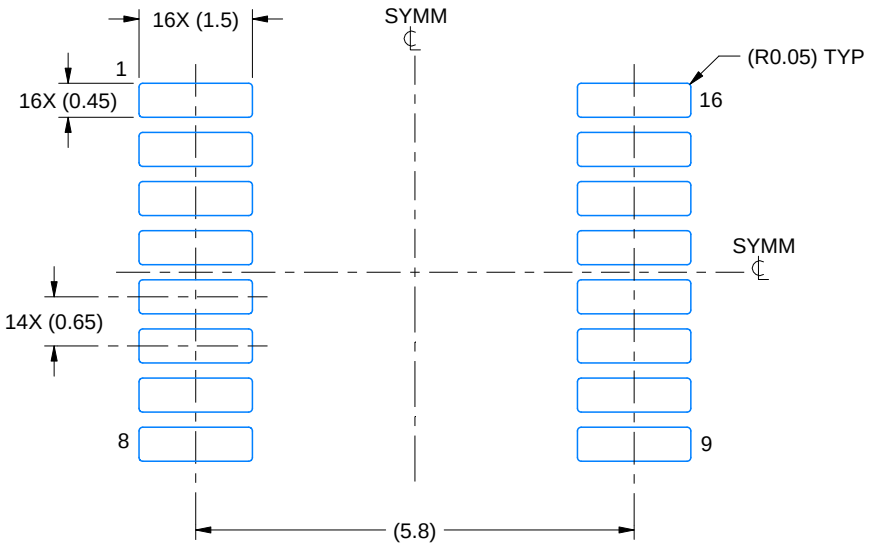
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

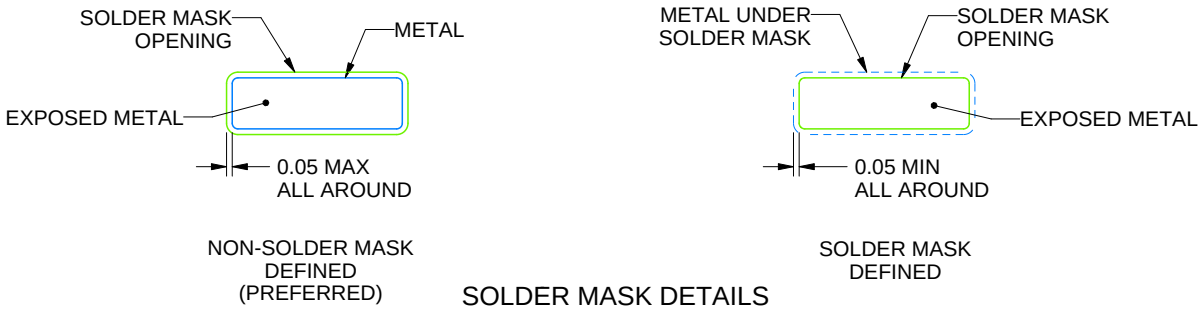


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

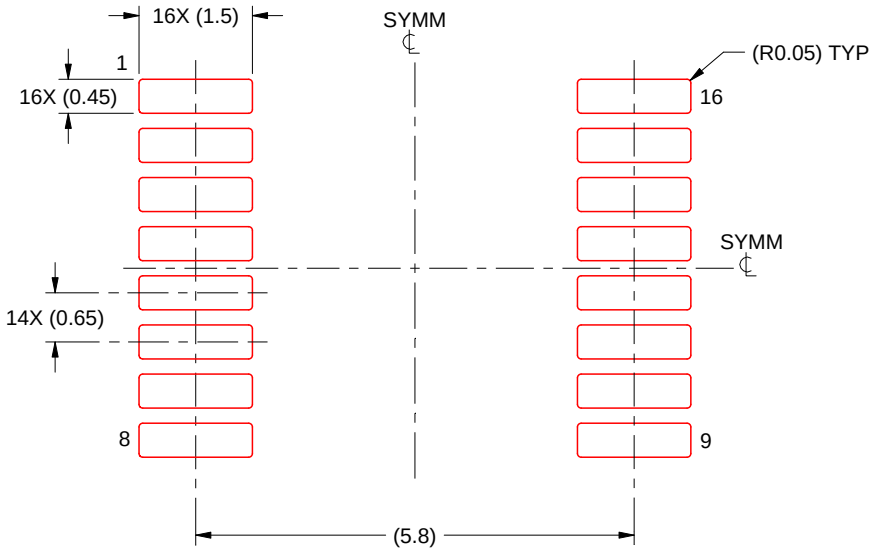
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.