4-Bit 100 Mb/s Configurable Dual-Supply Level Translator

NLSX5004, NLSXN5004

The NLSX5004 and NLSXN5004 are 4−bit configurable dual−supply autosensing bidirectional level translators that do not require direction control pins. The A− and B−ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both the V_{CCA} and the V_{CCB} supply rails are independently−configurable from 0.9 V to 3.6 V.

The NLSX5004 and NLSXN5004 have high dynamic output current capability, allowing the translators to drive high capacitive loads.

Enable input pins are available to reduce the power consumption. These pins may be used to disable both A− and B−ports by putting them in 3−state significantly reducing the supply current from both V_{CCA} and V_{CCB}. These pins are referenced to the V_{CCA} supply. The NLSX5004 has an active−High enable (EN) while the NLSXN5004 has active−Low enable ($\overline{EN}$).

Features

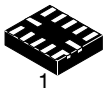
- Wide V_{CCA}, V_{CCB} Operating Range: 0.9 V to 3.6 V
- V_{CCA} and V_{CCB} are independent
  - V_{CCA} may be greater than, equal to, or less than V_{CCB}
- High 100 pF Capacitive Drive Capability
- High−Speed w/ 140 Mbps Guaranteed Date Rate for V_{CCA}, V_{CCB} > 1.8 V
- Low Bit−to−Bit skew
- Overvoltage Tolerant Enable and I/O Pins
- Non−preferential Power−Up Sequencing
- Partial Power−Off Protection
- Available packaging:
  UQFN−12, SOIC14, TSSOP14, QFN−14, Other packages
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and RoHS Compliant

Typical Applications

- Mobile Phones, Infotainment Systems, Other Devices

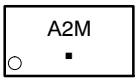
Important Information

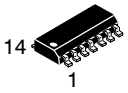
- ESD Protection for All Pins:
  HBM (Human Body Model) − 2000 V



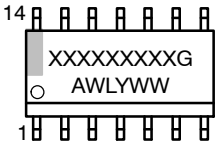
UQFN12
MU SUFFIX
CASE 523AE

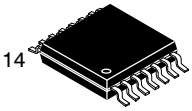
MARKING DIAGRAMS



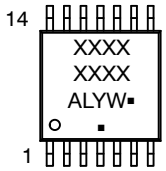


SOIC14
D SUFFIX
CASE 751A

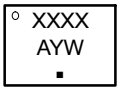




TSSOP14
DT SUFFIX
CASE 948G



QFN14
MN SUFFIX
CASE 485DE



QFN14
MN SUFFIX
CASE 485AL

XXXXX = Specific Device Code
M = Date Code
A = Assembly Location
L or WL = Wafer Lot
Y = Year
W or WW = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

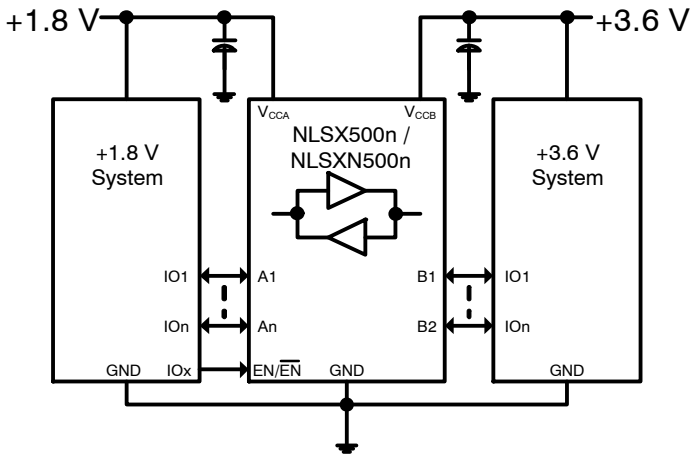


Figure 1. Typical Application Circuit

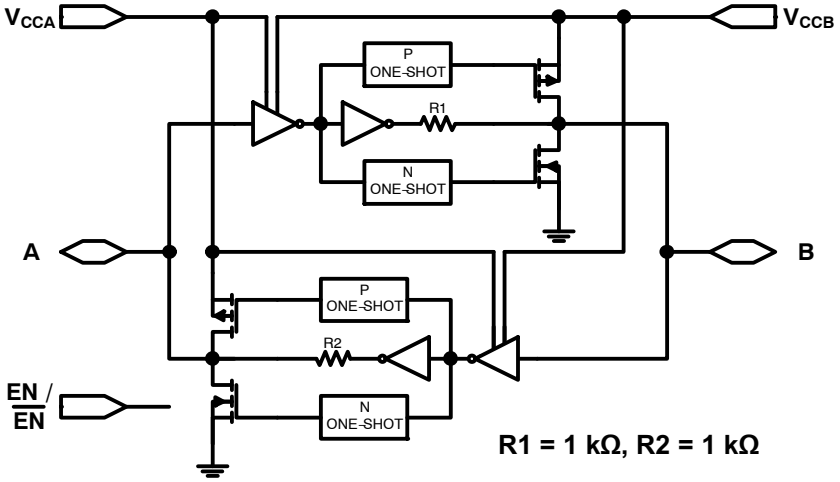


Figure 2. Functional Diagram (1 I/O Line)

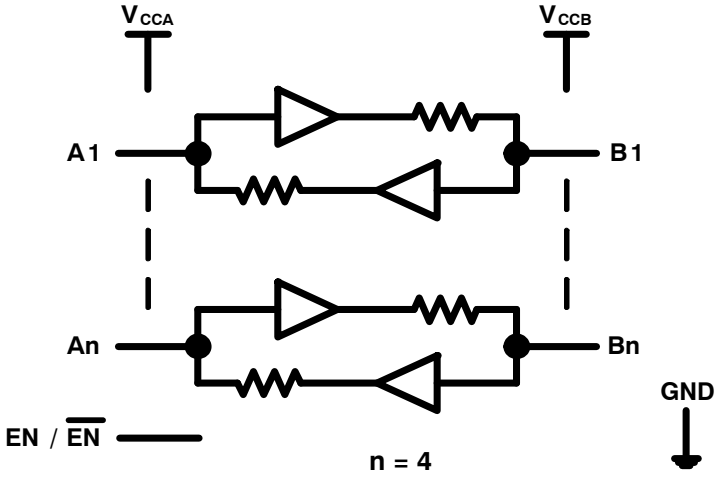


Figure 3. Logic Diagram

PIN ASSIGNMENTS

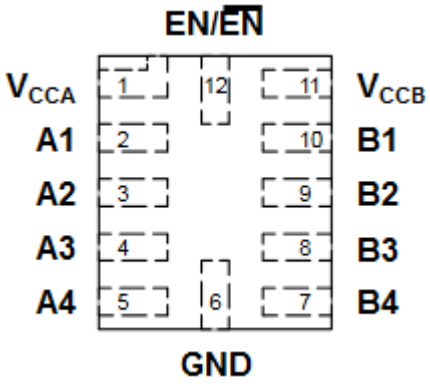


Figure 4. UQFN12

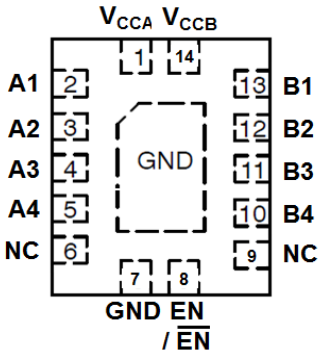


Figure 5. QFN14 (2.5 x 3.0)

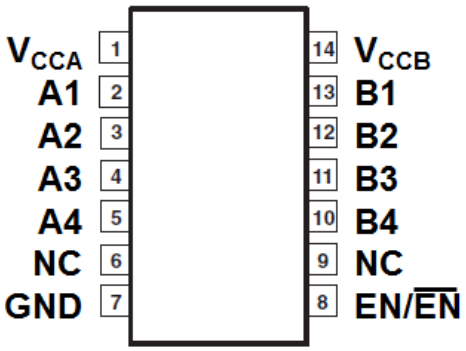


Figure 6. TSSOP / SOIC

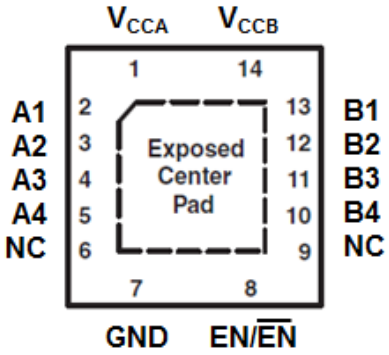


Figure 7. QFN14 (3.5 x 3.5)

PIN DESCRIPTIONS

Pins	Description
V_{CCA}	A−Port Supply Voltage
V_{CCB}	B−Port Supply Voltage
GND	Ground
EN	Active−High Enable (NLSX500n), Referenced to V_{CCA}
$\overline{EN}$	Active−Low Enable (NLSXN500n), Referenced to V_{CCA}
An	A−Port, Referenced to V_{CCA}
Bn	B−Port, Referenced to V_{CCB}

FUNCTION TABLE

NLSX500n	NLSXN500n	Operating
EN	**$\overline{EN}$**	**Mode**
L	H	An and Bn at Hi−Z
H	L	An and Bn Connected

Table 1. MAXIMUM RATINGS

Symbol	Parameter		Value	Condition	Unit
V_{CCA}	A−side DC Supply Voltage		−0.5 to +4.6		V
V_{CCB}	B−side DC Supply Voltage		−0.5 to +4.6		V
V_{IN}	Input/Output Voltage EN/$\overline{EN}$		−0.5 to +4.6		V
	Power Down Mode (V_{CCA} and/or V_{CCB} = 0 V)		−0.5 to +4.6		
	Tri−State Mode (EN = L or $\overline{EN}$ = H)		−0.5 to +4.6		
	Active Mode	A−Port	−0.5 to V_{CCA}+0.5		
		B−Port	−0.5 to V_{CCB}+0.5		
I_{IK}	DC Input Diode Current		−50	V_{IN} < GND	mA
I_{OK}	DC Output Diode Current		−50	V_O < GND	mA
I_{CCA}	DC Supply Current Through V_{CCA}		±100		mA
I_{CCB}	DC Supply Current Through V_{CCB}		±100		mA
I_{GND}	DC Ground Current Through Ground Pin		±100		mA
T_{STG}	Storage Temperature		−65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}	A−Port Supply Voltage		0.9	3.6	V
V_{CCB}	B−Port Supply Voltage		0.9	3.6	V
V_I	Input/Output Voltage EN/$\overline{EN}$		GND	3.6	V
	Power Down Mode (V_{CCA} and/or V_{CCB} = 0 V)		GND	3.6	
	Tri−State Mode (EN = L or $\overline{EN}$ = H)		GND	3.6	
	Active Mode	A−Port	GND	V_{CCA}	
		B−Port	GND	V_{CCB}	
T_A	Operating Temperature Range		−40	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate V_I from 30% to 70% of V_{CCA}/V_{CCB}		0	10	nS

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions (Note 1)	Pin/Port	V_{CCA} (V)	V_{CCB} (V)	–40°C to +85°C			–40°C to +125°C		Unit
						Min	Typ (Note 2)	Max	Min	Max	
V_{IH}	Input HIGH Voltage		A, EN/$\overline{EN}$	0.9–3.6	0.9–3.6	0.65 * V_{CCA}	–	–	0.65 * V_{CCA}	–	V
			B	0.9–3.6	0.9–3.6	0.65 * V_{CCB}	–	–	0.65 * V_{CCB}	–	V
V_{IL}	Input LOW Voltage		A, EN/$\overline{EN}$	0.9–3.6	0.9–3.6	–	–	0.35 * V_{CCA}	–	0.35 * V_{CCA}	V
			B	0.9–3.6	0.9–3.6	–	–	0.35 * V_{CCB}	–	0.35 * V_{CCB}	V
V_{OH}	Output HIGH Voltage	I_{OH} = –20 μA	A	0.9–3.6	0.9–3.6	0.9 * V_{CCA}	–	–	0.9 * V_{CCA}	–	V
			B	0.9–3.6	0.9–3.6	0.9 * V_{CCB}	–	–	0.9 * V_{CCB}	–	V
V_{OL}	Output LOW Voltage	I_{OL} = 20 μA	A	0.9–3.6	0.9–3.6	–	–	0.2	–	0.2	V
			B	0.9–3.6	0.9–3.6	–	–	0.2	–	0.2	V
I_{OZ}	Tristate Output Leakage	(EN = 0V or $\overline{EN}$ = V_{CCA});									μA
		(A = 0 V or V_{CCA})	A	0.9–3.6	0.9–3.6	–	0.01	±1.5	–	±4.5	
		(B = 0 V or V_{CCB})	B	0.9–3.6	0.9–3.6	–	0.01	±1	–	±3.5	
I_I	Input Pin Leakage	V_{IN} = 0 V to V_{CCA}	EN/$\overline{EN}$	0.9–3.6	0.9–3.6	–	0.01	±1	–	±3	μA
I_{CC}	Supply Current	(EN = V_{CCA} or $\overline{EN}$ = 0 V); I_O = 0 A, (A = 0 V, B = 0 V) or (A = V_{CCA}, B = V_{CCB})	V_{CCA}	0.9–3.6	0.9–3.6	–	0.4	2.0	–	6.0	μA
			V_{CCB}	0.9–3.6	0.9–3.6	–	0.3	1.5	–	6.0	
I_{CCZ}	Tristate Output Mode Supply Current	(EN = 0V or $\overline{EN}$ = V_{CCA}), (A = 0 V, B = 0 V) or (A = V_{CCA}, B = V_{CCB})	V_{CCA}	0.9–3.6	0.9–3.6	–	0.2	1.5	–	7.0	μA
			V_{CCB}	0.9–3.6	0.9–3.6	–	0.2	1.5	–	6.0	
I_{OFF}	Power Off Leakage	A = 0 to 3.6 V, B = 0 to 3.6 V	A, B	0	0	–	0.02	1.5	–	5.0	μA
				0.9–3.6	0	–	0.01	1.5	–	5.0	
				0	0.9–3.6	–	0.01	1.5	–	5.0	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Normal test conditions are V_I = 0 V, C_{LA} ≤ 15 pF and C_{LB} ≤ 15 pF, unless otherwise specified.
2. Typical values are for T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Table 4. TIMING CHARACTERISTICS

Symbol	Parameter	Test Conditions (Note 3)		V_{CCA} (V)	V_{CCB} (V)	–40°C to +85°C			–40°C to +125°C		Unit
						Min	Typ (Note 4)	Max	Min	Max	
t_{PD}	Propagation Delay	C_L = 15 pF	A to B	0.9–3.6	0.9–3.6	–	8.8	30	–	35	ns
				1.2	1.8	–	7.3	9	–	9	
				1.8	1.2	–	9.9	12	–	12	
				1.8	2.8	–	4.9	7	–	7	
				2.8	1.8	–	5.8	7.5	–	7.5	
				1.8	3.3	–	4.6	6	–	6	
				3.3	1.8	–	5.7	7	–	7	
				1.8–3.6	1.8–3.6	–	4.3	9.5	–	10	
			B to A	0.9–3.6	0.9–3.6	–	8.8	30	–	35	
				1.2	1.8	–	9.9	12	–	12	
				1.8	1.2	–	7.3	9	–	9	
				1.8	2.8	–	5.8	7.5	–	7.5	
				2.8	1.8	–	4.9	7	–	7	
				1.8	3.3	–	5.7	7	–	7	
				3.3	1.8	–	4.6	6	–	6	
				1.8–3.6	1.8–3.6	–	4.3	9.5	–	10	
		C_L = 30 pF	A to B	0.9–3.6	0.9–3.6	–	9.1	32	–	35	
				1.2	1.8	–	7.8	9.3	–	9.3	
				1.8	1.2	–	10.8	12.6	–	12.6	
				1.8	2.8	–	6.2	7.4	–	7.4	
				2.8	1.8	–	6.0	7.9	–	7.9	
				1.8	3.3	–	6.1	7.4	–	7.4	
				3.3	1.8	–	4.2	6.5	–	6.5	
				1.8–3.6	1.8–3.6	–	4.5	10	–	10.5	
			B to A	0.9–3.6	0.9–3.6	–	9.1	32	–	35	
				1.2	1.8	–	10.8	12.6	–	12.6	
				1.8	1.2	–	7.8	9.3	–	9.3	
				1.8	2.8	–	6.0	7.9	–	8.0	
				2.8	1.8	–	6.2	7.4	–	7.4	
				1.8	3.3	–	4.2	6.5	–	6.5	
				3.3	1.8	–	6.1	7.4	–	7.4	
				1.8–3.6	1.8–3.6	–	4.5	10	–	10.5	
			A to B	0.9–3.6	0.9–3.6	–	9.4	35	–	37	
				1.2	1.8	–	8.1	9.5	–	9.5	
				1.8	1.2	–	11.1	13.6	–	13.6	
				1.8	2.8	–	6.5	7.6	–	7.6	
				2.8	1.8	–	6.2	8.2	–	8.3	
				1.8	3.3	–	6.3	7.6	–	7.6	

3. Typical values are for T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
4. Guaranteed by design.

Table 4. TIMING CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions (Note 3)		V_{CCA} (V)	V_{CCB} (V)	–40°C to +85°C			–40°C to +125°C		Unit
						Min	Typ (Note 4)	Max	Min	Max	
		C_L = 50 pF		3.3	1.8	–	4.3	6.6	–	6.6	
				1.8–3.6	1.8–3.6	–	4.7	10.3	–	10.8	
			B to A	0.9–3.6	0.9–3.6	–	9.4	35	–	37	
				1.2	1.8	–	11.1	13.6	–	13.6	
				1.8	1.2	–	8.1	9.5	–	9.5	
				1.8	2.8	–	6.2	8.2	–	8.3	
				2.8	1.8	–	6.5	7.6	–	7.6	
				1.8	3.3	–	4.3	6.6	–	6.6	
				3.3	1.8	–	6.3	7.6	–	7.6	
				1.8–3.6	1.8–3.6	–	4.7	10.3	–	10.8	

3. Typical values are for T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
4. Guaranteed by design.

Table 4. TIMING CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions (Note 3)		V_{CCA} (V)	V_{CCB} (V)	–40°C to +85°C			–40°C to +125°C		Unit
						Min	Typ (Note 4)	Max	Min	Max	
t_{PD}	Propagation Delay	C_L = 100 pF	A to B	0.9–3.6	0.9–3.6	–	9.9	–	–	–	ns
				1.2	1.8	–	8.4	10	–	10	
				1.8	1.2	–	11.5	14	–	14	
				1.8	2.8	–	5.5	8.3	–	8.3	
				2.8	1.8	–	6.9	8.9	–	9.0	
				1.8	3.3	–	5.1	6.7	–	6.8	
				3.3	1.8	–	6.8	8.2	–	8.2	
				1.8–3.6	1.8–3.6	–	5.0	11	–	11.5	
			B to A	0.9–3.6	0.9–3.6	–	9.9	–	–	–	
				1.2	1.8	–	11.5	14	–	14	
				1.8	1.2	–	8.4	10	–	10	
				1.8	2.8	–	6.9	8.9	–	9.0	
				2.8	1.8	–	5.5	8.3	–	8.3	
				1.8	3.3	–	6.8	8.2	–	8.2	
				3.3	1.8	–	5.1	6.7	–	6.8	
				1.8–3.6	1.8–3.6	–	5.0	11	–	11.5	
t_R	Output Rise Time trial	C_L = 15 pF	A	0.9–1.2	0.9–3.6	–	2.5	4.5	–	4.5	ns
				1.2–1.8		–	2.0	3.0	–	3.0	
				1.8–2.8		–	0.6	2.0	–	2.0	
				2.8–3.6		–	0.5	2.5	–	2.5	
			B	0.9–3.6	0.9–1.2	–	2.5	4.5	–	4.5	
					1.2–1.8	–	2.0	3.0	–	3.0	
					1.8–2.8	–	0.6	2.0	–	2.0	
					2.8–3.6	–	0.5	2.5	–	2.5	
t_F	Output Fall Time trial	C_L = 15 pF	A	0.9–1.2	0.9–3.6	–	2.5	6.0	–	6.0	ns
				1.2–1.8		–	1.8	3.0	–	3.0	
				1.8–2.8		–	0.6	2.0	–	2.0	
				2.8–3.6		–	0.5	2.5	–	2.5	
			B	0.9–3.6	0.9–1.2	–	2.5	6.0	–	6.0	
					1.2–1.8	–	1.8	3.0	–	3.0	
					1.8–2.8	–	0.6	2.0	–	2.0	
					2.8–3.6	–	0.5	2.5	–	2.5	
t_{SK}	Channel–to–Channel Skew			0.9–3.6	0.9–3.6	–	–	0.15	–	0.15	ns

3. Typical values are for T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
4. Guaranteed by design.

Table 4. TIMING CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions (Note 3)		V_{CCA} (V)	V_{CCB} (V)	–40°C to +85°C			–40°C to +125°C		Unit
						Min	Typ (Note 4)	Max	Min	Max	
MDR	Maximum Data Rate	C_L = 15 pF		0.9–3.6	0.9–3.6	50	–	–	50	–	Mbps
				1.8–3.6	1.8–3.6	140	–	–	140	–	
		C_L = 30 pF		0.9–3.6	0.9–3.6	40	–	–	40	–	
				1.8–3.6	1.8–3.6	120	–	–	120	–	
		C_L = 50 pF		0.9–3.6	0.9–3.6	30	–	–	30	–	
				1.8–3.6	1.8–3.6	100	–	–	100	–	
		C_L = 100 pF		0.9–3.6	0.9–3.6	20	–	–	20	–	
				1.8–3.6	1.8–3.6	60	–	–	60	–	
I_{I_PEAK}	Input Driver Peak Current	$\overline{EN}$ = V_{CCA} or $\overline{EN}$ = 0 V									mA
		A = 1 MHz Sq Wave, Amplitude = V_{CCA}	A	0.9–3.6	0.9–3.6	–	–	5.0	–	5.0	
		B = 1 MHz Sq Wave, Amplitude = V_{CCB}	B	0.9–3.6	0.9–3.6	–	–	5.0	–	5.0	
Z_O (Note 4)	1−Shot Output Impedance		A	0.9	0.9–3.6	–	37	–	–	–	Ω
				1.8		–	20	–	–	–	
				3.6		–	10	–	–	–	
			B	0.9–3.6	0.9	–	37	–	–	–	
					1.8	–	20	–	–	–	
					3.6	–	10	–	–	–	
t_{EN}	Output Enable Time	C_L = 15 pF; B = V_{CCB}	EN/$\overline{EN}$ to A	0.9–3.6	0.9–3.6	–	116.3	200	–	200	ns
				1.2–1.8	1.2–1.8	–	64.5	180	–	180	
				1.8–2.8	1.8–2.8	–	49.6	150	–	150	
				1.8–3.6	1.8–3.6	–	42.5	100	–	100	
		C_L = 15 pF; B = 0 V		0.9–3.6	0.9–3.6	–	113.4	300	–	300	
				1.2–1.8	1.2–1.8	–	100	250	–	250	
				1.8–2.8	1.8–2.8	–	94.3	200	–	200	
				1.8–3.6	1.8–3.6	–	90.9	170	–	170	
		C_L = 15 pF; A = V_{CCA}	EN/$\overline{EN}$ to B	0.9–3.6	0.9–3.6	–	116.3	200	–	200	
				1.2–1.8	1.2–1.8	–	64.5	180	–	180	
				1.8–2.8	1.8–2.8	–	49.6	150	–	150	
				1.8–3.6	1.8–3.6	–	42.5	100	–	100	
		C_L = 15 pF; A = 0 V		0.9–3.6	0.9–3.6	–	113.4	300	–	300	ns
				1.2–1.8	1.2–1.8	–	100	250	–	250	
				1.8–2.8	1.8–2.8	–	94.3	200	–	200	
				1.8–3.6	1.8–3.6	–	90.9	170	–	170	

3. Typical values are for T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
4. Guaranteed by design.

Table 4. TIMING CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions (Note 3)		V_{CCA} (V)	V_{CCB} (V)	–40°C to +85°C			–40°C to +125°C		Unit
						Min	Typ (Note 4)	Max	Min	Max	
t_{DIS}	Output Disable Time	C_L = 15 pF; B = V_{CCB}	EN/$\overline{EN}$ to A	0.9–3.6	0.9–3.6	–	255	600	–	600	ns
				1.2–1.8	1.2–1.8	–	180	350	–	350	
				1.8–2.8	1.8–2.8	–	166.7	350	–	350	
				1.8–3.6	1.8–3.6	–	155.6	300	–	300	
		C_L = 15 pF; B = 0 V		0.9–3.6	0.9–3.6	–	156.7	400	–	400	
				1.2–1.8	1.2–1.8	–	140	300	–	300	
				1.8–2.8	1.8–2.8	–	130.2	300	–	300	
				1.8–3.6	1.8–3.6	–	124.6	250	–	250	
		C_L = 15 pF; A = V_{CCA}	EN/$\overline{EN}$ to B	0.9–3.6	0.9–3.6	–	255	600	–	600	
				1.2–1.8	1.2–1.8	–	180	350	–	350	
				1.8–2.8	1.8–2.8	–	166.7	350	–	350	
				1.8–3.6	1.8–3.6	–	155.6	300	–	300	
		C_L = 15 pF; A = 0 V		0.9–3.6	0.9–3.6	–	156.7	400	–	400	
				1.2–1.8	1.2–1.8	–	140	300	–	300	
				1.8–2.8	1.8–2.8	–	130.2	300	–	300	
				1.8–3.6	1.8–3.6	–	124.6	250	–	250	

3. Typical values are for T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
4. Guaranteed by design.

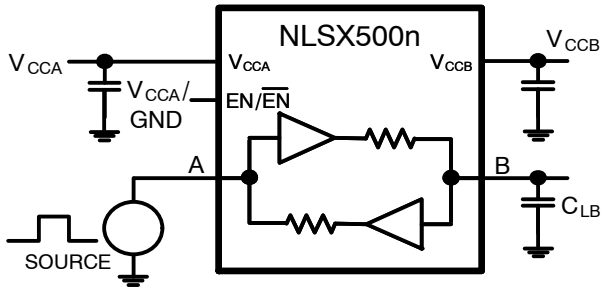


Figure 8. Driving A−Port Test Circuit (t_{PD})

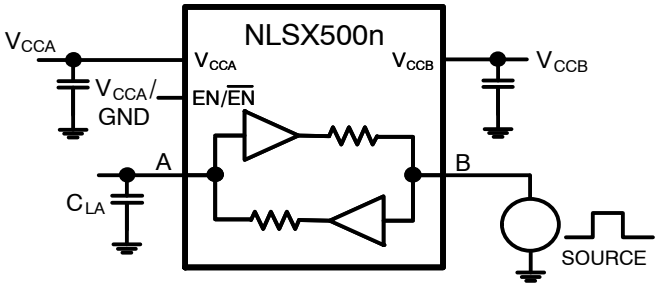


Figure 9. Driving B−Port Test Circuit (t_{PD})

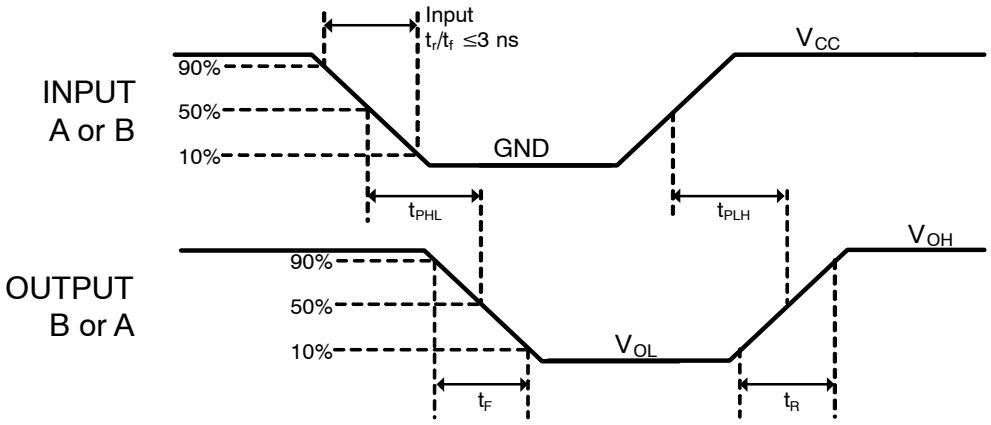


Figure 10. t_{PD} (t_{PLH}/t_{PHL}) Propagation Delay Measurements

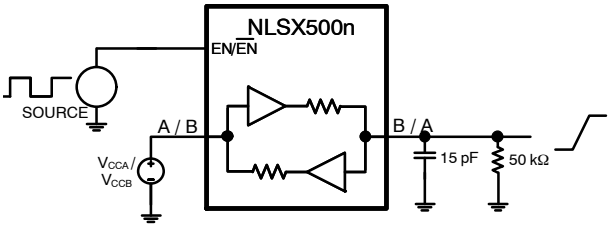


Figure 11. Enable/Disable Test Circuit (t_{PZH}/t_{PHZ})

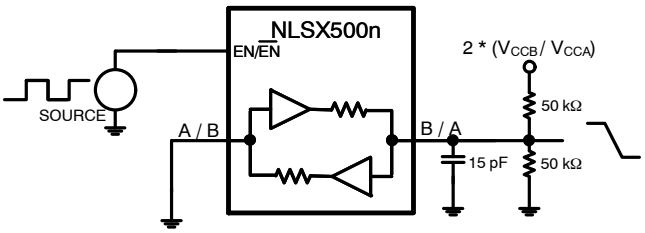


Figure 12. Enable/Disable Test Circuit (t_{PZL}/t_{PLZ})

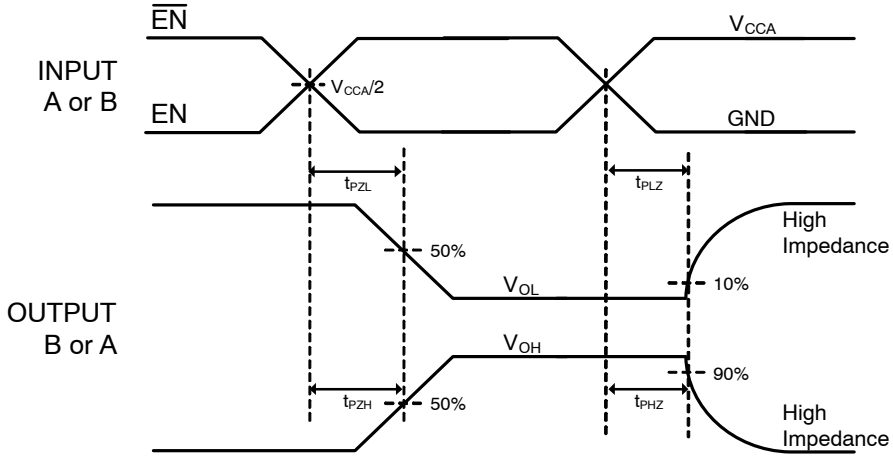


Figure 13. t_{EN}/t_{DIS} (t_{PZL}/t_{PLZ}/t_{PZH}/t_{PHZ}) Propagation Delay Measurements

IMPORTANT APPLICATIONS INFORMATION

Level Translator Architecture

The NLSX5004 and the NLSXN5004 auto−sense translators provide bi−directional logic voltage level shifting to transfer data in multiple supply voltage systems. These level translators have two supply voltages, V_{CCA} and V_{CCB}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the A to the B ports, input signals referenced to the V_{CCA} supply are translated to output signals with a logic level matched to V_{CCB}. In a similar manner, the B to A translation shifts input signals with a logic level compatible to V_{CCB} to an output signal matched to V_{CCA}.

The NLSX5004 and the NLSXN5004 translators consist of bi−directional channels that independently determine the direction of the data flow without requiring a directional pin. One−shot circuits are used to detect the rising or falling input signals. In addition, the one−shots decrease the rise and fall times of the output signal for high−to−low and low−to−high transitions.

Input Driver Requirements

The NLSX5004 and NLSXN5004 support high data rates, but these translators have relatively modest DC output current drive. The high data rate of the bi−directional I/O circuit is used to quickly transform from an input to an output driver and vice versa. Each I/O port has a modest DC current output so that the internal output driver can be over−driven when data is sent in the opposite direction. For proper operation, the input driver to the auto−sense translator should be capable of driving 5.0 mA of peak output current. The bi−directional configuration of the translator results in both input stages being active for a very short time period. Although the peak current required from the input signal circuit is relatively large, the average current is small and consistent with a standard CMOS input stage.

Enable Input (EN/$\overline{\text{EN}}$)

The NLSX5004 and NLSXN5004 translators have enable pins that provide tri−state operation at the I/O ports.

Driving the NLSX5004 Enable pin (EN) to a low logic level minimizes the power consumption of the device and drives the A− and B−ports to high impedance states. Normal translation operation occurs when the EN pin is equal to a logic high signal.

Driving NLSXN5004 Enable pin ($\overline{\text{EN}}$) to a high logic level minimizes the power consumption of the device and drives the A− and B−ports to high impedance states. Normal translation operation occurs when the $\overline{\text{EN}}$ pin is equal to a logic low signal.

Both EN and $\overline{\text{EN}}$ pins are referenced to the V_{CCA} supply and are Over−Voltage Tolerant (OVT).

Uni−Directional versus Bi−Directional Translation

The NLSX5004 and NLSXN5004 translators can function as non−inverting uni−directional translators. One advantage of using these translators as uni−directional devices is that each I/O−port can be configured as either an input or an output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni−directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

Power Supply Guidelines

The values of the V_{CCA} and V_{CCB} supplies can be set to anywhere between 0.9 and 3.6 V. Design flexibility is maximized because V_{CCA} may be either greater than, equal to or less than the V_{CCB} supply.

The sequencing of the power supplies will not damage the device during power−up operation. In addition, the A− and B−ports are in high impedance states if either supply voltage is equal to 0 V. For optimal performance, 0.01 to 0.1 μF decoupling capacitors should be used on the V_{CCA} and V_{CCB} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

DEVICE ORDERING INFORMATION

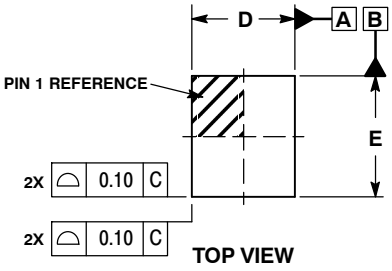
Device Order Number	Package Type	Tape & Reel Size†
NLSX5004MUTAG	UQFN−12	3000 / Tape & Reel
NLVSX5004MUTAG*	UQFN−12	3000 / Tape & Reel
NLSX5004DR2G (In Development)	SOIC14	2500 / Tape & Reel
NLVSX5004DR2G* (In Development)	SOIC14	2500 / Tape & Reel
NLSX5004DTR2G (In Development)	TSSOP14	2500 / Tape & Reel
NLVSX5004DTR2G* (In Development)	TSSOP14	2500 / Tape & Reel
NLSX5004MN1TXG (In Development)	QFN14, 3.5 x 3.5 x 0.5P	3000 / Tape & Reel
NLVSX5004MN1TXG*	QFN14, 3.5 x 3.5 x 0.5P	3000 / Tape & Reel
NLSX5004MN1TWG (In Development)	QFN14, 2.5 x 3.0 x 0.5P	3000 / Tape & Reel
NLVSX5004MN1TWG* (In Development)	QFN14, 2.5 x 3.0 x 0.5P	3000 / Tape & Reel
NLSXN5004MU2TAG (In Development)	UQFN−12	3000 / Tape & Reel
NLVSXN5004MU2TAG* (In Development)	UQFN−12	3000 / Tape & Reel
NLSXN5004DR2G (In Development)	SOIC14	2500 / Tape & Reel
NLVSXN5004DR2G* (In Development)	SOIC14	2500 / Tape & Reel
NLSXN5004DTR2G (In Development)	TSSOP14	2500 / Tape & Reel
NLVSXN5004DTR2G* (In Development)	TSSOP14	2500 / Tape & Reel
NLSXN5004MN1TXG (In Development)	QFN14, 3.5 x 3.5 x 0.5P	3000 / Tape & Reel
NLVSXN5004MN1TXG* (In Development)	QFN14, 3.5 x 3.5 x 0.5P	3000 / Tape & Reel
NLSXN5004MN1TWG (In Development)	QFN14, 2.5 x 3.0 x 0.5P	3000 / Tape & Reel
NLVSXN5004MN1TWG* (In Development)	QFN14, 2.5 x 3.0 x 0.5P	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

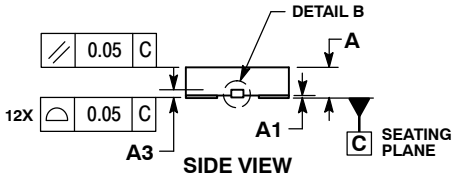
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

PACKAGE DIMENSIONS

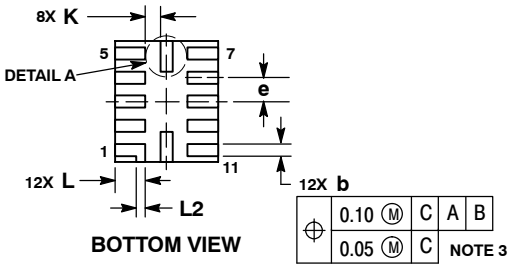
UQFN12 1.7x2.0, 0.4P
CASE 523AE
ISSUE A



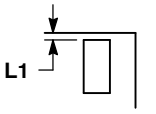
TOP VIEW



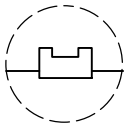
SIDE VIEW



BOTTOM VIEW



DETAIL A
NOTE 5

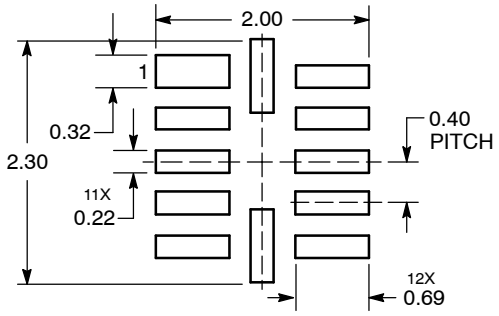


DETAIL B
OPTIONAL CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	----
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

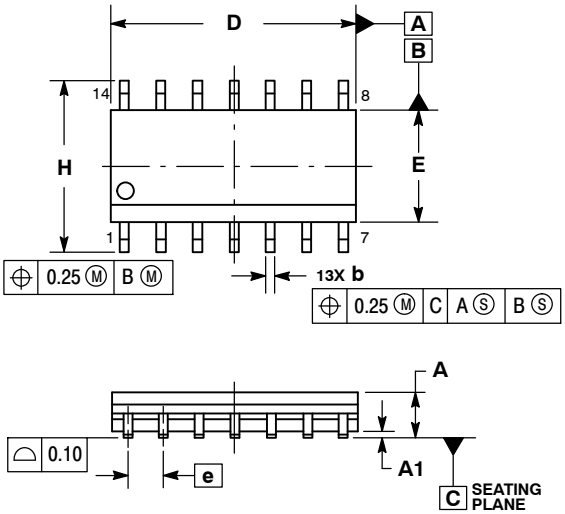
MOUNTING FOOTPRINT
SOLDERMASK DEFINED

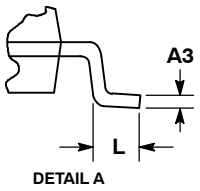


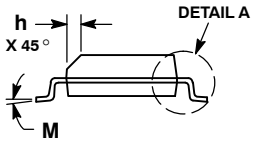
DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE L



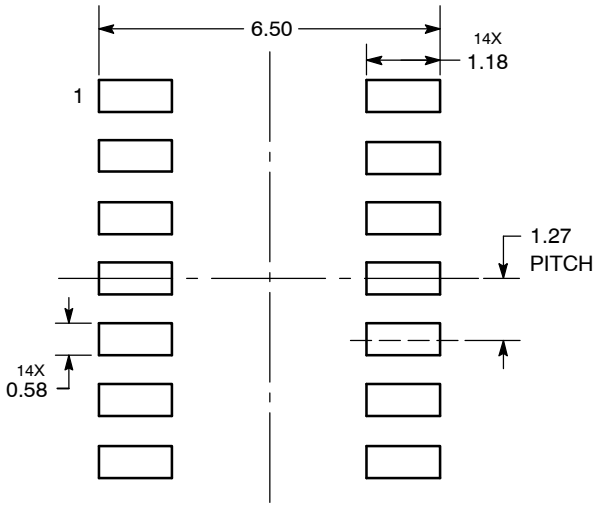




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*

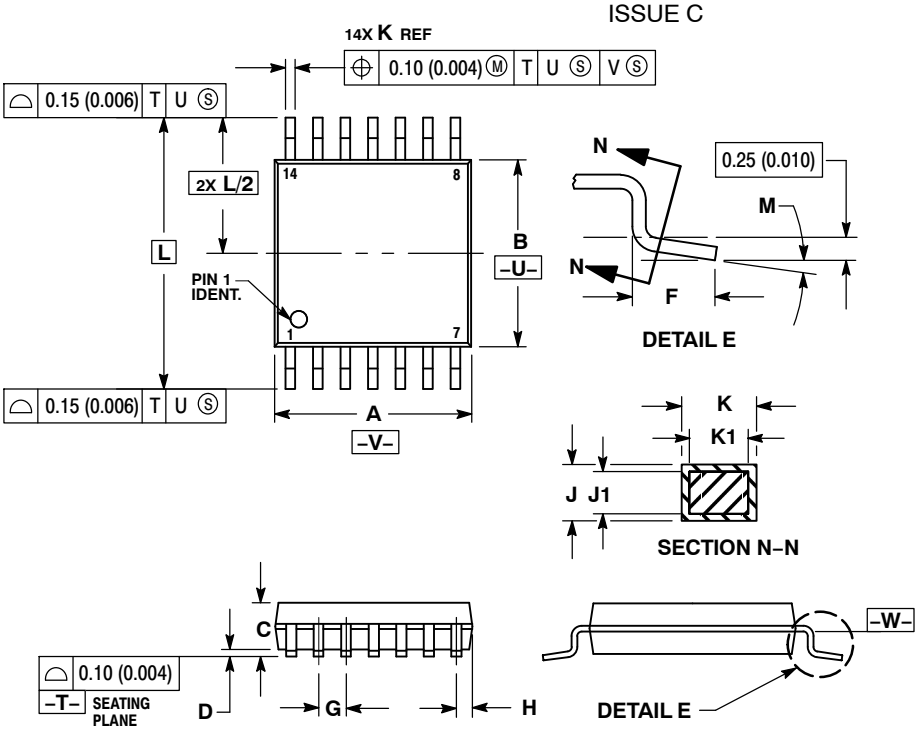


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

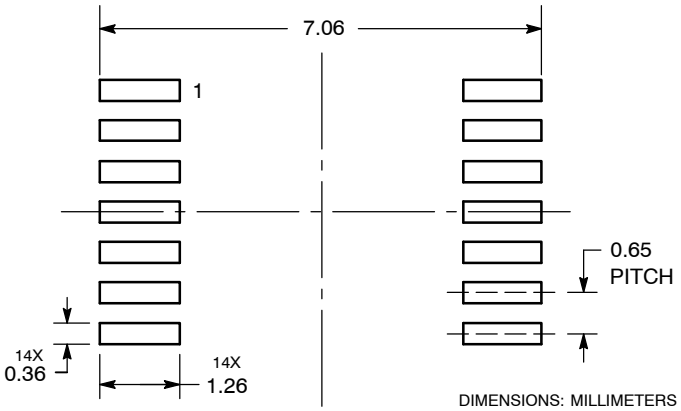
TSSOP−14 WB
CASE 948G
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

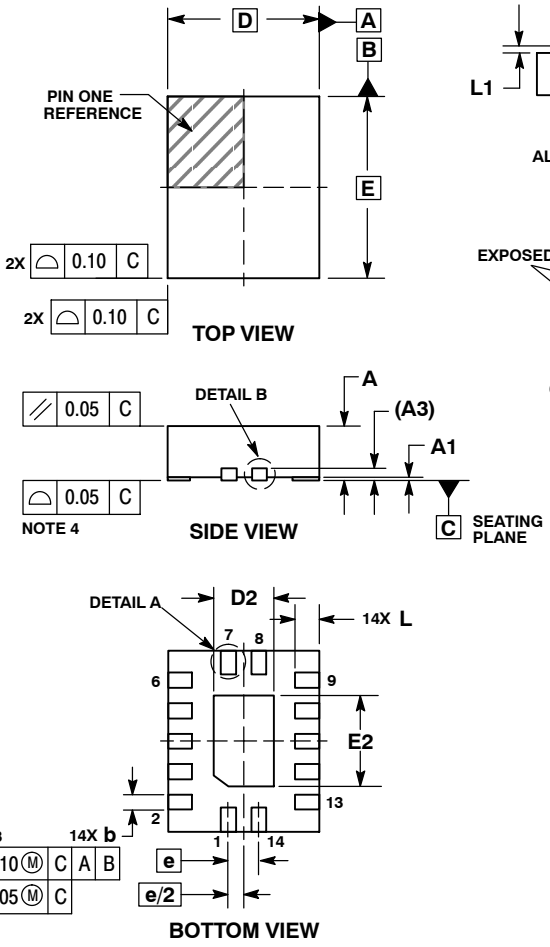
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

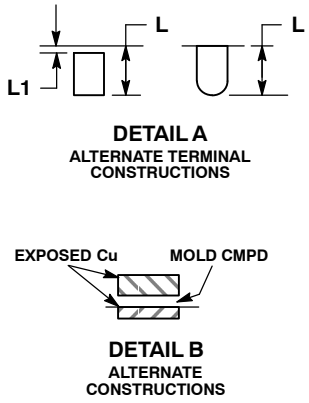
SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

QFN14, 2.5x3.0, 0.5P
CASE 485DE
ISSUE O

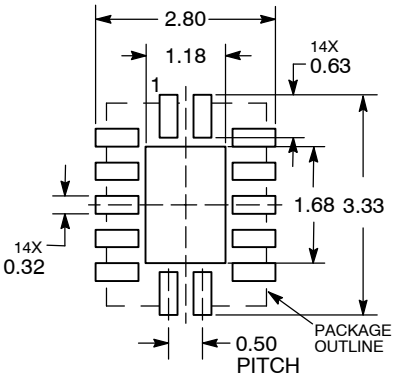




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.90	1.10
E	3.00 BSC	
E2	1.40	1.60
e	0.50 BSC	
L	0.30	0.50
L1	---	0.05

RECOMMENDED SOLDERING FOOTPRINT*

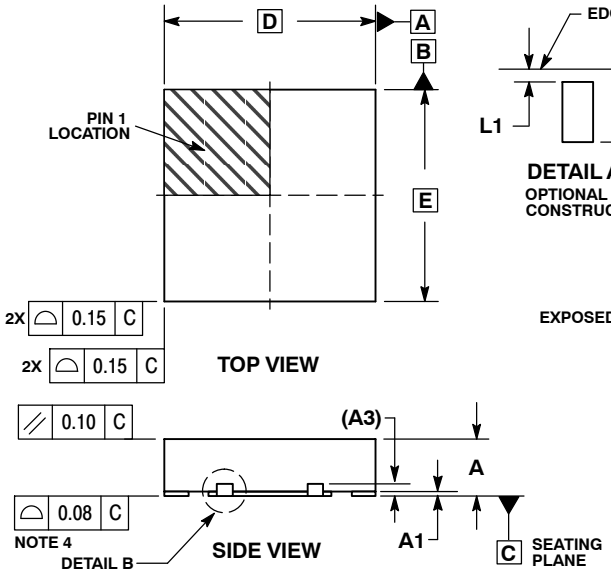


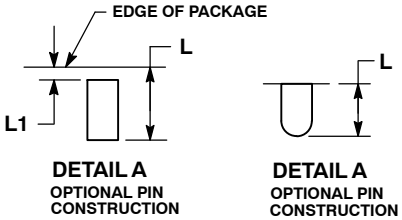
DIMENSIONS: MILLIMETERS

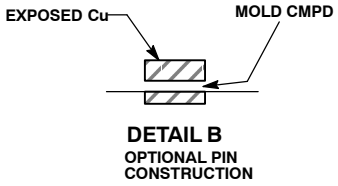
*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

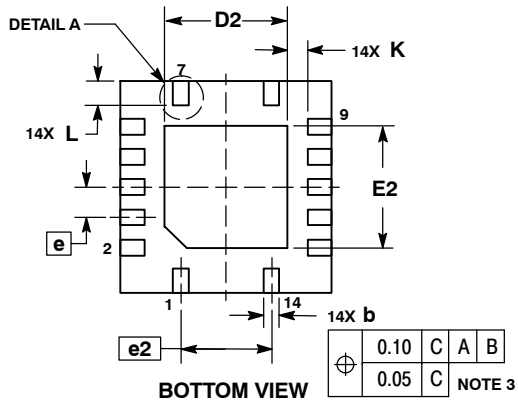
PACKAGE DIMENSIONS

QFN14 3.5x3.5, 0.5P
CASE 485AL
ISSUE O





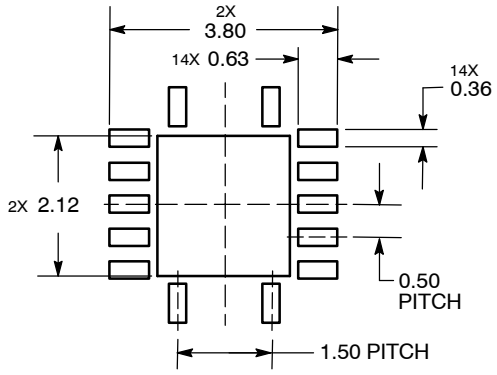




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.50 BSC	
D2	1.90	2.15
E	3.50 BSC	
E2	1.90	2.15
e	0.50 BSC	
e2	1.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.03

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.