TCA9509 Level-Translating I²C and SMBUS Bus Repeater

1 Features

- Two-channel bidirectional buffer
- I²C bus and SMBus compatible
- Operating supply voltage range of 2.7V to 5.5V on B side
- Operating voltage range of 0.9V to 5.5V on A side
- Voltage-level translation from 0.9V to 5.5V and 2.7V to 5.5V
- Active-high repeater-enable input
- Requires no external pullup resistors on lower-voltage port-A
- Open-drain I²C I/O
- 5.5-V Tolerant I²C and enable input support mixed-mode signal operation
- Lockup-free operation
- Accommodates standard mode and fast mode I²C devices and multiple controllers
- Supports arbitration and clock stretching across Repeater
- Powered-off high-impedance I²C bus pins
- Supports 400-kHz fast I²C bus operating speeds
- Available in
  - 1.6mm × 1.6mm, 0.4mm height, 0.5mm pitch QFN package
  - 3mm × 3mm Industry standard MSOP package
- Latch-up performance exceeds 100mA Per JESD 78, class II
- ESD protection exceeds JESD 22
  - 2000V Human-body model (A114-A)
  - 1000V Charged-device model (C101)

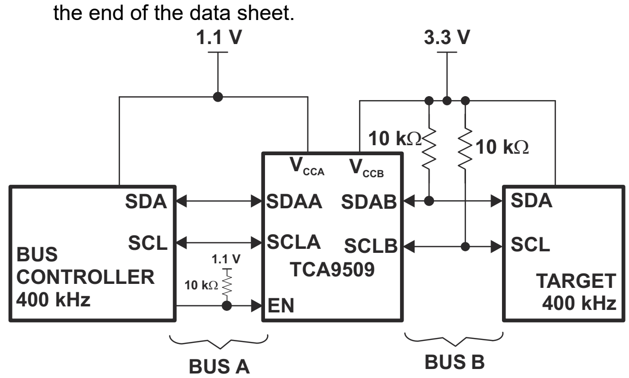
2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Industrial Equipment
- Products with many I²C targets and or long PCB Traces

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TCA9509	VSSOP (8)	3.00mm × 3.00mm
	X2QFN (8)	1.60mm × 1.60mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

3 Description

This TCA9509 integrated circuit is an I^2C bus/SMBus Repeater for use in I^2C/SMBus systems. It can also provide bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9V) and higher voltages (2.7V to 5.5V) in mixed-mode applications. This device enables I^2C and similar bus systems to be extended, without degradation of performance even during level shifting.

The TCA9509 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I^2C bus, thus allowing 400pF bus capacitance on the B-side. This device can also be used to isolate two halves of a bus for voltage and capacitance.

The TCA9509 has two types of drivers – A-side drivers and B-side drivers. All inputs and B-side I/Os are overvoltage tolerant to 5.5V. The A-side I/Os are overvoltage tolerant to 5.5V when the device is unpowered (VCCB and/or VCCA = 0 V).

The bus port B drivers are compliant with SMBus I/O levels, while the A-side uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. The A-side uses a 1 mA current source for pull-up and a 200Ω pull-down driver. This results in a LOW on the A-side accommodating smaller voltage swings. The output pull-down on the A-side internal buffer LOW is set for approximately 0.2V, while the input threshold of the internal buffer is set about 50mV lower than that of the output voltage LOW. When the A-side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the B-side drives a hard LOW and the input level is set at 0.3 of SMBus or I^2C-bus voltage level which enables B side to connect to any other I^2C-bus devices or buffer.

The TCA9509 drivers are not enabled unless V_{CCA} is above 0.8V and V_{CCB} is above 2.5V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

Table of Contents

4 Pin Configuration and Functions

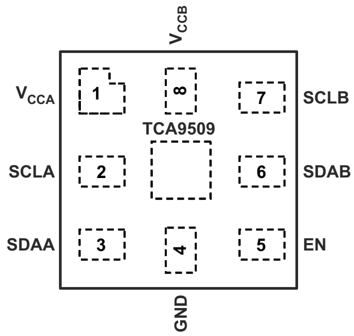


Figure 4-1. RVH Package, 8-Pin X2QFN, Top View

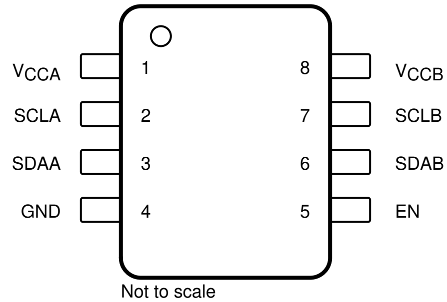


Figure 4-2. DGK Package, 8-Pin VSSOP, Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{CCA}	1	Supply	A-side supply voltage (0.9 V to 5.5 V)
SCLA	2	I/O	Serial clock bus, A side.
SDAA	3	I/O	Serial data bus, A side.
GND	4	Supply	Supply ground
EN	5	Input	Active-high repeater enable input
SDAB	6	I/O	Serial data bus, B side. Connect to V_{CCB} through a pull-up resistor.
SCLB	7	I/O	Serial clock bus, B side. Connect to V_{CCB} through a pull-up resistor.
V_{CCB}	8	Supply	B-side and device supply voltage (2.7 V to 5.5 V)
Thermal Attach Pad	-	-	Thermal Attach Pad is not electrically connected and it is recommended to be attached to GND for best thermal performance. This is for the RVH package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		–0.5	6	V
V_{CCA}	Supply voltage		–0.5	6	V
V_I	Enable input voltage[2]		–0.5	6	V
$V_{I/O}$	I^2C bus voltage[2]		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
P_d	Max power dissipation			100	mW
T_J	Junction temperature			125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus		0.9[1]	5.5	V
V_{CCB}	Supply voltage, B-side bus		2.7	5.5	V
V_{IH}	High-level input voltage	SDAA, SCLA	$0.7 \times V_{CCA}$	V_{CCA}	V
		SDAB, SCLB	$0.7 \times V_{CCB}$	5.5	
		EN	$0.7 \times V_{CCA}$	5.5	
V_{IL}	Low-level input voltage	SDAA, SCLA	–0.5	0.3	V
		SDAB, SCLB	–0.5	$0.3 \times V_{CCB}$	
		EN	–0.5	$0.3 \times V_{CCA}$	
I_{OL}	Low-level output current	SDAA, SCLA		10	µA
		SDAB, SCLB		6	mA
T_A	Operating free-air temperature		–40	85	°C

(1) Low-level supply voltage

5.4 Thermal Information

THERMAL METRIC[1]		TCA9509 RVH (X2QFN) 8 PINS	TCA9509 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	160.3	222.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.4	109.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	115.9	144.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	34.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	116.2	142.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	80.5	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

5.5 Electrical Characteristics

V_{CCB} = 2.7 V to 5.5 V, V_{CCA} = 0.9 V to (V_{CCB}-1), T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA	–1.5		–0.5	V
V_{OL}	Low-level output voltage	SDAA, SCLA	I_{OL} = 10 µA, V_{ILA} = V_{ILB} = 0 V, V_{CCA} = 0.9 to 1.2 V		0.18	0.25	V
		SDAA, SCLA	I_{OL} = 20 µA, V_{ILA} = V_{ILB} = 0 V, 1.2V < V_{CCA} ≤ (V_{CCB} – 1 V)		0.2	0.3	
$V_{OL} – V_{ILc}$	Low-level input voltage below low-level output voltage	SDAA, SCLA			50		mV
V_{ILc}	SDA and SCL low-level input voltage contention	SDAA, SCLA	V_{CCA} ≥ 1.5 V and V_{CCB} ≥ 3.15 V	110	150		mV
			V_{CCA} < 1.5 V or V_{CCB} < 3.15 V	50	100		
V_{OLB}	Low-level output voltage	SDAB, SCLB	I_{OL} = 6 mA		0.1	0.2	V
I_{CC}	Quiescent supply current for V_{CCA}		All port A Static high	0.25	0.45	0.9	mA
			All port A Static low	1.25			
I_{CC}	Quiescent supply current for V_{CCB}		All port B Static high	0.2	0.5	1.1	mA
I_I	Input leakage current	SDAB, SCLB	V_I = V_{CCB}			±1	µA
			V_I = 0.2 V			10	
		SDAA, SCLA	V_I = V_{CCA}			±1	
			V_I = 0.2 V			10	
		EN	V_I = V_{CCB}			±1	
			V_I = 0.2 V			–10	
I_{OH}	High-level output leakage current	SDAB, SCLB	V_O = 3.6 V			10	µA
		SDAA, SCLA				10	
C_{IOA}	I/O capacitance of A-side	SCLA, SDAA	V_I = 0 V		6.5	7	pF
C_{IOB}	I/O capacitance of B-side	SCLB, SDAB	V_I = 0 V	5.5		6.2	pF

5.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition[(1)]	100		ns
t_h	Hold time, EN high after Stop condition[(1)]	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

5.7 I²C Interface Timing Requirements

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			V_{CCA} (INPUT)	V_{CCB} (OUTPUT)	TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
t_{PHL}	Propagation delay	port A to port B	1.9 V	5 V	EN High	123.1	127.2	132.8	ns
		port B to port A				88.1	88.8	89.8	
t_{PLH}	Propagation delay	port A to port B	1.9 V	5 V	EN High	122.6	125.7	131.7	ns
		port B to port A				123	124.1	126.9	
t_{rise}	Transition time	port A	1.9 V	5 V	EN High	40.1	40.9	41.9	ns
		port B				57.3	57.5	58.4	
t_{fall}	Transition time	port A	1.9 V	5 V	EN High	14.5	16.4	17.9	ns
		port B				18.7	19.4	20.2	
t_{PLH2}	Propagation delay 50% of initial low on Port A to 1.5 V on Port B	port A to port B	1.9 V	5 V		176	177.3	178	ns
f_{MAX}	Maximum switching frequency					400			KHz

(1) Typical values were measured with $V_{CCA} = V_{CCB}$ = 2.7 V at T_A = 25°C, unless otherwise noted.

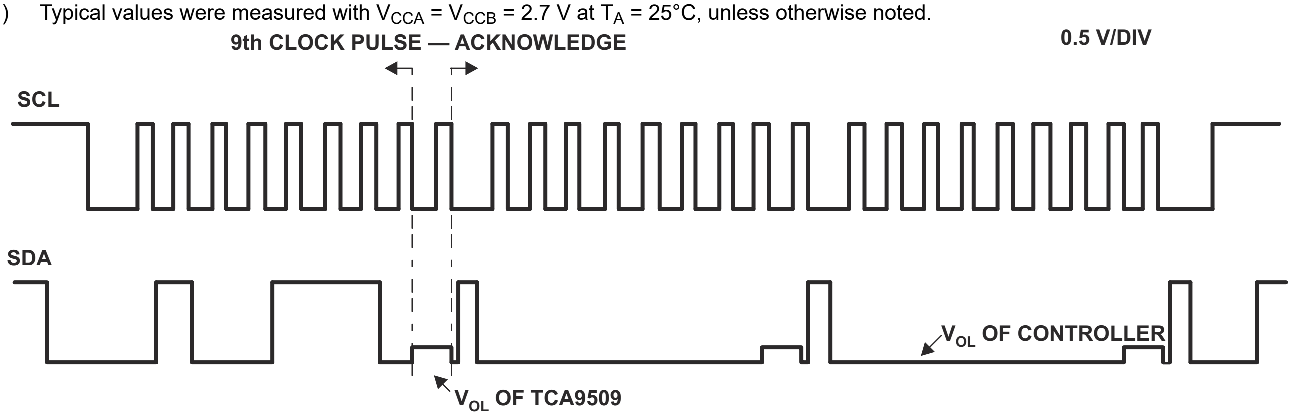


Figure 5-1. Bus A (0.9-V to 5.5-V Bus) Waveform

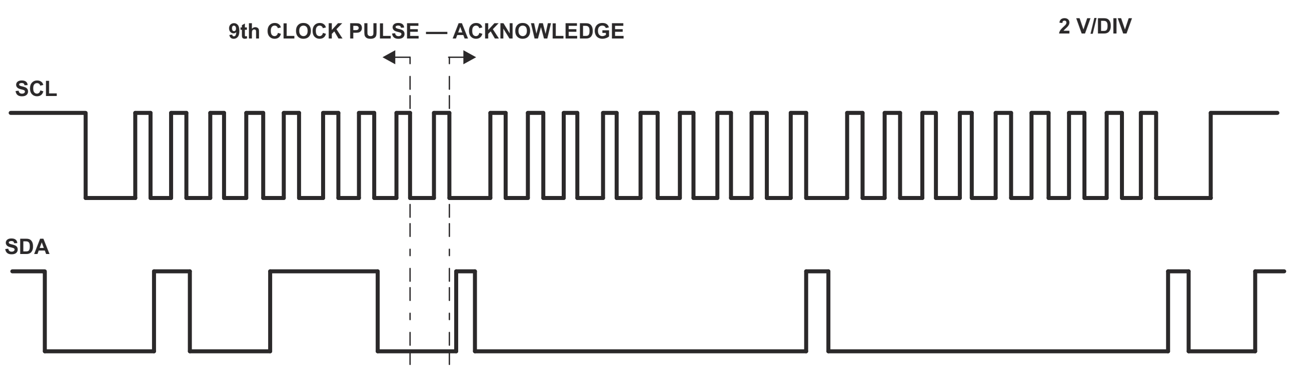
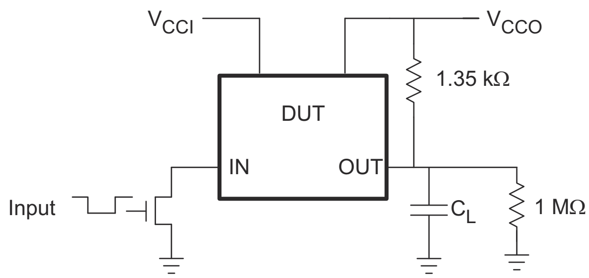
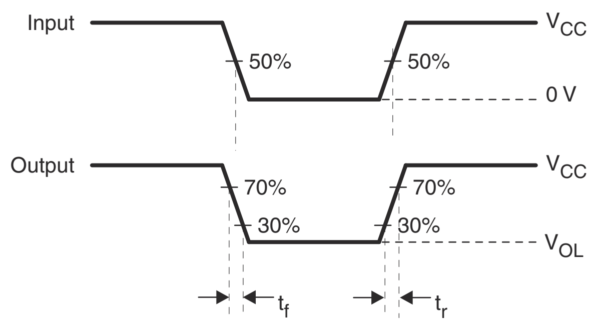


Figure 5-2. Bus B (2.7-V to 5.5-V Bus) Waveform

6 Parameter Measurement Information



PIN	C_L
SCLA, SDAA (A-side)	50 pF
SDAB, SCLB (B-side)	50 pF



A. R_T termination resistance should be equal to Z_{OUT} of pulse generators.

B. C_L includes probe and jig capacitance.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 6-1. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

This TCA9509 integrated circuit is an I²C bus/SMBus Repeater for use in I²C/SMBus systems. It can also provide bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

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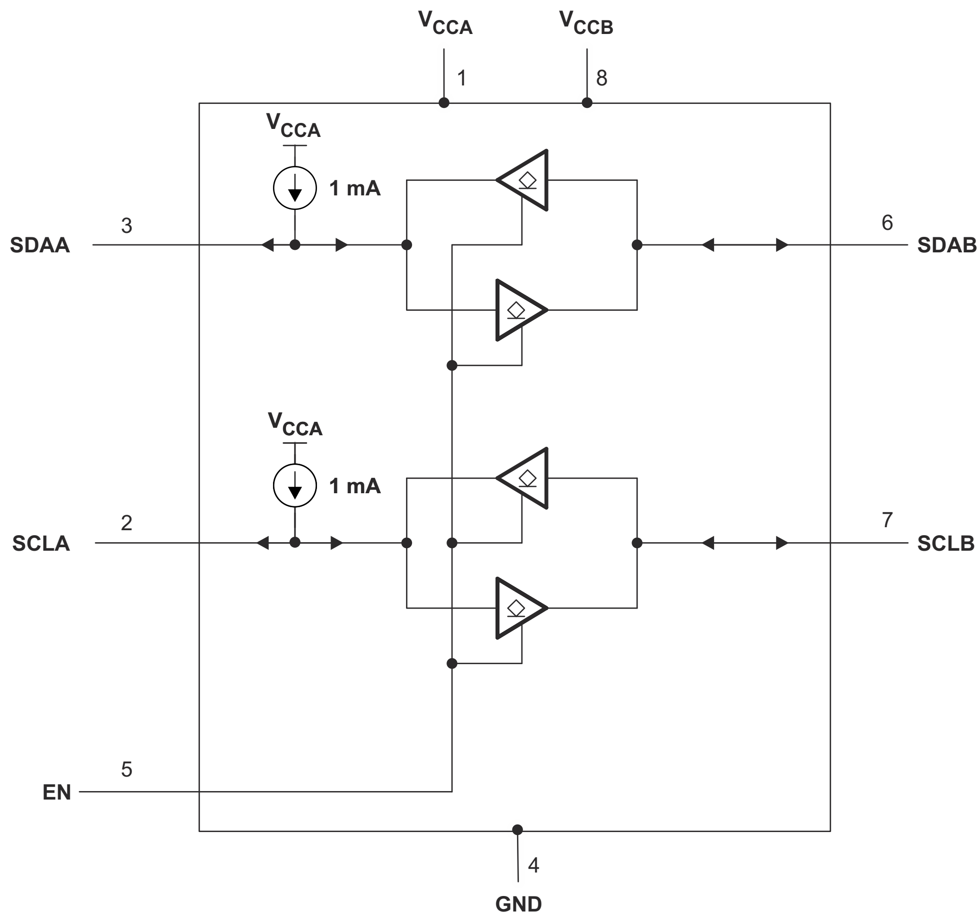
The TCA9509 has two types of drivers – A-side drivers and B-side drivers. All inputs and B-side I/O's are overvoltage tolerant to 5.5V. The A-side I/O's are overvoltage tolerant to 5.5 V when the device is unpowered (V_{CCB} and/or V_{CCA} = 0V).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Two-Channel Bidirectional Buffer

The TCA9509 is a two-channel bidirectional buffer with level-shifting capabilities, featuring an integrated current source on the A-side.

7.3.2 Integrated A-Side Current Source

The A-side ports of the TCA9509 feature an integrated 1 mA current source, eliminating the need for external pull-up resistors on SDAA and SCLA.

7.3.3 Standard Mode and Fast Mode Support

The TCA9509 supports standard mode as well as fast mode I^2C. The maximum system operating frequency will depend on system design and delays added by the repeater.

7.4 Device Functional Modes

Table 7-1 lists the functional modes for the TCA9509.

Table 7-1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TCA9509 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the B-side of the TCA9509 is pulled low by a driver on the I^2C bus and the falling edge goes below 0.3 V_{CCB}, it causes the internal driver on the A-side to turn on, causing the A-side to pull down to about 0.2 V (V_{OL}). When the A-side of the TCA9509 falls, a comparator detects the falling edge and causes the internal driver on the B-side to turn on and pull the B-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 5-1. If the bus controller in Figure 8-1 were to write to the target through the TCA9509, waveforms shown in Figure 5-2 would be observed on the B bus. This looks like a normal I^2C bus transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the A-side bus of the TCA9509, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9509. After the eighth clock pulse, the data line is pulled to the V_{OL} of the controller device, which is close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9509 for a short delay, while the B-bus side rises above 0.3 V_{CCB} and then continues high. It is important to note that any arbitration or clock stretching events require that the low level on the A-bus side at the input of the TCA9509 (V_{IL}) be at or below V_{ILC} to be recognized by the TCA9509 and then transmitted to the B-bus side.

8.2 Typical Application

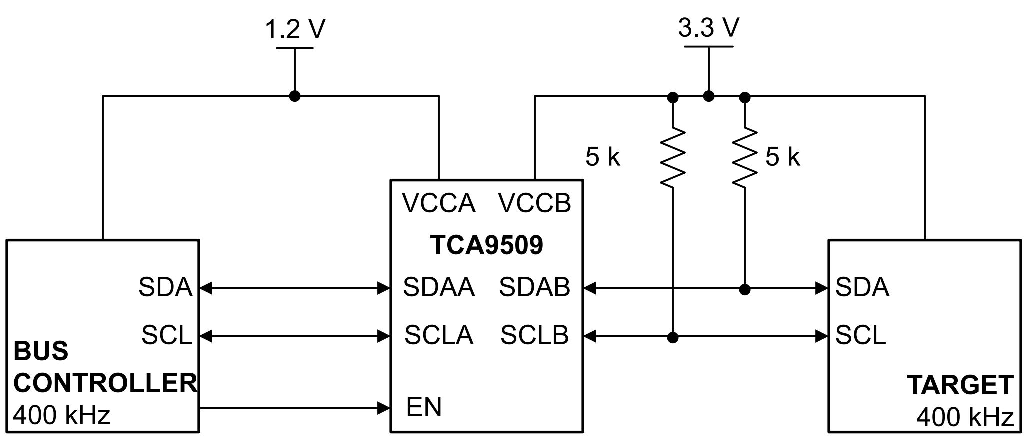


Figure 8-1. Typical Application, A-side Connected to controller

8.2.1 Design Requirements

A typical application is shown in Figure 8-1. In this example, the system controller is running on a 1.2-V I^2C bus, and the target is connected to a 3.3-V bus. Both buses run at 400 kHz. Controller devices can be placed on either bus. For the level translating application, the following should be true: $V_{CCA} \leq (V_{CCB} - 1\ V)$

- V_{CCA} = 0.9 V to 5.5 V
- V_{CCB} = 2.7 to 5.5 V
- A-side ports must not be connected together

- Pullup resistors should not be placed on the A-side ports

8.2.2 Detailed Design Procedure

8.2.2.1 Clock Stretching Support

The TCA9509 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the target and controller. This is best done by increasing the pull-up resistor value on B-side ports.

8.2.2.2 V_{ILC} and Pulldown Strength Requirements

For the TCA9509 to function correctly, all devices on the A-side must be able to pull the A-side below the voltage input low contention level (V_{ILC}). This means that the V_{OL} of any device on the A-side must be below V_{ILC} min.

The V_{OL} can be adjusted by changing the I_{OL}through the device which is set by the pull-up resistance value. The pull-up resistance on the A-side must be carefully selected to ensure that the logic levels will be transferred correctly to the B-side.

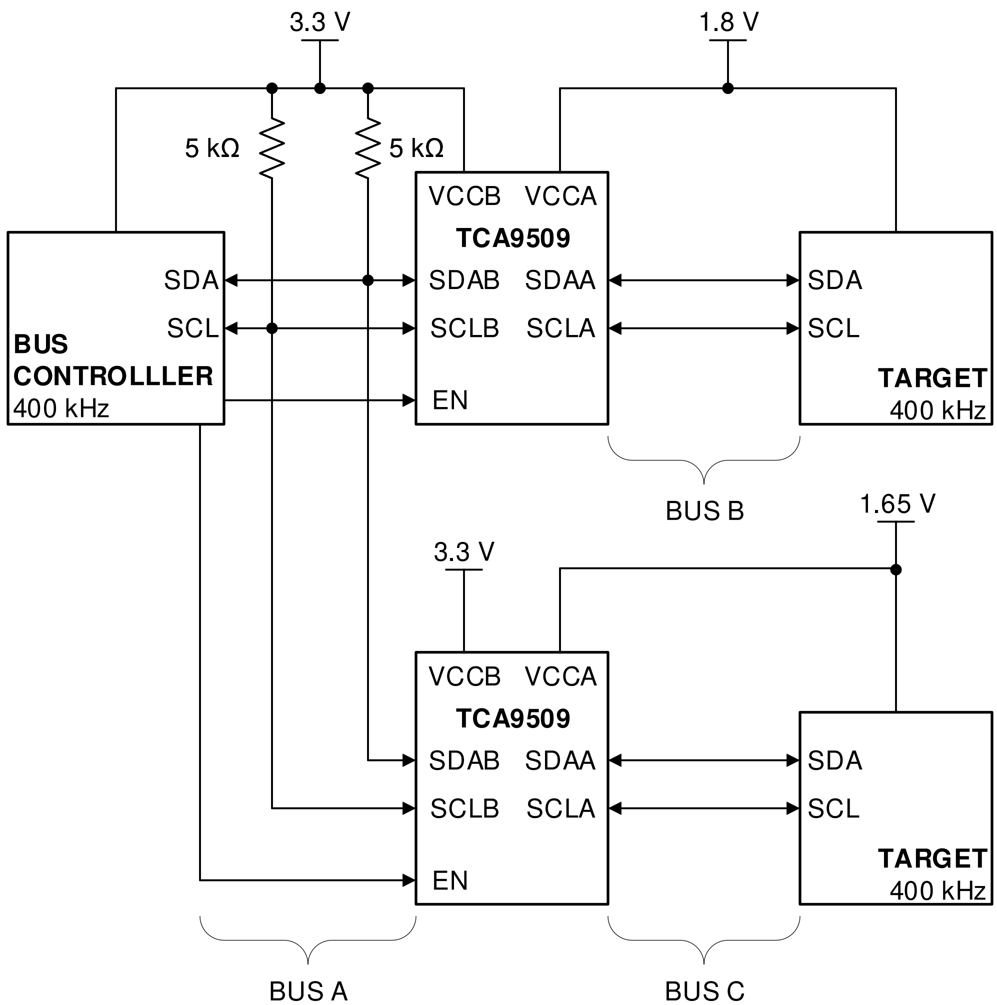


Figure 8-2. Typical Star Application

Multiple B-sides of TCA9509 can be connected in a star configuration, allowing all nodes to communicate with each other. The A-sides should not be connected together when used in a star/parallel configuration.

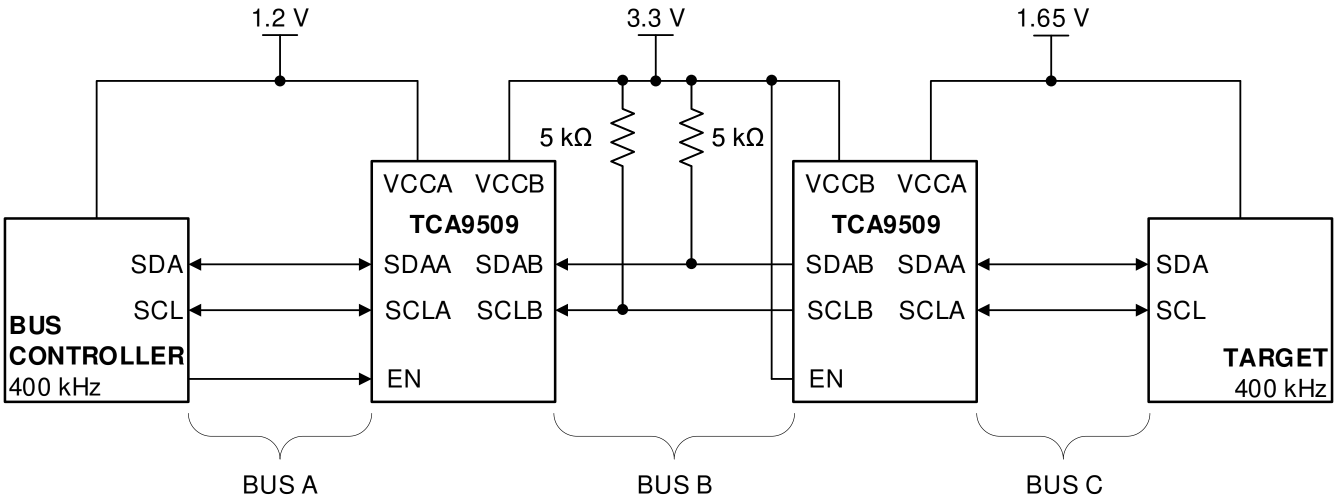


Figure 8-3. Typical Series Application, Two B-Sides Connected Together

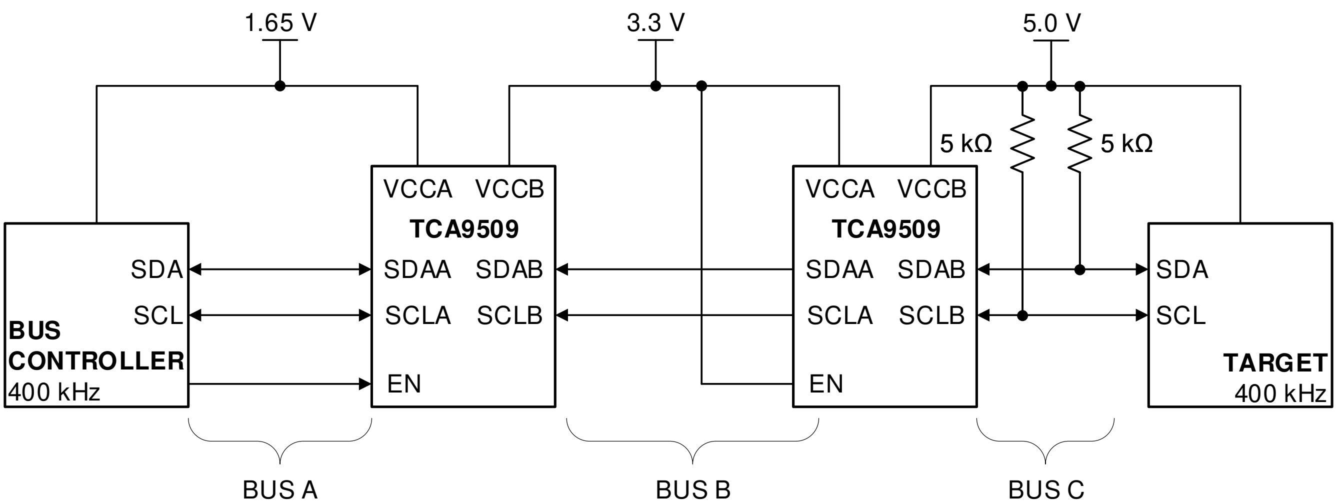


Figure 8-4. Typical Series Application, A-side Connected to B-Side

To further extend the I²C bus for long traces/cables, multiple TCA9509 devices can be connected in series as long as the A-side is connected to the B-side and $V_{CCA} \leq (V_{CCB} – 1\ V)$ must also be met. Series connections can also be made by connecting both B-sides together while following power supply rule $V_{CCA} \leq (V_{CCB} – 1\ V)$. I²C bus target devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

9 Power Supply Recommendations

V_{CCB} and V_{CCA} can be applied in any sequence at power up. The TCA9509 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. After power up and with the EN high, a low level on the B-side (below 0.3 × V_{CCB}) turns the corresponding A-side driver (either SDA or SCL) on and drives the A-side down to approximately 0.2 V. When the B-side rises above 0.3 × V_{CCB}, the A-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the A-side falls first and goes below 0.3 × V_{CCA}, the B-side driver is turned on and the B-side pulls down to 0 V. The A-side pull-down is not enabled unless the A-side voltage goes below 0.4 V. If the A-side low voltage does not go below 0.5 V, the B-side driver turns off when the A-side voltage is above 0.7 × V_{CCA}. If the A-side low voltage goes below 0.4 V, the A-side pull-down driver is enabled, and the A-side is able to rise to only 0.5 V until the B-side rises above 0.3 × V_{CCB}.

A 100 nF a decoupling capacitor should be placed as close to the V_{CCA} and V_{CCB} pins in order to provide proper filtering of supply noise.

10 Layout

10.1 Layout Guidelines

There are no special layout procedures required for the TCA9509.

It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

10.2 Layout Example

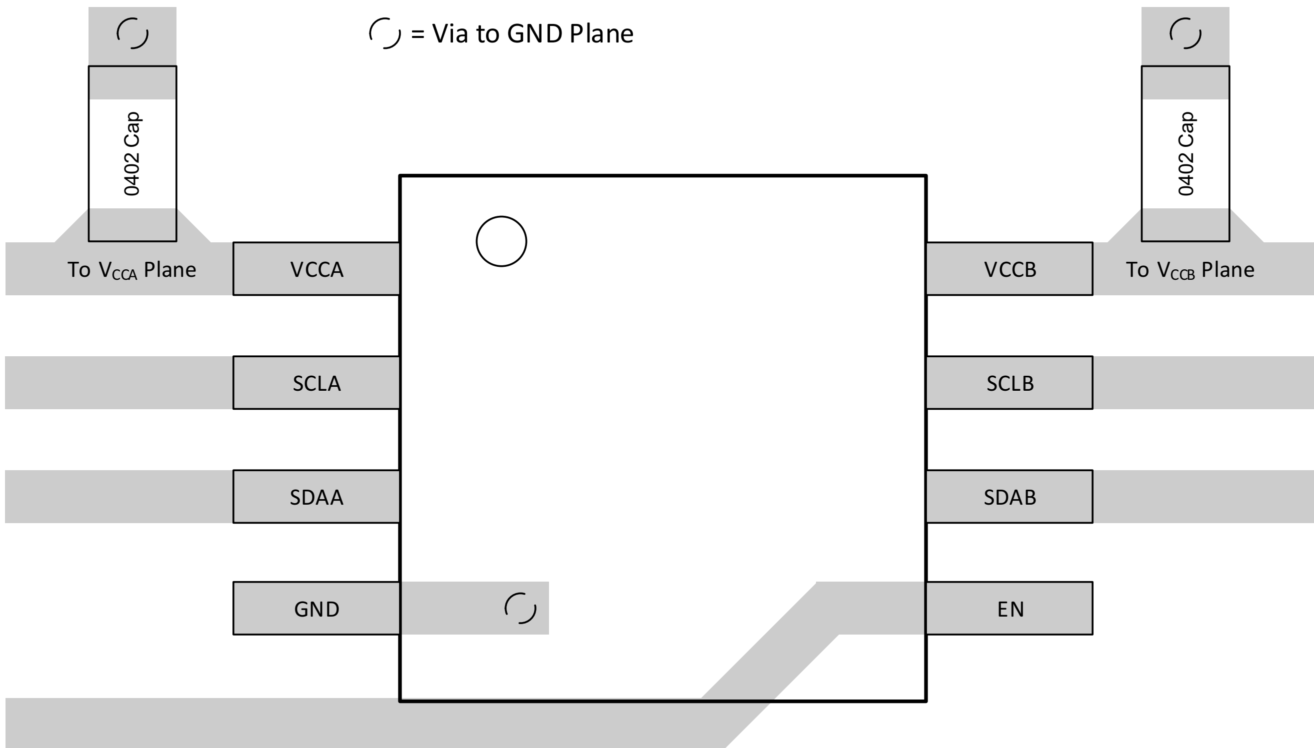


Figure 10-1. Example Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2021) to Revision E (October 2024)	Page
• Updated Tape and Reel Information	18

Changes from Revision C (December 2017) to Revision D (April 2021)	Page
• Changed the terms *master and slave* To *controller and target* in the data sheet	1
• Changed I_{CC} Quiescent supply current for V_{CCB} MIN value from 0.5 mA to 0.20 mA and the TYP value from 0.9 mA to 0.5 mA in the *Electrical Characteristics* table	6
• Changed text From: "Multiple B-sides of TCA9509 s..." To: "Multiple B-sides of TCA9509..."	12
• Updated Tape and Reel Information	18

Changes from Revision B (January 2012) to Revision C (December 2017)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added junction temperature to the *Absolute Maximum Ratings*	5
• Changed thermal information for RVH and DGK packages	6
• Changed V_{ILC}, added Test Conditions with new MIN and TYP values in the *Electrical Characteristics* table	6
• Updated Bus A (0.9-V to 5.5-V Bus) Waveform	7
• Updated Bus B (2.7-V to 5.5-V Bus) Waveform	7

Changes from Revision A (October 2011) to Revision B (January 2012)	Page
• Added DGK package and package information to datasheet.	1

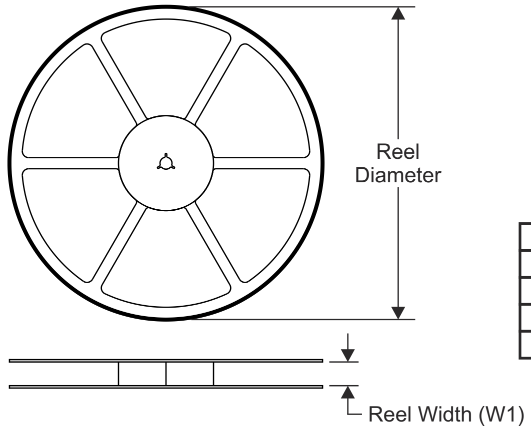
Changes from Revision * (August 2011) to Revision A (October 2011)	Page
• Corrected V_{CCA} operating voltage lower limit, to 0.9 V at multiple instances in document	1
• Changed Operating Supply Voltage Range value error in FEATURES for B side. Changed from (0.9 V to 5.5 V on B side) to (2.7 V to 5.5 V on B side)	1
• Changed Operating Voltage Range value error in FEATURES for A side. Changed (2.7 V to V_{CCB} – 1 V on A side) to (0.9 V to V_{CCB} – 1 V on A side)	1

13 Mechanical, Packaging, and Orderable Information

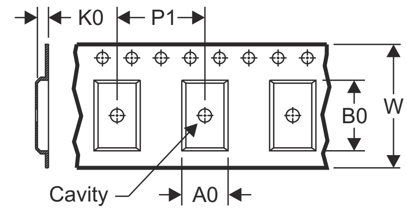
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Tape and Reel Information

REEL DIMENSIONS

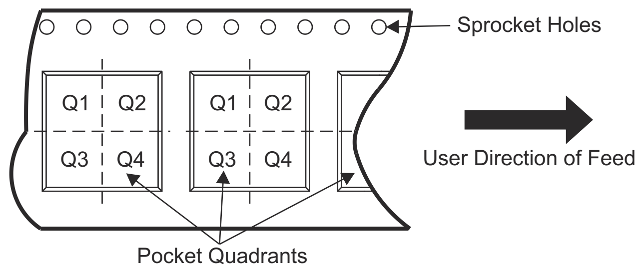


TAPE DIMENSIONS



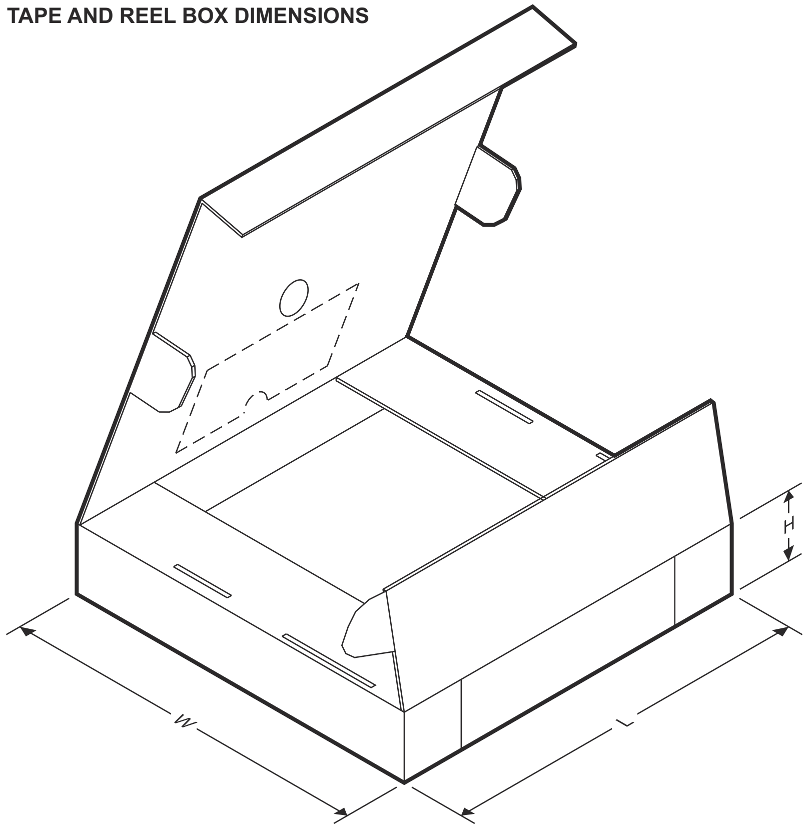
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9509MRVHR	X2QFN	RVH	8	5000	180.0	8.4	1.8	1.8	0.5	4.0	8.0	Q1
TCA9509RVHR	X2QFN	RVH	8	5000	180.0	8.4	1.8	1.8	0.5	4.0	8.0	Q3
TCA9509DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9509MRVHR	X2QFN	RVH	8	5000	183.0	183.0	20.0
TCA9509RVHR	X2QFN	RVH	8	5000	202.0	201.0	28.0
TCA9509DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCA9509DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(7KO, 7KQ)
TCA9509DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7KO, 7KQ)
TCA9509DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7KO, 7KQ)
TCA9509MRVHR	Active	Production	X2QFN (RVH) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7K
TCA9509MRVHR.A	Active	Production	X2QFN (RVH) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7K
TCA9509MRVHR.B	Active	Production	X2QFN (RVH) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7K
TCA9509RVHR	Active	Production	X2QFN (RVH) | 8	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7K
TCA9509RVHR.A	Active	Production	X2QFN (RVH) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7K
TCA9509RVHR.B	Active	Production	X2QFN (RVH) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7K

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

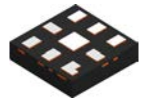
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

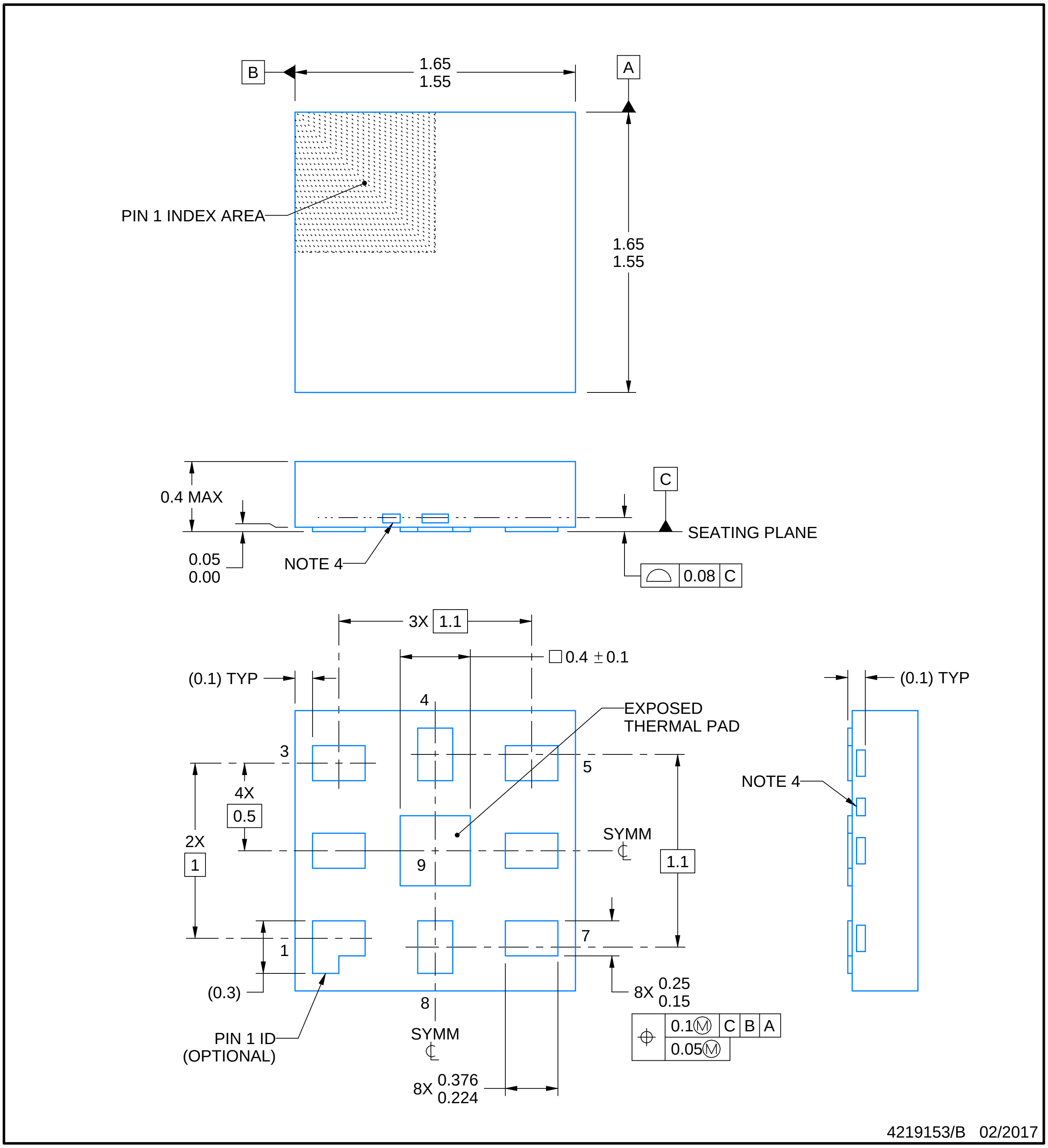


PACKAGE OUTLINE

RVH0008A

X2QFN - 0.4 mm max height

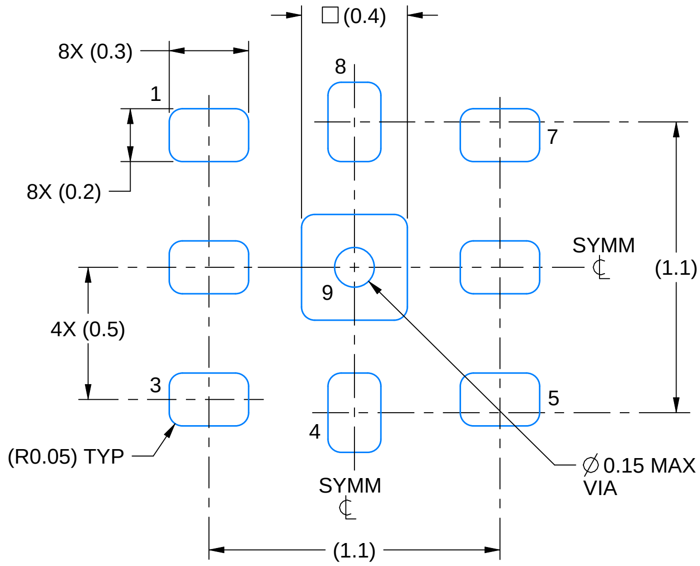
PLASTIC QUAD FLATPACK - NO LEAD



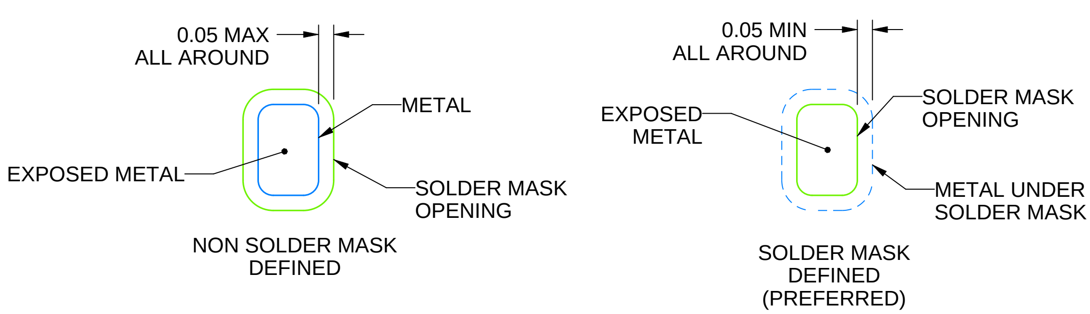
4219153/B 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed tie bars may vary in size and location.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:35X

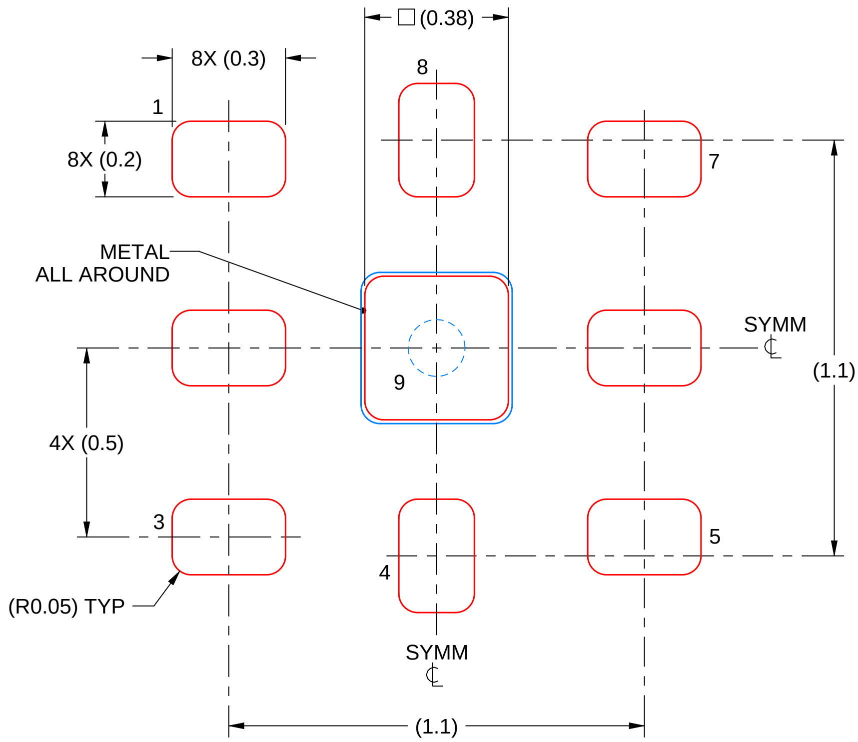


SOLDER MASK DETAILS

4219153/B 02/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



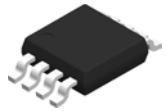
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

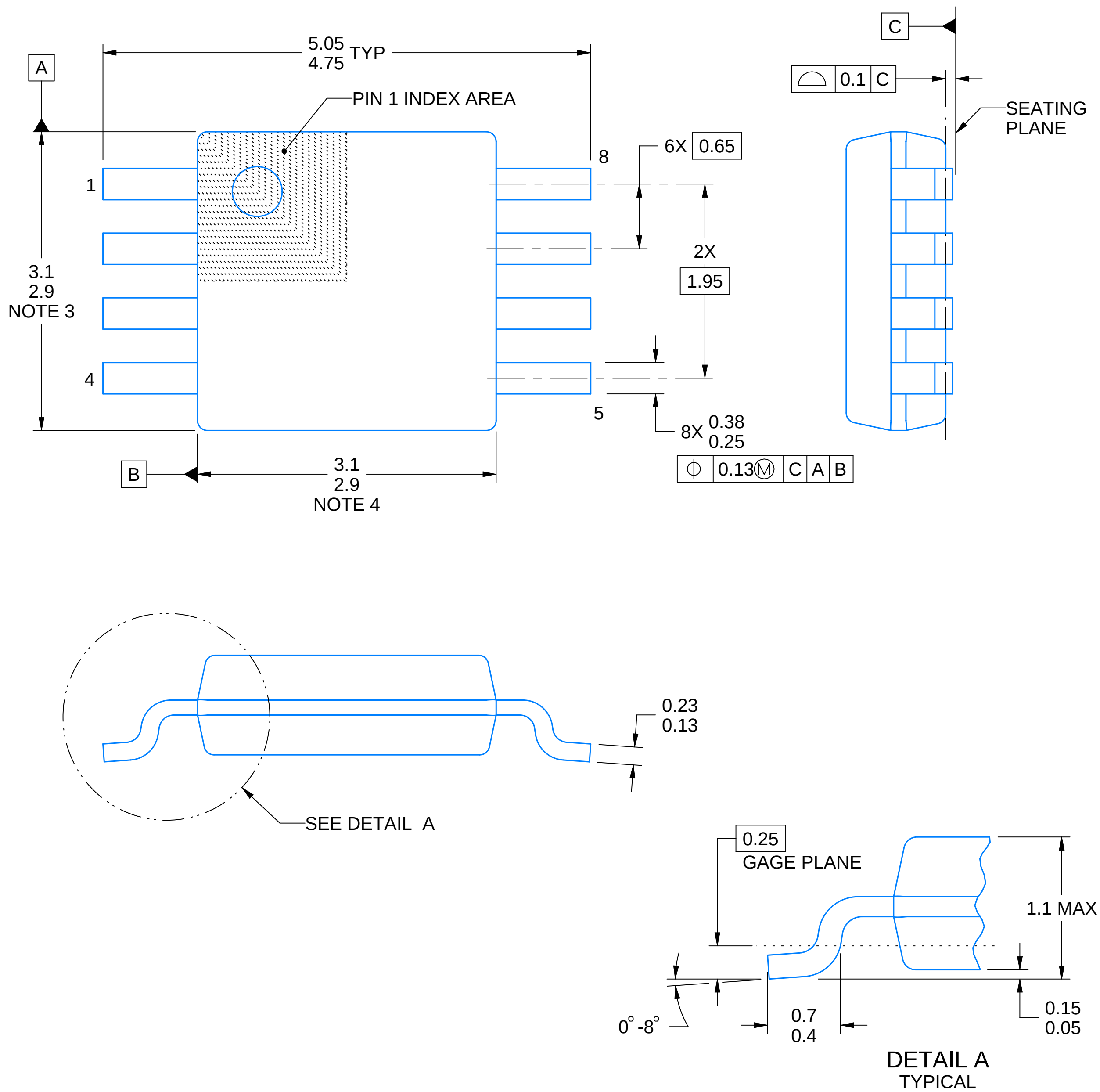
EXPOSED PAD 9
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4219153/B 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



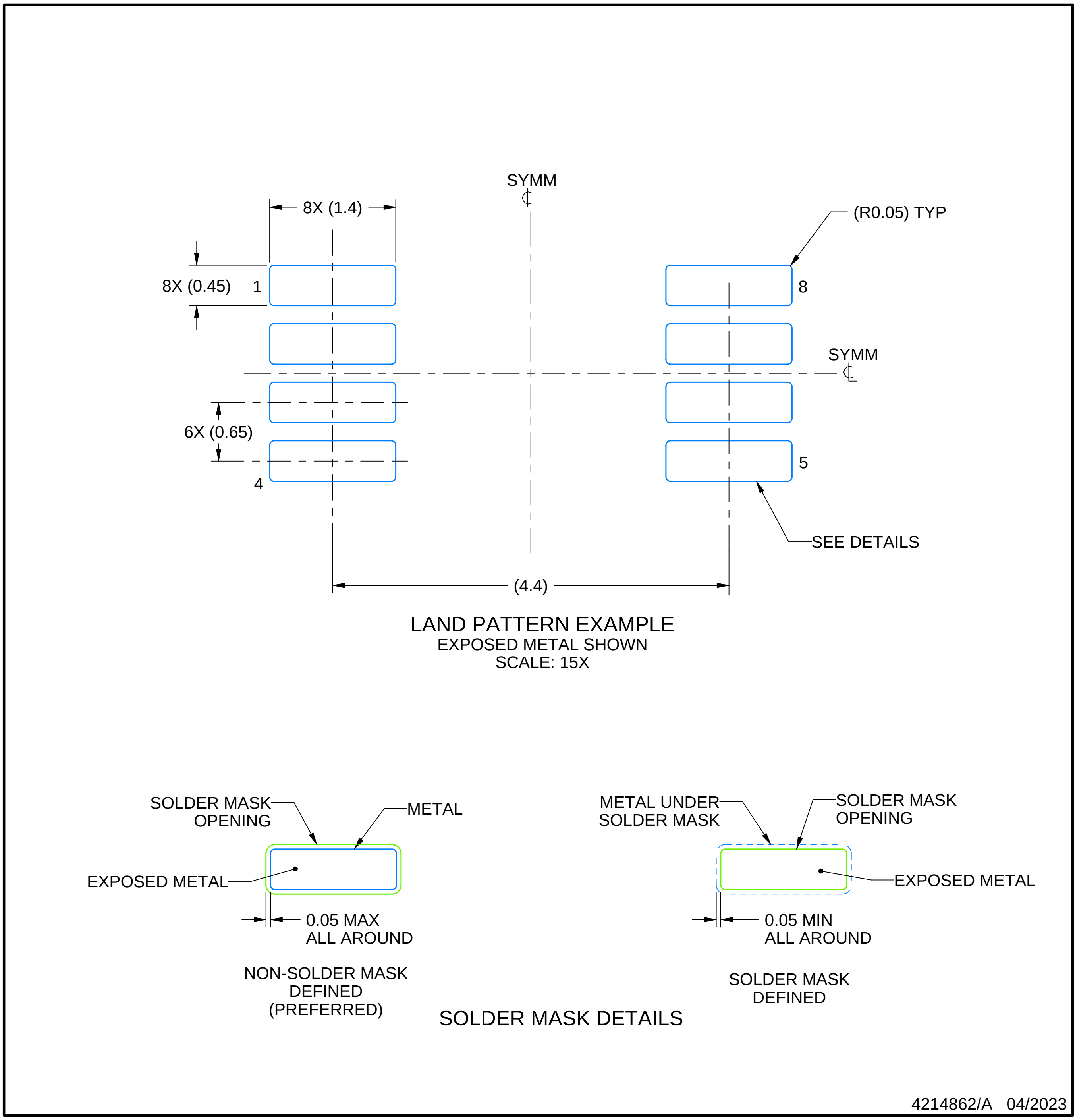


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

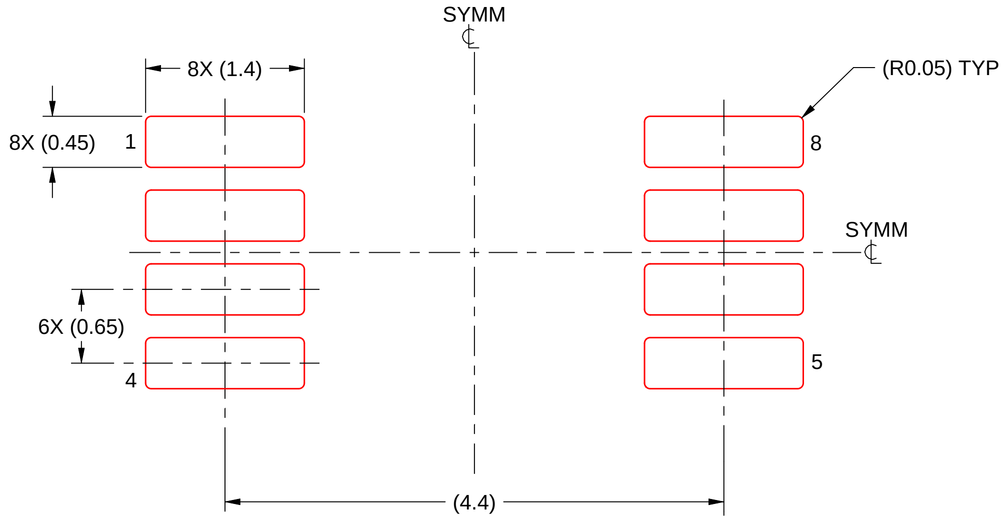
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.