4.5V-60V Vin, 1.5A, High Efficiency Step-down DCDC Converter

FEATURES

- Wide Input Range: 4.5V-60V
- Continuous Output Current: 1.5A
- Peak Output Current: 2A
- 0.8V Feedback Reference Voltage
- Integrated 500mΩ High-Side
- Low Quiescent Current: 80uA
- Pulse Skipping Mode (PSM) in light load
- 80ns Minimum On-time
- 6ms Internal Soft-start Time
- Internal compensation
- Switching Frequency 480kHz
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Low Dropout Mode Operation
- Over-voltage and Over-Temperature Protection
- Available in an ESOP-8L Package

APPLICATIONS

- 12-V, 24-V, 48-V Industry and Telecom Power System
- Industrial Automation and Motor Control
- Vehicle Accessories
- Portable Handheld Instruments
- Portable Media Players

DESCRIPTION

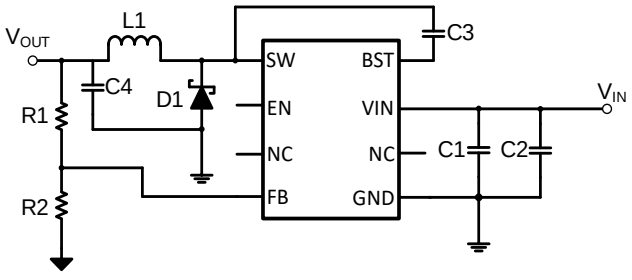
The SCT2617 is 1.5A buck converter with wide input voltage, ranging from 4.5V to 60V, which integrates an 500mΩ high-side MOSFET. The SCT2617, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with 80uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The SCT2617 features fixed 480kHz switching frequency, which minimizes the external off chip passive components size and reduces the output ripple. The SCT2617 allows power conversion from high input voltage to low output voltage with a minimum 80ns on-time of high-side MOSFET and supports low dropout operation with a low voltage difference from input to output.

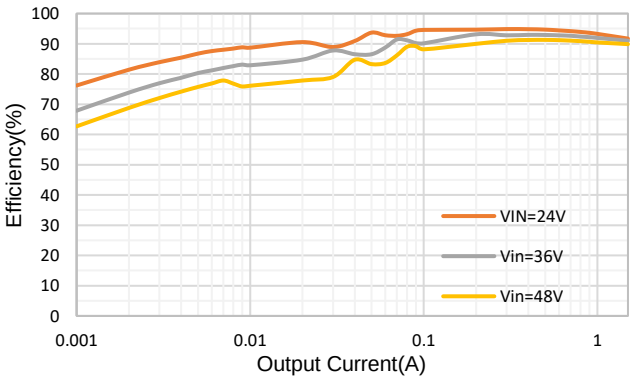
The device offers fixed 6ms soft start to prevent inrush current during the startup of output voltage ramping, and compensation circuits are implemented internally which allows the device to be used with minimized external components.

The SCT2617 provides cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an ESOP-8L package.

TYPICAL APPLICATION



4.5V-60V, Asynchronous Buck Converter



Efficiency, Vout=12V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

Revision 1.1: Update TAPE AND REEL INFORMATION.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2617STER	Tape & Reel	4000	2617	8	ESOP-8L	3

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	65	V
BST	-0.3	71	V
SW	-1	65	V
BST-SW	-0.3	6	V
FB	-0.3	6	V
Operating junction temperature TJ (2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION

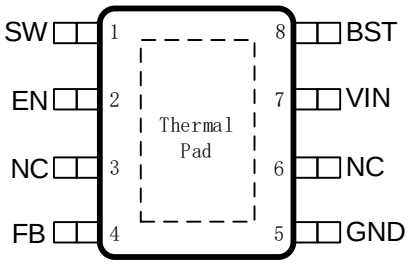


Figure 1. 8-Lead Plastic ESOP

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
SW	1	Regulator switching output. Connect SW to an external power inductor
EN	2	Enable pin to the regulator with internal pull-up current source. Pull below 1.13V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
NC	3	Not connected.
FB	4	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typically.
GND	5	Ground.
NC	6	Not connected.
VIN	7	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin
BST	8	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.5	60	V
V_{OUT}	Output voltage range	0.8	57	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-1	1	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (2)	-1	1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ESOP-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (1)	47.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.5	
Ψ_{JB}	Junction-to-board characterization parameter (1)	26	
$R_{\theta JCtop}$	Junction to case thermal resistance (1)	86.2	
$R_{\theta JB}$	Junction-to-board thermal resistance (1)	15.7	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2617 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2617. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual RθJA and RθJC.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		4.5		60	V
V_{IN_UVLO}	Input UVLO Threshold Hysteresis	V_{IN} rising		4.23 200	4.45	V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		2	5	μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching		80		μA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		500		mΩ
Reference						
V_{REF}	Reference voltage of FB		0.77	0.8	0.83	V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		2.8	3.5	4.1	A
Enable and Soft Startup						
V_{EN_H}	Enable high threshold			1.223	1.4	V
V_{EN_L}	Enable low threshold		0.9	1.13		V
V_{EN_HYS}	Enable threshold hysteresis			93		mV
I_{EN_L}	Enable pin pull-up current	EN=1V		1		μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		4		uA
T_{SS}	Soft start time			6		ms
Switching Frequency						
F_{SW}	Switching frequency		390	480	566	kHz
t_{ON_MIN}	Minimum on-time	V_{IN}=12V		100		ns
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising V_{FB}/V_{REF} falling		110 105		% %
V_{BOOTUV}	BOOT-SW UVLO threshold	BOOT-SW falling Hysteresis		2.2 250		V mV
T_{SD}	Thermal shutdown threshold*	T_J rising Hysteresis		173 10		°C °C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

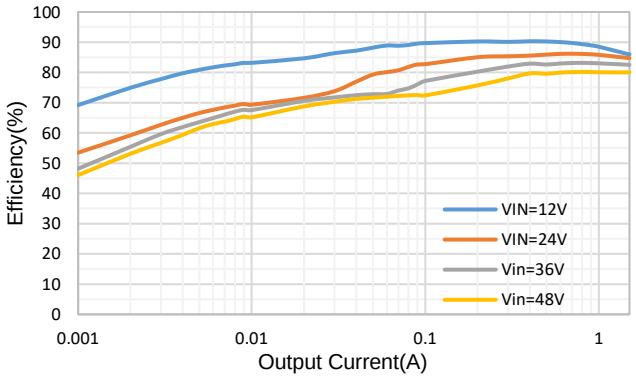


Figure 2. Efficiency vs Load Current, Vout=5V

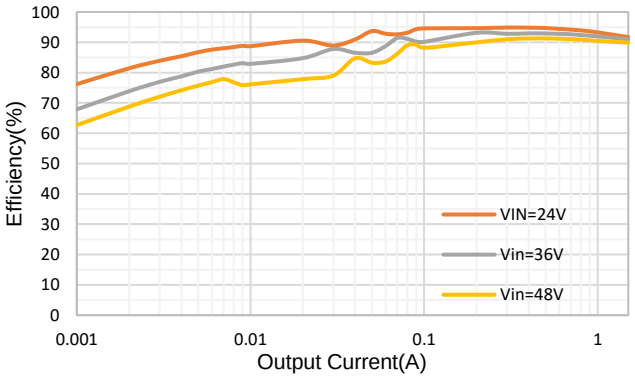


Figure 3. Efficiency vs Load Current, Vout=12V

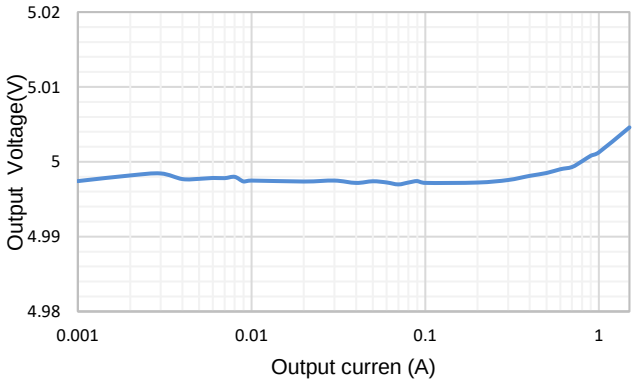


Figure 4. Load Regulation, Vin=24V, Vout=5V

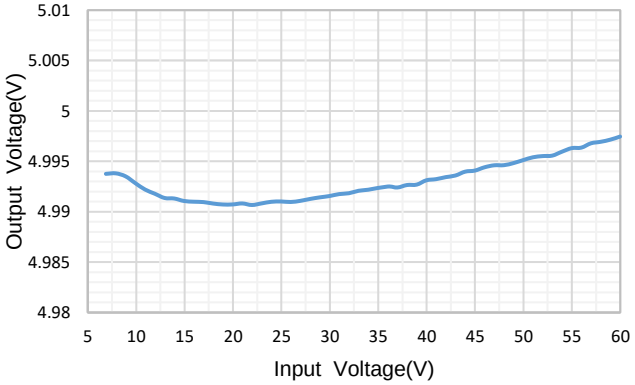


Figure 5. Line Regulation, Vout=5V, Iout=1.5A

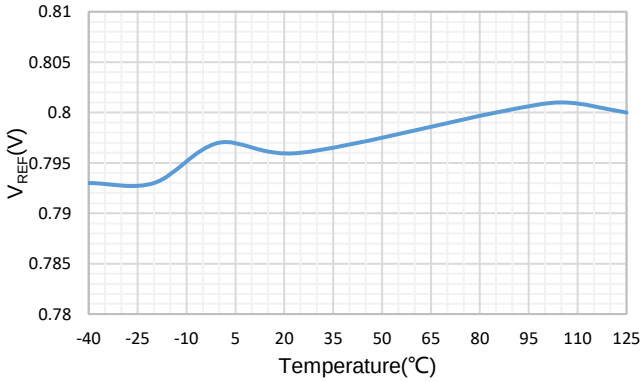


Figure 6. Reference Voltage VS Temperature

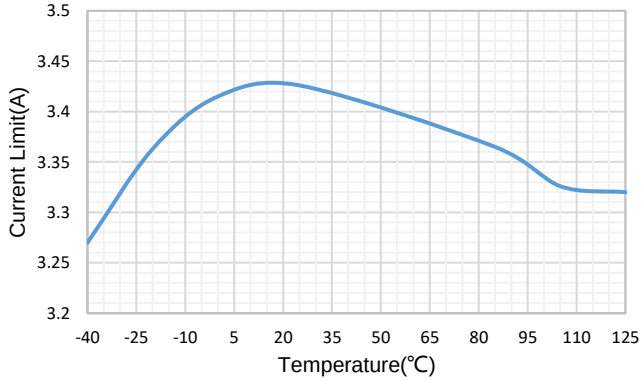


Figure 7. HS Current Limit VS Temperature

FUNCTIONAL BLOCK DIAGRAM

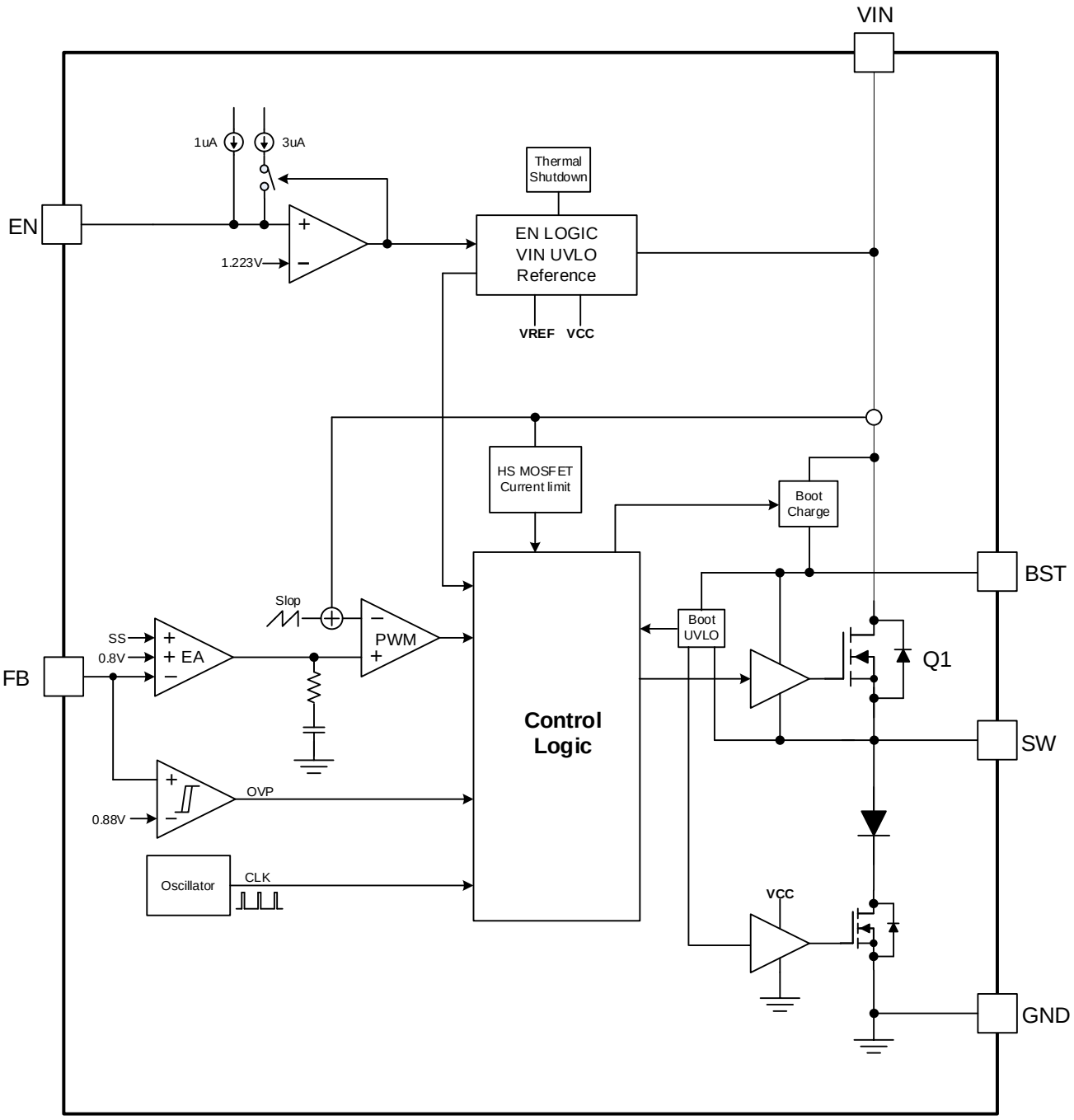


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT2617 is a 4.5V-60V input, 1.5A output, buck converter with integrated 500mΩ Rdson high-side power MOSFET. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response.

The SCT2617 features fixed 480kHz switching frequency, which minimizes the external off chip passive components size and reduces the output ripple. The SCT2617 features an internal 6ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 80uA under no load or sleep mode condition to achieve high efficiency at light load.

The SCT2617 has a default input start-up voltage of 4.23V with 200mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2617 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2617 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the integrated high-side MOSFET is turned off.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2617 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (450mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 140mA peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 80uA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The SCT2617 is enabled when the VIN pin voltage rises above 4.23V and the EN pin voltage exceeds the enable threshold of 1.223V. The device is disabled when the VIN pin voltage falls below 4.03V or when the EN pin voltage is below 1.13V. An internal 1uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R3 and R4) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$R3 = \frac{V_{rise} * 0.924 - V_{fall}}{3.076uA} \quad (1)$$

$$R4 = \frac{R_3 \times 1.13}{V_{fall} - 1.13 + R_3 * 4uA} \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

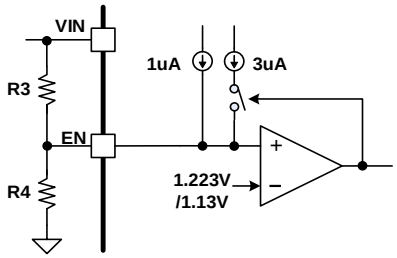


Figure 9. System UVLO by enable divide

Output Voltage

The SCT2617 regulates the internal reference voltage at 0.8V typical over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

Where:

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2617 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 6ms. If the EN pin is pulled below 1.13V, switching stops and the internal soft-start resets. The soft start also resets during shutdown due to thermal overloading.

Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 μF.

The UVLO of high-side MOSFET gate driver has rising threshold of 2.45V and hysteresis of 250mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.2V, BOOT UVLO occurs. The converter forces turning on an integrated low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, SCT2617 operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.45V. When the voltage from BOOT to SW drops below 2.2V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 200ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.45V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%.

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e., during slowing

power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2617 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

Over Current Limit

The SCT2617 implements over current protection with fold back current limit. The SCT2617 cycle-by-cycle limits high-side MOSFET peak current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously.

The SCT2617 implements frequency fold back to protect the converter in unexpected overload or output hard short condition at higher switching frequencies and input voltages. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8V to 0V. The SCT2617 uses a digital frequency fold back to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current can exceed the peak current limit because of the high input voltage and the minimum on-time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off-time. The frequency fold back effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency fold back ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency fold back protection. Equation 4 calculates the maximum switching frequency at which the inductor current remains under control when V_{OUT} is forced to V_{OUT_SHORT}. The selected operating frequency must not exceed the calculated value.

$$f_{sw(\max skip)} = \frac{f_{DIV}}{t_{min\_ON}} \times \left(\frac{I_{LIMIT} \times R_{DC} + V_{OUT\_SHORT} + V_d}{V_{IN\_MAX} - I_{LIMIT} \times R_{DS(on)} + V_d}\right) \quad (4)$$

Where:

I_{LIMIT}: Limited average current.

R_{DC}: Inductor DC resistance.

V_{IN_MAX}: Maximum input voltage.

V_{OUT_SHORT}: Output voltage during short.

V_d: Diode voltage drop.

$R_{DS(on)}$: Integrated high side FET on resistance.

T_{min_ON}: Controllable minimum on time.

f_{DIV}: Frequency divide equals (1,2,4 or 8).

Over voltage Protection

The SCT2617 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

The SCT2617 protects the device from the damage during excessive heat and power dissipation conditions. Once

the junction temperature exceeds 173℃, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 163℃, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

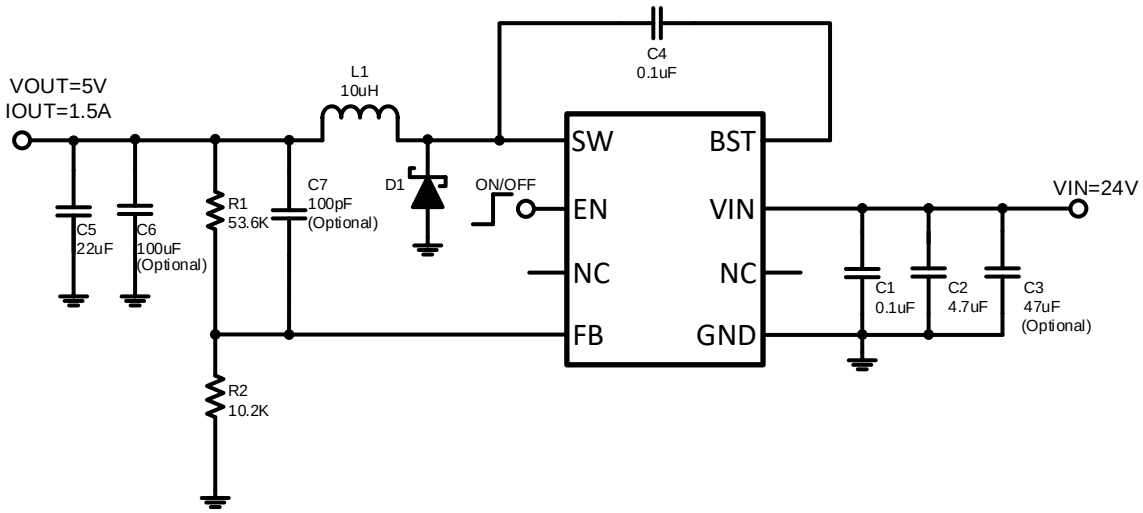


Figure 10. SCT2617 Design Example, 5V Output with Programmable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal, 6V~60V
Output Voltage	5V
Maximum Output Current	1.5A
Switching Frequency	480kHz
Output voltage ripple (peak to peak)	30mV
Transient Response 0.38A to 1.12A load step	ΔVout = 760mV
Start Input Voltage (rising VIN)	4.23V
Stop Input Voltage (falling VIN)	4.03V

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 10.2KΩ. Use Equation 5 to calculate R1.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_2 \quad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V

Table 1. R_1, R_2Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
3.3V	31.6 KΩ	10.2 KΩ
5V	53.6 KΩ	10.2 KΩ
12 V	143 KΩ	10.2 KΩ
24V	294 KΩ	10.2 KΩ

Under Voltage Lock-Out

An external voltage divider network from the input to EN pin and EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 4.23V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.02V (stop or disable). Use Equation 6 and Equation 7 to calculate the values of R_{TOP} and R_{BOT} resistors.

$$R_{TOP} = \frac{V_{rise} * 0.924 - V_{fall}}{3.076uA} \quad (6)$$

$$R_{BOT} = \frac{R_{TOP} \times 1.13}{V_{fall} - 1.13 + R_{TOP} * 4uA} \quad (7)$$

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 8.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (8)$$

Where:

- I_{LPP} is the inductor peak-to-peak current.
- L is the inductance of inductor.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 9 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (9)$$

Where:

- L_{MIN} is the minimum inductance required.
- f_{sw} is the switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN(max)}$ is the maximum input voltage.
- $I_{OUT(max)}$ is the maximum DC load current.
- LIR is coefficient of I_{LPP} to I_{OUT}.

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 10 and Equation 11.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (10)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (11)$$

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 3.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 3.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2617 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Diode Selection

The SCT2617 requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than VIN (max). The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60-V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SCT2617.

For the example design, the B360A-13-F Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the B360A-13-F is 0.41 volts at 1.5A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off time of the internal power switch. The off time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be considered. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 12 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The B360A-13-F diode has a junction capacitance of 50 pF. Using Equation 12, the total loss in the diode at the maximum input voltage is 0.6W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{(V_{IN\_MAX} - V_{OUT}) \times I_{OUT} \times V_d}{V_{IN\_MAX}} + \frac{C_j \times f_{SW} \times (V_{IN\_MAX} + V_d)^2}{2} \quad (12)$$

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g., 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 13.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (13)$$

The worst-case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (14)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

For this example, one 4.7μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output

capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 16 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}{}^2 * L * C_{OUT} * V_{IN}} \quad (16)$$

Where:

- $\Delta V_{OUT}$is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 22μF ceramic output capacitors work for most applications.

Table 2. Recommended External Components

Vout	L1	COUT	R1	R2
5V	10uH	22uF	53.6 KΩ	10.2k
12V	33uH	22uF	143 KΩ	10.2k
24V	47uH	2*22uF	294 KΩ	10.2k

Application Waveforms

V_{IN}=24V, V_{OUT}=5V, F_{SW}=480k, unless otherwise noted

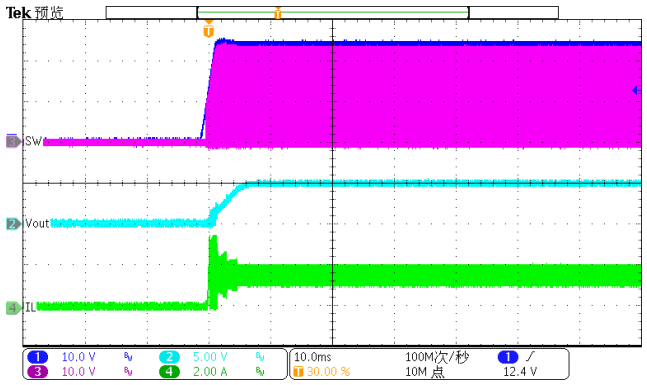


Figure 11. Power up (I_{LOAD}=1.5A)

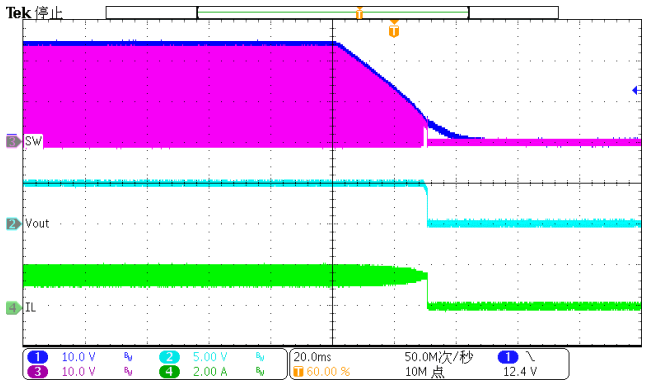


Figure 12. Power down (I_{LOAD}=1.5A)

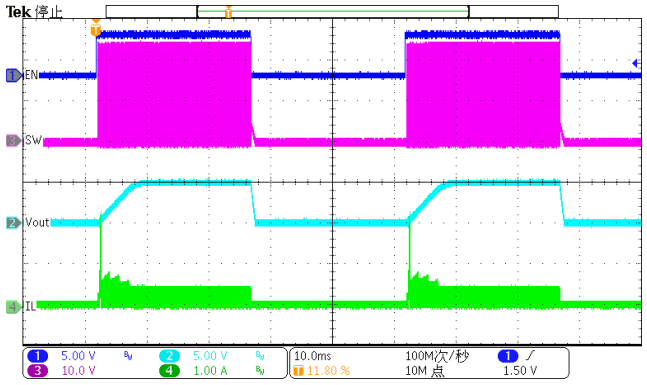


Figure 13. EN toggle (I_{LOAD}=0.1A)

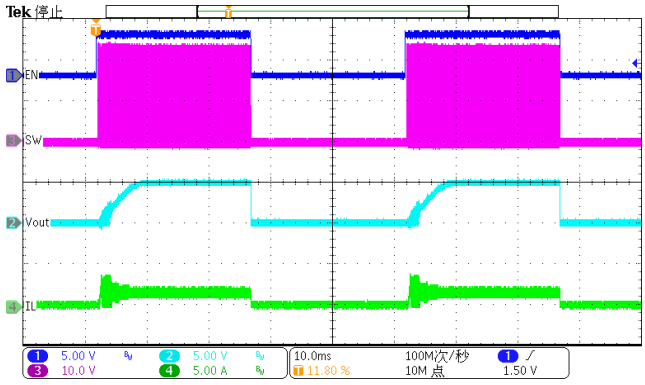


Figure 14. EN toggle (I_{LOAD}=1.5A)

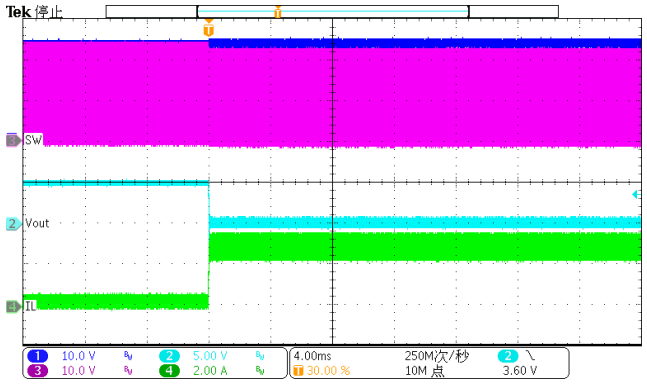


Figure 15. Over Current Protection (0.1A to hard short)

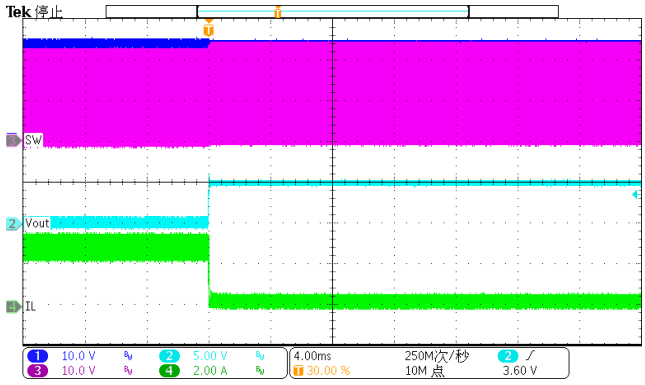


Figure 16. Over Current Release (hard short to 0.1A)

Application Waveforms

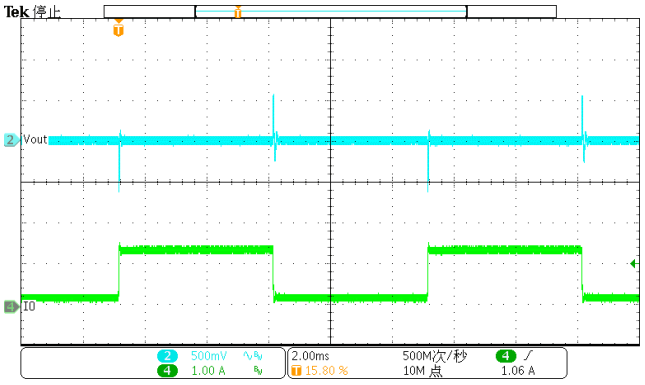


Figure 17. Load Transient (0.15A-1.35A, 1.6A/us)

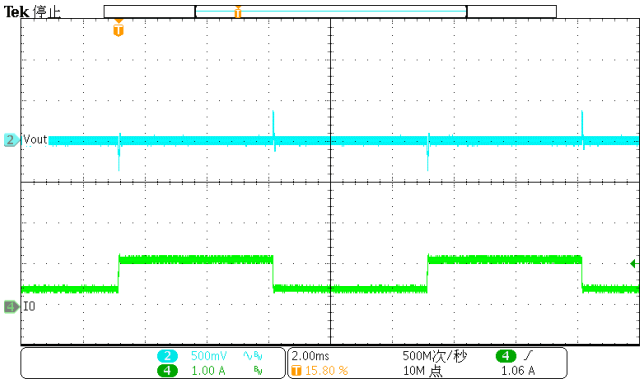


Figure 18. Load Transient (0.38A-1.12A, 1.6A/us)

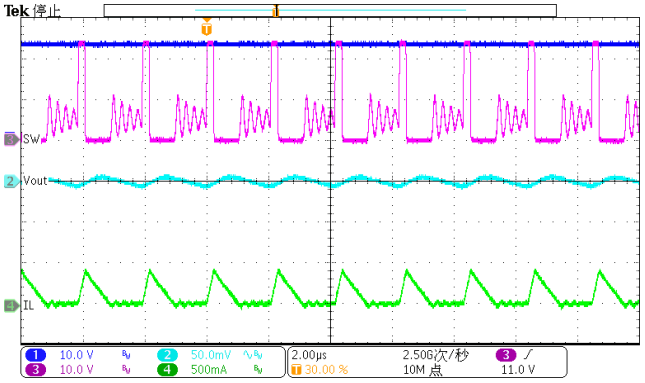


Figure 19. Output Ripple (I_{LOAD}=0.1mA)

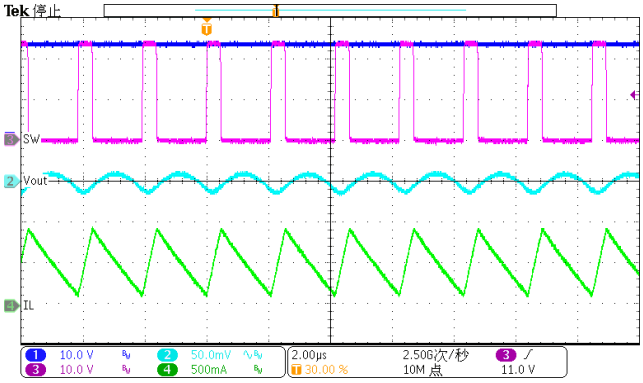


Figure 20. Output Ripple (I_{LOAD}=0.5A)

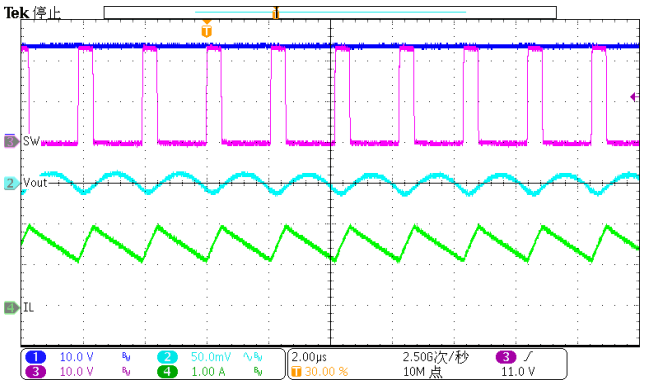


Figure 21. Output Ripple (I_{LOAD}=1.5A)

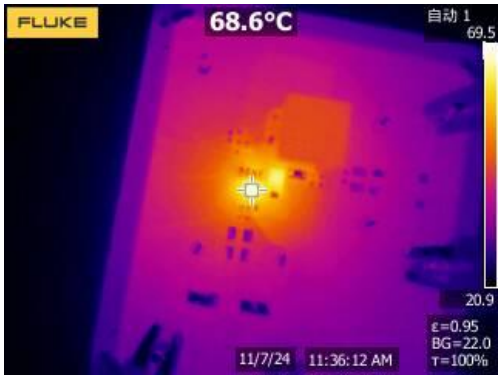


Figure 22. Thermal, 24V_{IN}, 5V_{OUT}, 1.5A

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential.

1. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling.
2. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. UVLO adjust and RT resistors, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
5. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.
6. The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

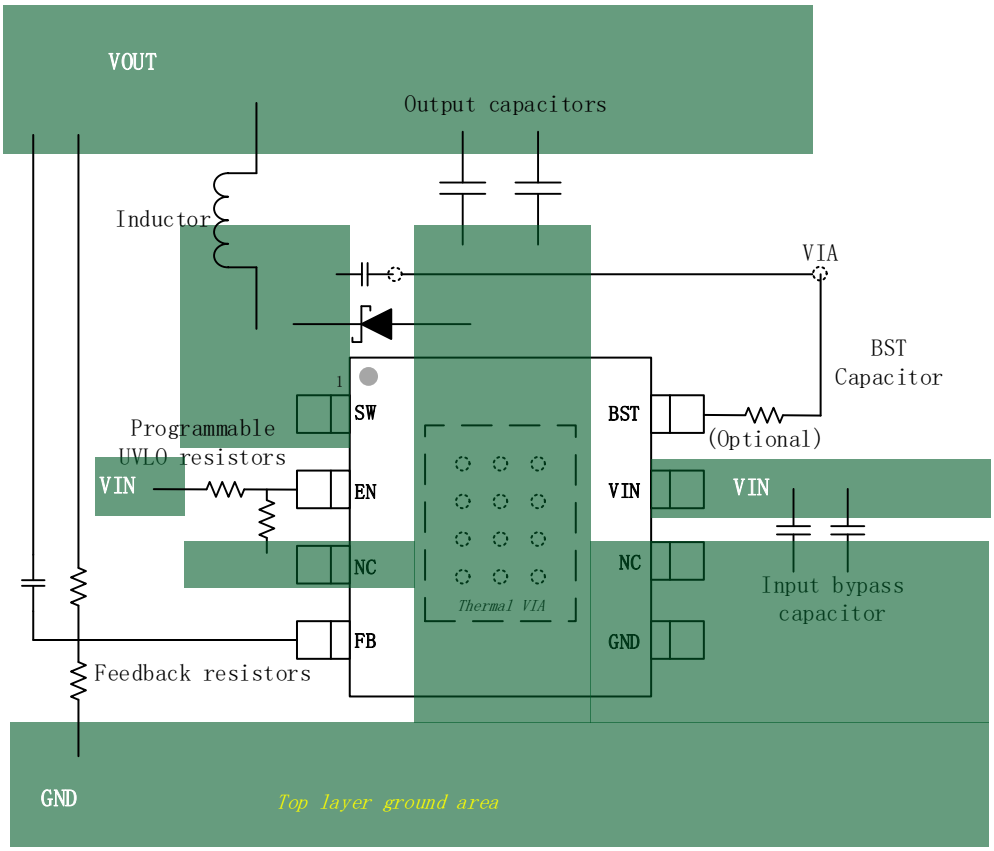
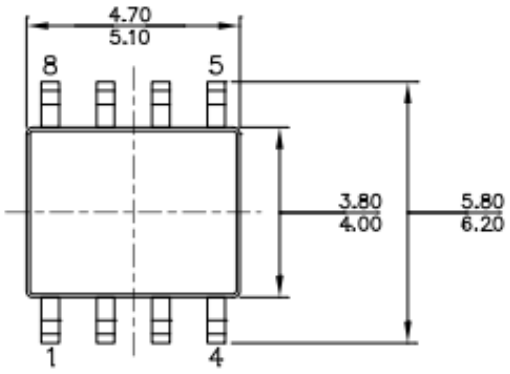
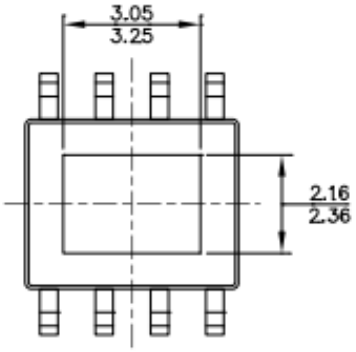


Figure 23. PCB Layout Example

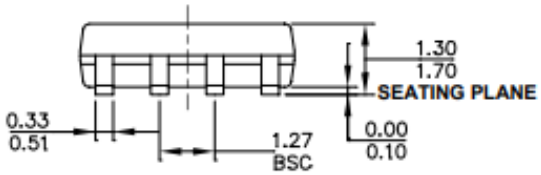
PACKAGE INFORMATION



TOP VIEW

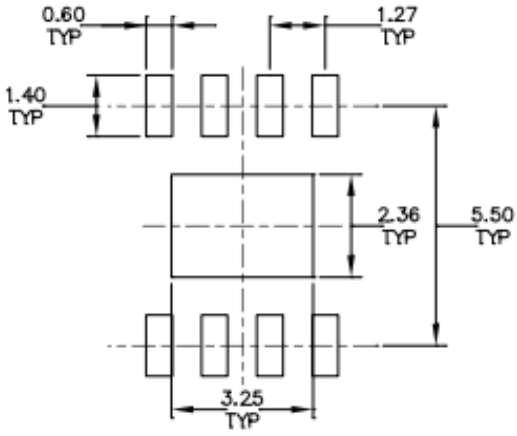


BOTTOM VIEW

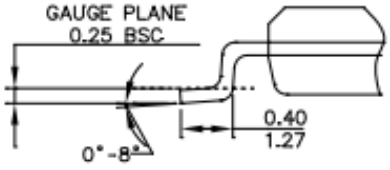


FRONT VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

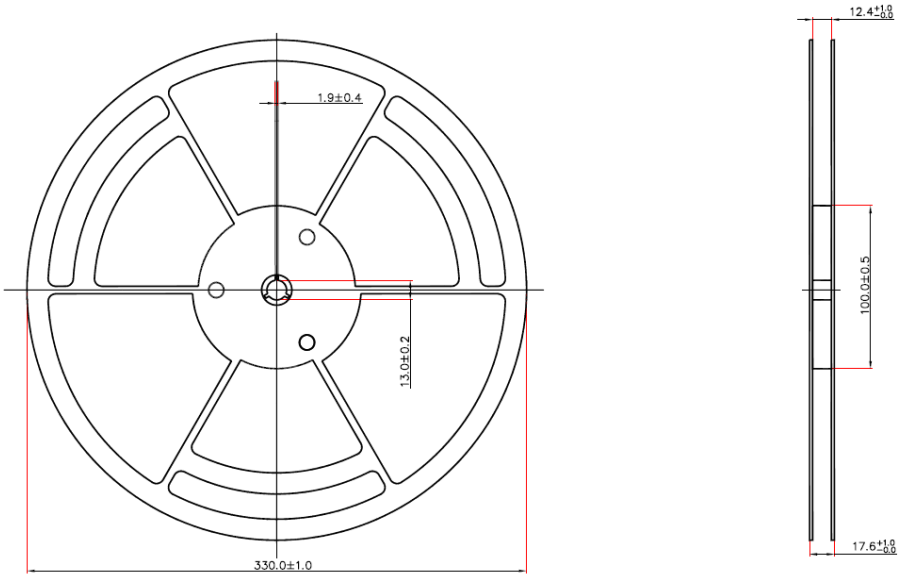


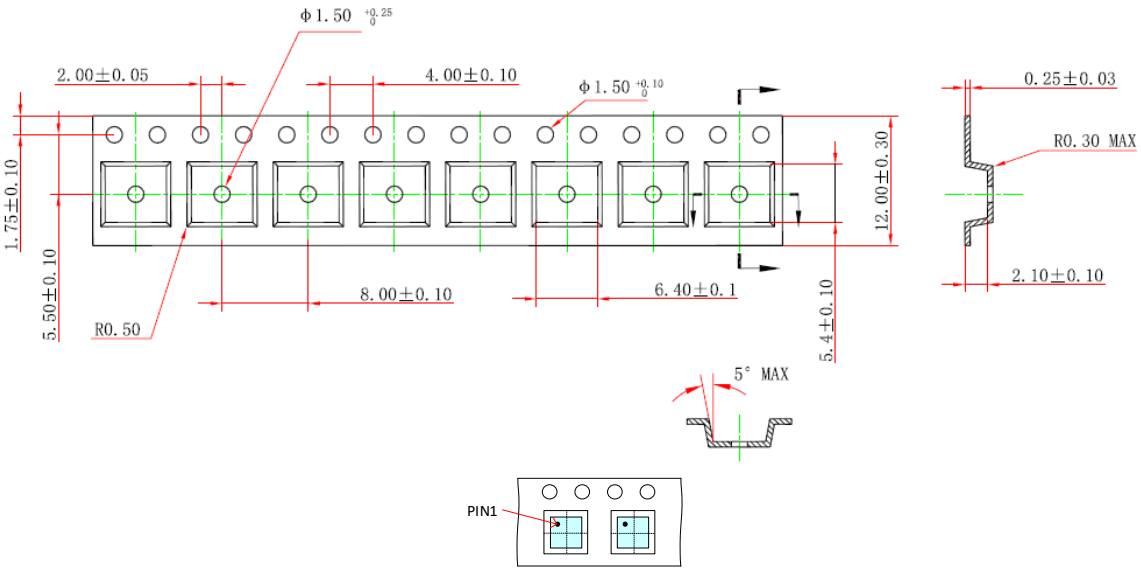
DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING REFERENCE TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION





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