3A, 24V, Synchronous Step-Down Converter

DESCRIPTION

The EUP3293 is a high frequency synchronous rectified step-down current mode converter with built-in power MOSFETs. It offers a very compact solution to achieve a 3A continuous output current with excellent load and line regulation over a wide input supply range from 4.5V to 24V. The EUP3293 has synchronous mode operation for higher efficiency over the output current load range. Current-mode operation provides fast transient response and eases loop stabilization. Full protection features include input under voltage lockout, input over voltage protection, output under voltage protection, over-current protection and thermal shutdown.

The EUP3293 requires a minimal number of readily-available standard external components, and is available in a space-saving 8-pin TSOT23 package.

FEATURES

- Wide Input Voltage Range: 4.5V to 24V
- 80mΩ/30mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Current Mode Control
- Fixed 500kHz Switching Frequency
- Synchronizes from a 200kHz-to-1MHz External Clock
- Power Saving Mode at Light Load
- Internal Soft-Start
- Power Good Indicator
- Over Current Protection and Hiccup
- Thermal Shutdown
- Input Under Voltage Lockout
- Available in an 8-pin TSOT23 package
- RoHS Compliant and Halogen-Free

APPLICATIONS

- Notebook Systems and I/O Power
- Digital Set-top Boxes
- LCD Monitors and TVs
- Distributed Power Systems

Typical Application Circuit

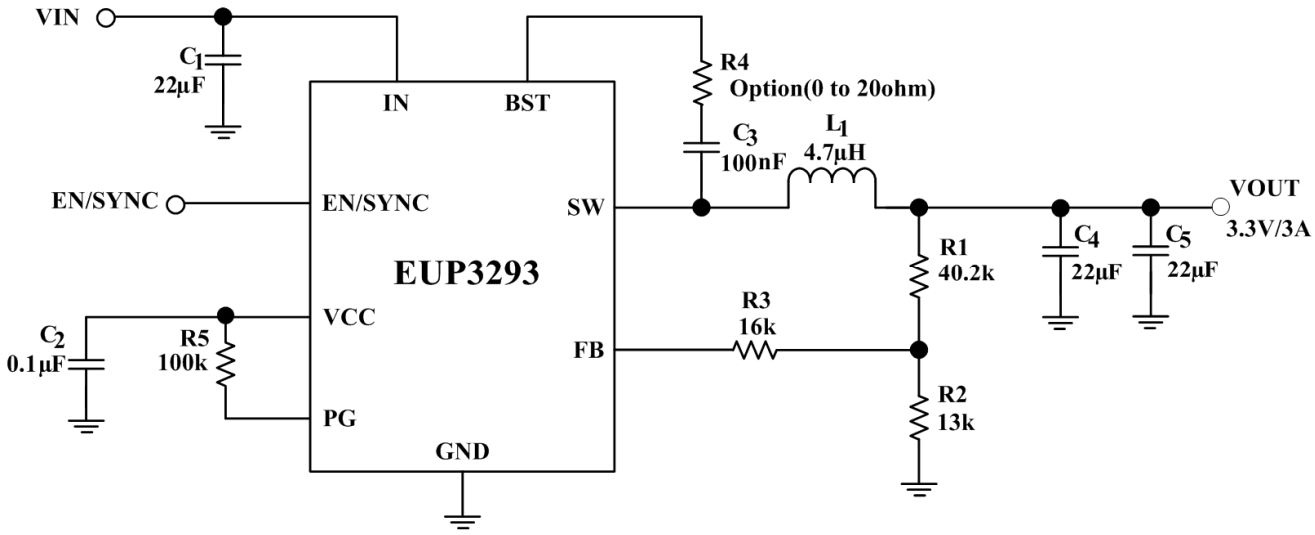
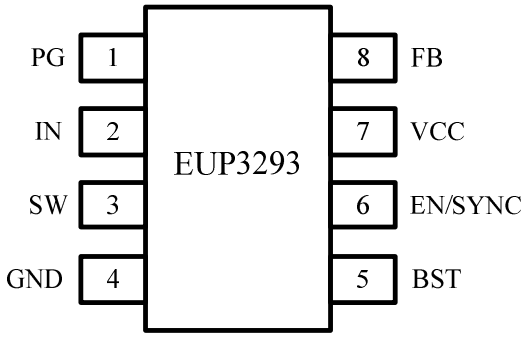


Figure1. Application Circuit

Pin Configurations

Package Type	Pin Configurations
TSOT23-8	(TOP VIEW) 

Pin Description

Pin	Pin Name	Description
1	PG	Power Good. The output of this pin is an open drain and goes high if the output voltage exceeds 90% of the nominal voltage.
2	IN	Supply Voltage Input. The EUP3293 operates from a 4.5V to 24V input rail. Requires C1 to decouple the input rail. Connect using a wide PCB trace.
3	SW	Switch Output. Connect with a wide PCB trace.
4	GND	System Ground. This pin is the reference ground of the regulated output voltage, and PCB layout requires special care. For best results, connect to GND with copper traces and vias.
5	BST	Bootstrap. Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
6	EN/SYNC	Enable/Synchronize. EN/SYNC high to enable the EUP3293. Apply an external clock to the EN/SYNC pin to change the switching frequency. For automatic startup, directly connect EN/SYNC to IN (or through a resistor).
7	VCC	Internal 5V LDO output. Connect a minimum of 0.1μF capacitor to ground.
8	FB	Feedback. Connect to an external resistor divider to set the output voltage.

Ordering Information

Order Number	Package Type	Marking	Quantity per Reel	Operating Temperature Range
EUP3293OIR1	TSOT23-8	xxxxx B900	3000	-40 °C to +85°C

EUP3293 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen-Free
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  O: TSOT23

Block Diagram

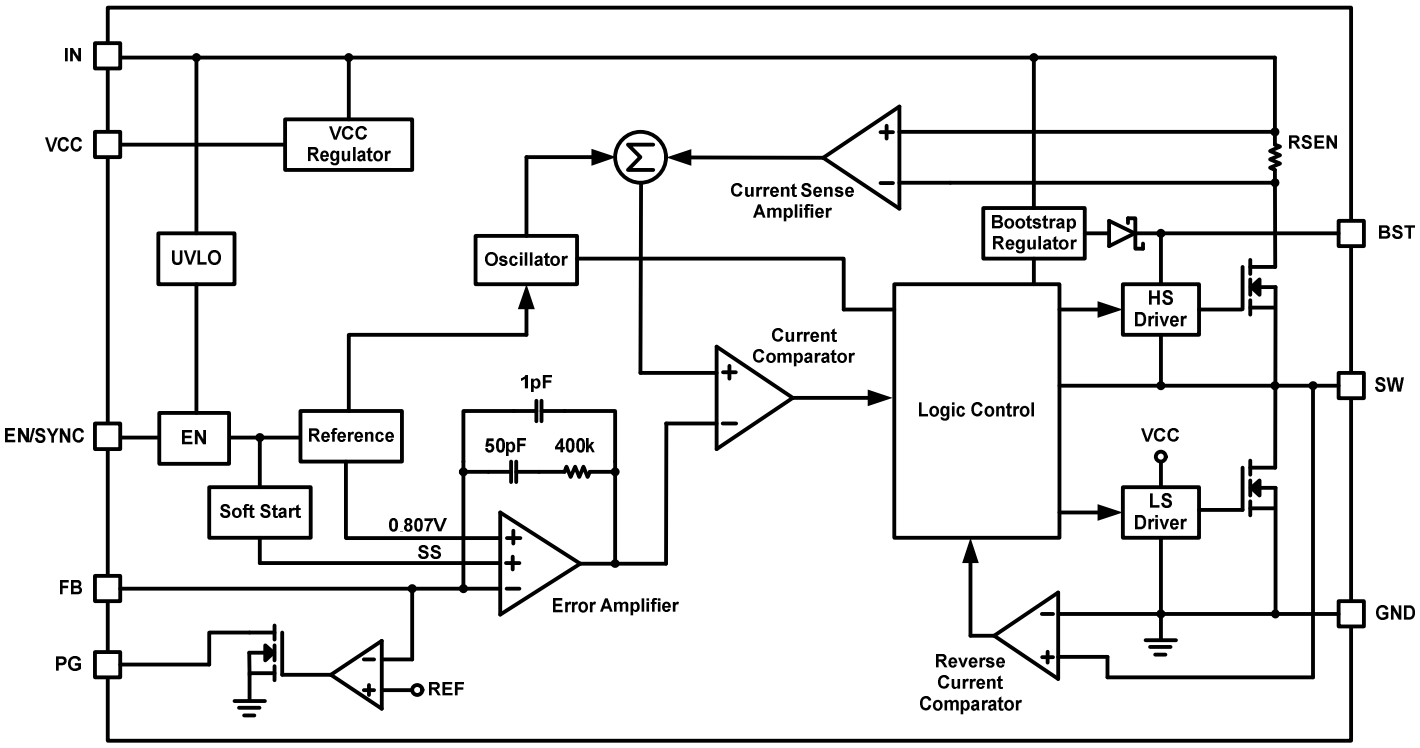


Figure2. Functional Block Diagram

Absolute Maximum Ratings(1)

- Input Voltage (V_{IN}) ---------- -0.3V to 26V
- Enable Voltage (V_{EN}) ---------- -0.3V to 26V
- Switch Voltage(V_{SW}) ---------- -0.3V to 26V
- Bootstrap Voltage(V_{BST}) ---------- V_{SW}-0.3V to V_{SW}+6V
- All Other Pins ---------- -0.3V to 6V
- Junction Temperature ---------- 150°C
- Storage Temperature ---------- -65°C to +150°C
- Lead Temp(Soldering, 10sec) ---------- 260°C
- Thermal Resistance θ_{JA} (TSOT23-8) ---------- 100°C/W

Recommend Operating Conditions(2)

- Supply Voltage (V_{IN}) ---------- 4.5V to 24V
- Ambient Operating Temperature ---------- -40°C to +85°C

Note(1):Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.
Note(2):The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

(V_{IN}=12V, T_A=+25°C, unless otherwise specified)

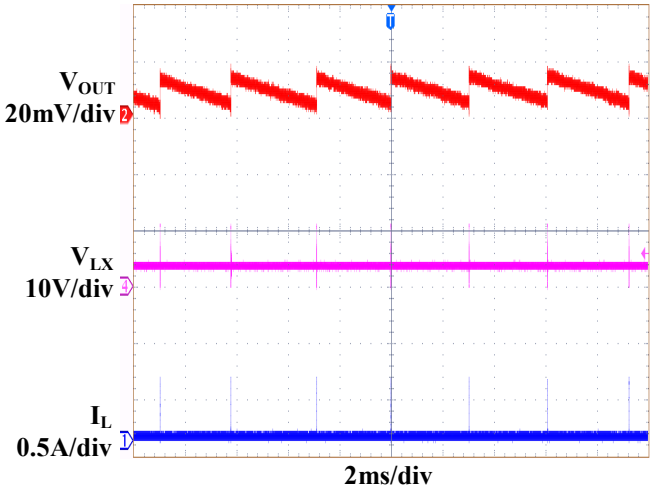
Symbol	Parameter	Conditions	EUP3293			Unit
			Min.	Typ.	Max.	
General Section						
V_{IN}	Input Voltage Range		4.5		24	V
V_{UVLO_RISING}	V_{IN} UVLO Rising Threshold	V_{IN} rising	3.6	3.8	4.0	V
$V_{UVLO\_FALLING}$	V_{IN} UVLO Falling Threshold	V_{IN} falling	3.2	3.4	3.6	V
V_{UVLO_HYS}	V_{IN} UVLO Threshold Hysteresis			400		mV
I_Q	Quiescent Current	V_{EN}=2V,V_{FB}=1V		140	200	μA
I_{SD}	Shutdown Current	V_{EN}=0V		4	10	μA
I_{LKG_SW}	Switch Leakage	V_{EN} = 0V, V_{SW} =12V			1	μA
V_{CC}	VCC Regulator			4.9		V
V_{FB}	Feedback Voltage		0.791	0.807	0.823	V
T_{SS}	Soft Start Time			1.2		ms
f_{SW}	Oscillator Frequency	V_{FB}=750mV	430	500	570	kHz
f_{FB}	Fold-Back Frequency	V_{FB}<400mV		125		kHz
D_{MAX}	Maximum Duty Cycle	V_{FB}=700mV, 500kHz	90	95		%
t_{ON_MIN}	Minimum On Time			150		ns
f_{SYNC}	Synchronous Frequency Range		0.2		1	MHz
V_{ENH}	Enable Threshold	EN Rising Threshold	1.2	1.42	1.6	V
V_{ENL}		EN Falling Threshold	1.1	1.22	1.4	V
R_{ON_HS}	High Side MOS on Resistance			80		mΩ
R_{ON_LS}	Low Side MOS on Resistance			30		mΩ
PG_{VTH_R}	PG Rising Threshold	As percentage of V_{FB}		90		%
PG_{VTH_F}	PG Falling Threshold	As percentage of V_{FB}		84		%
PG_{VTH_HYS}	PG Threshold Hysteresis	As percentage of V_{FB}		6		%
V_{PG}	PG Sink Current Capability	Sink 4mA		0.1	0.4	V
I_{LIMIT}	Current Limit	Under 40% Duty Cycle	4.2	5		A
T_{SD}	Thermal Shutdown Threshold			160		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			40		°C

Typical Operating Characteristics

T_A=25°C, V_{IN}=12V, V_{OUT}=3.3V, F_{SW}=500kHz, unless otherwise specified.

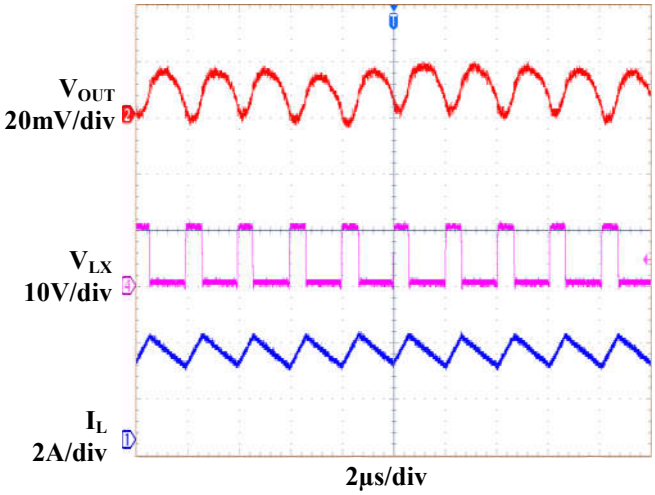
Steady State

V_{IN}=12V, V_{OUT}=3.3V, No load



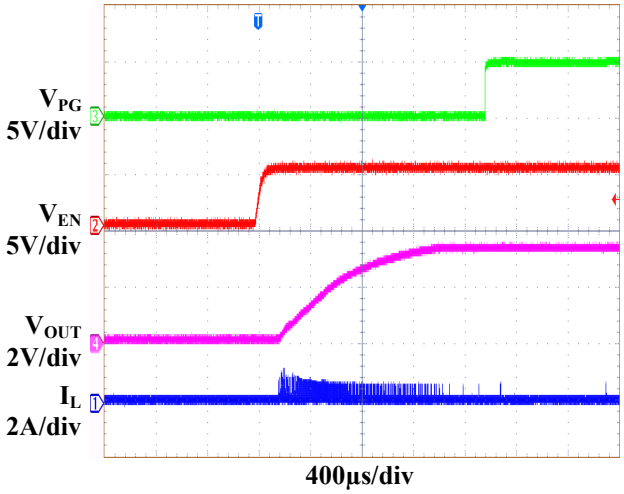
Steady State

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A



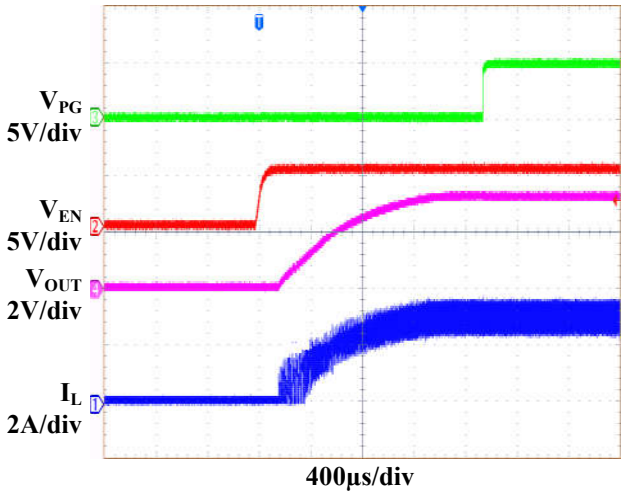
Startup through Enable

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A



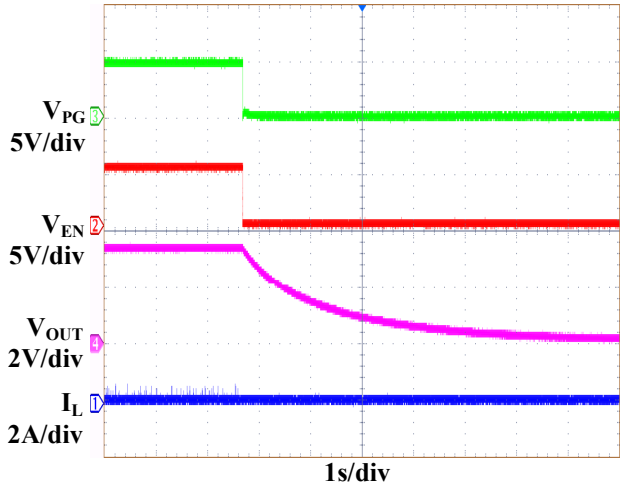
Startup through Enable

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A



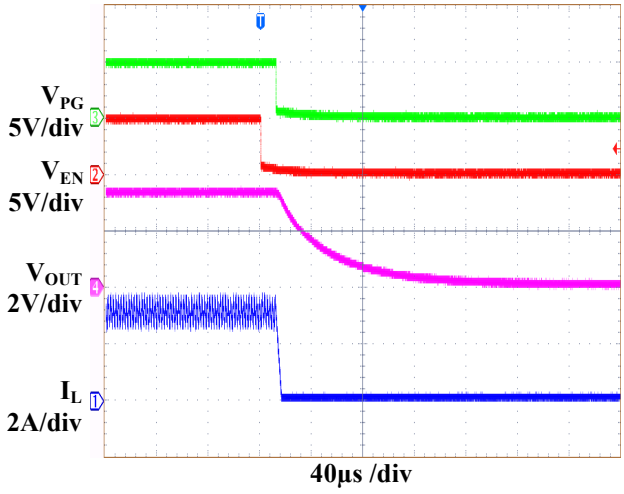
Shutdown through Enable

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A



Shutdown through Enable

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A

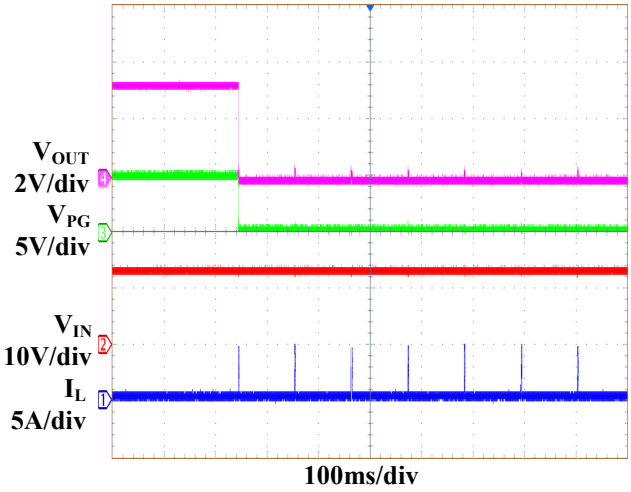


Typical Operating Characteristics

T_A=25°C, V_{IN}=12V, V_{OUT}=3.3V, F_{SW}=500kHz, unless otherwise specified.

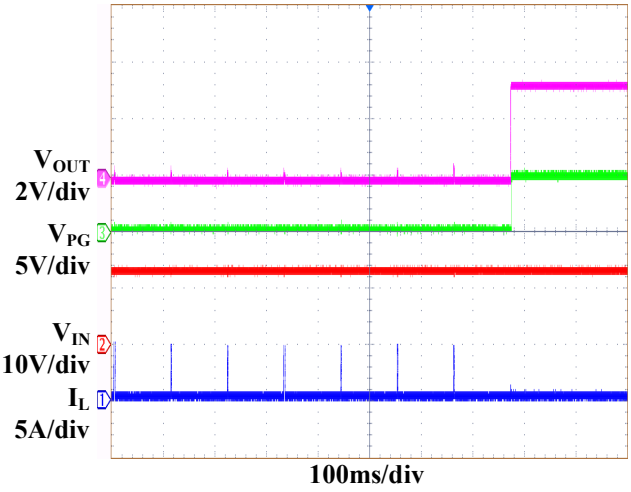
Short Circuit

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A



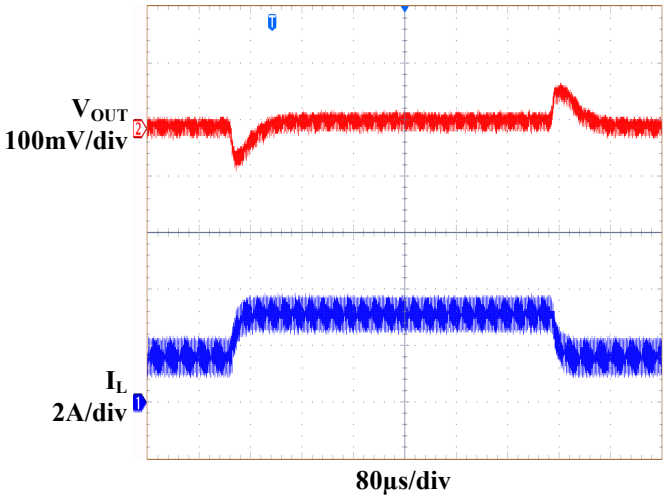
Short Circuit Recovery

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A



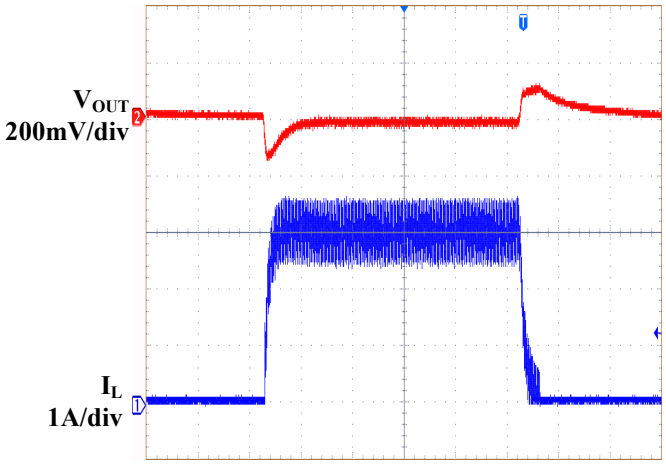
Load Transient Response

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=1.5A to 3A

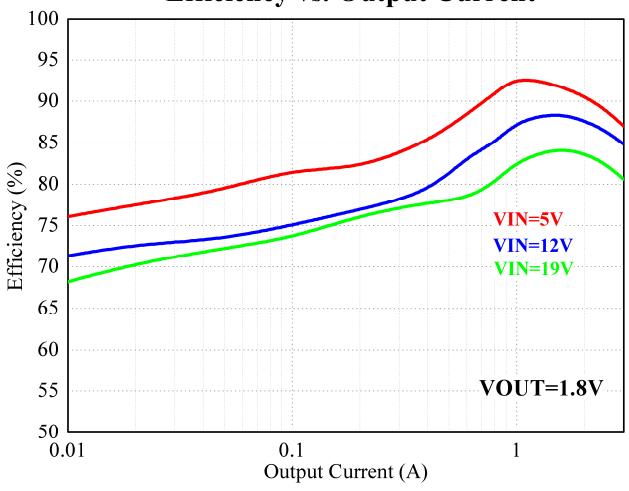


Load Transient Response

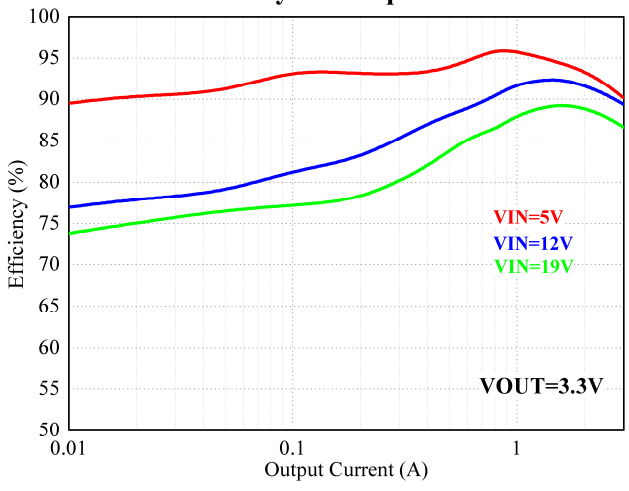
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A to 3A



Efficiency vs. Output Current

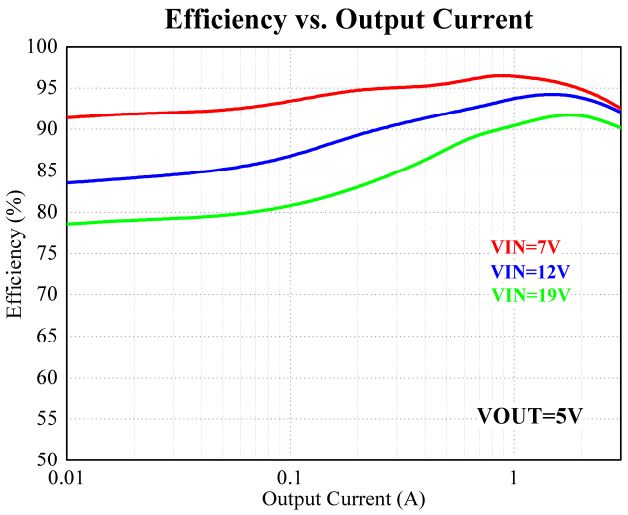


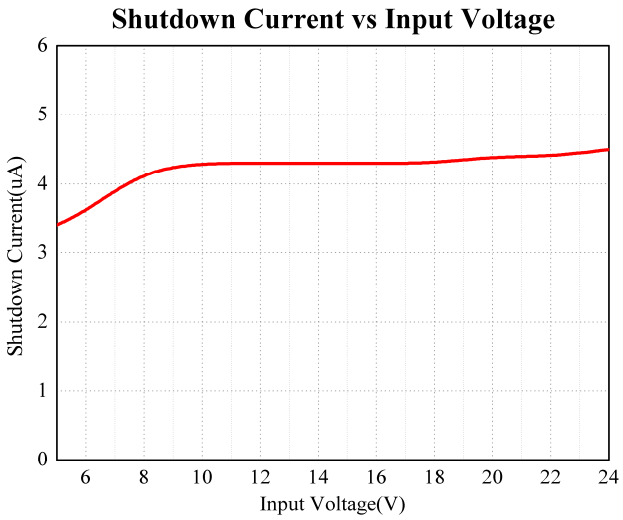
Efficiency vs. Output Current

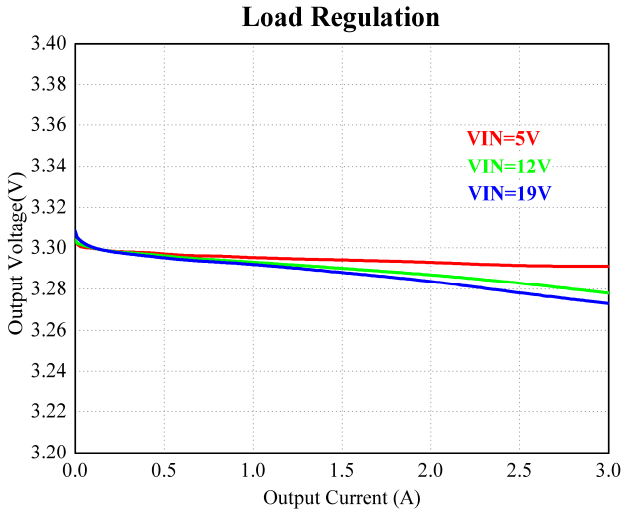


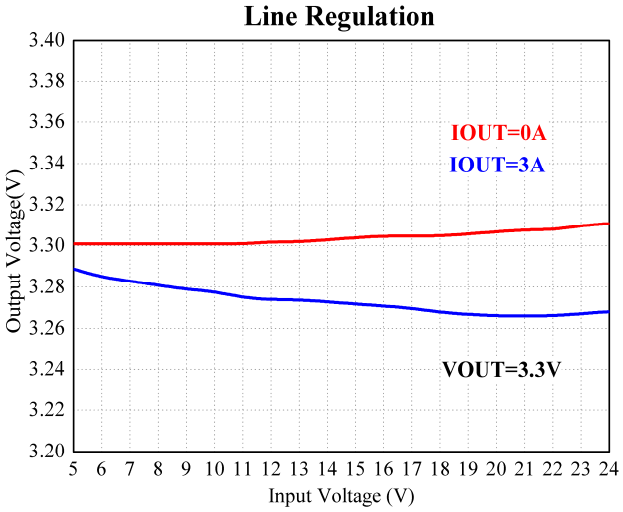
Typical Operating Characteristics

T_A=25°C, V_{IN}=12V, V_{OUT}=3.3V, F_{SW}=500kHz, unless otherwise specified.









Functional Description

The EUP3293 is a high-frequency synchronous rectified step-down current mode converter with 4.5V to 24V input power supply. The device can provide up to 3A continuous current to the output.

Internal Regulator

The internal regulator generates 5V power and drives internal circuit. When VIN exceeds 5V, the output of the regulator is in full regulation. When VIN is less than 5V, the output decreases. A minimum 0.1μF ceramic capacitor is required between VCC and GND.

Enable/SYNC Control

The EN pin is the chip enable input. Pulling the EN pin low (<0.5V) will shutdown the output voltage. During shutdown mode, the EUP3293's shutdown current drops to about 4μA. Driving the EN pin high (>1.6V) will turn on the device.

The internal oscillator runs at 500 kHz (typ.) when the EN/SYNC pin is at logic-high level (>1.6V). If the EN pin is pulled to low-level over 13μs, the IC will shut down. The EUP3293 can be synchronized with an external clock ranging from 200 kHz to 1MHz applied to the EN/SYNC pin.

Soft-Start

The EUP3293 has internal soft start feature to minimize the inrush supply current and the output overshoot at initial startup. When the EUP3293 starts up, the internal reference voltage which is compared with V_{FB} ramps up gradually, so the output voltage ramps up as well. The typical soft-start time is 1.2ms.

Over Current Protection and Hiccup

The EUP3293 features cycle-by-cycle current limit protection and prevents the device from the damage in output short circuit or over current. The EUP3293 enters hiccup mode to periodically restart the part when V_{FB} below 0.42V (tpy.). This protection greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator. The EUP3293 exits the hiccup mode once the over current condition is removed.

Under Voltage Lockout (UVLO)

The EUP3293 includes an input Under Voltage Lockout Protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (3.8V), the converter will power up. If the input voltage falls below the UVLO falling threshold voltage (3.4V) during normal operation, the device stops switching. The UVLO rising and falling threshold voltage includes a hysteresis to prevent noise caused reset.

Power Good Indicator

The EUP3293 features an open-drain power-good output (PG) to monitor the output voltage status. Connect PG to VCC with a resistor. The power-good function is activated after soft-start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above typically 90% of the reference voltage, the PG pin will be in high impedance. When V_{FB} goes below typically 84% of the reference voltage, the PG pin will be pulled low.

Bootstrap Voltage Regulator

An external bootstrap capacitor and an option resistor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side MOSFET is off and the low-side MOSFET turns on. The recommended value of the BOOT capacitor is 0.1μF, resistor is 0~20Ω.

Thermal Shutdown

The EUP3293 stops switching when its junction temperature exceeds 160°C and resumes when the temperature has dropped by 40°C to protect the device.

Application Information

Setting the Output Voltage

The output voltage is set through a resistive voltage divider and can be expressed by the equation as follows

$$V_{OUT} = 0.807 \times \frac{R1 + R2}{R2}$$

The T-type network is highly recommended when VOUT is low.

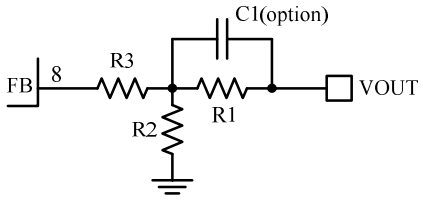


Figure3. Output Voltage Setting

Table 1 lists the recommended resistors value for common output voltages.

Table1. Recommended Resistors Value

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	L1 (μH)
1.0	20.5	84.5	82	2.2
1.8	40.2	32.4	33	3.3
2.5	40.2	19.1	33	3.3
3.3	40.2	13	16	4.7
5.0	40.2	7.68	16	4.7

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will in turn result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and lower saturation current. A good rule for determining inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum switch current limit. So, make sure that the peak inductor current is

below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current. Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current, the choice of which style inductor to use mainly depends on the price vs size requirements and any EMI constraints. In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 5A. Because of the maximum I_{LP} limited by device, the maximum output current that the EUP3293 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors. Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{CIN} = I_{LOAD}/2$. For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C_{IN} \times F_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C_{IN} is the input capacitance. For this example design, a ceramic capacitor with at least a 25V voltage rating is required to support the maximum input voltage.

Output Capacitor

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance. The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by equation below:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C_{OUT} is the output capacitance value and F_{SW} is the switching frequency. Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

Layout Considerations

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance. When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3293.

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
2. The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The feedback components must be connected as close as possible between the FB and GND.
5. Keep the switching node, SW, away from the sensitive FB node.
6. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
7. PG resistors and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
8. Route BST capacitor trace on the other layer than top layer to provide wide path for topside ground.

An example of PCB layout guide is shown in the figure4 below for reference.

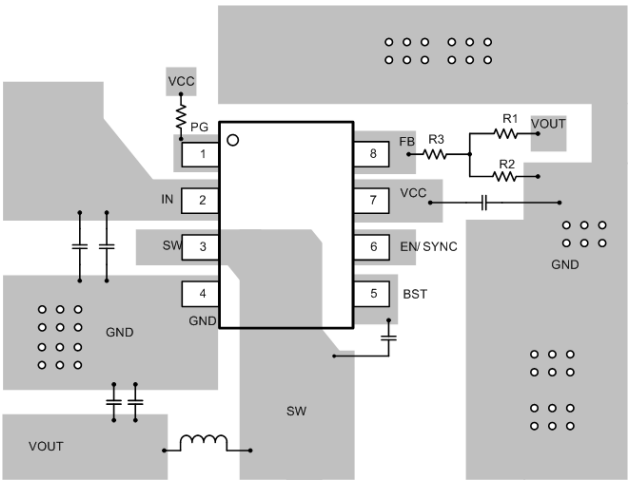
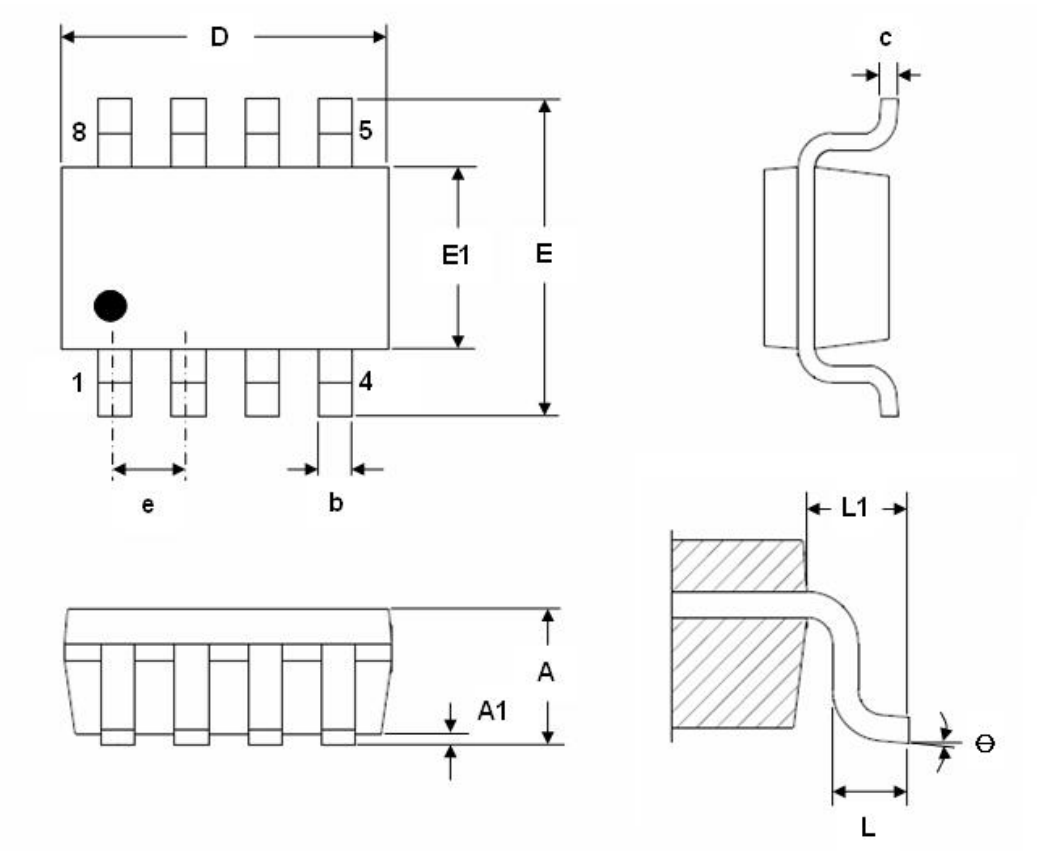


Figure4. PCB Layout Example

Packaging Information

TSOT23-8



SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.70	-	1.00	0.028	-	0.039
A1	0.00	-	0.10	0.000	-	0.004
b	0.20	-	0.50	0.008	-	0.020
c	0.09	-	0.20	0.004	-	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
e	0.65 REF			0.026 REF		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
Θ	0°	4°	8°	0°	4°	8°