Applications Note: AN_SY8063

High Efficiency 1 MHz, 3.5A Synchronous Step Down Regulator

Preliminary Specification

General Description

The SY8063 is a high-efficiency 1 MHz synchronous step-down DC-DC regulator IC capable of delivering up to 3.5A output current. The SY8063 operates over a wide input voltage range from 2.7V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with 1MHz switching frequency.

Ordering Information

SY8063□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Note
SY8063DBC	DFN3x3-10	3.5A

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom): 85/65m<
- 2.7-5.5V input voltage range
- 1 MHz switching frequency minimizes the external components
- Internal softstart limits the inrush current
- 100% dropout operation
- Power good indicator
- RoHS Compliant and Halogen Free
- Compact package: DFN3x3-10

Applications

- Set Top Box
- LCD TV
- Access Point Router
- Mini-notebook PC
- Net PC

Typical Application Circuit

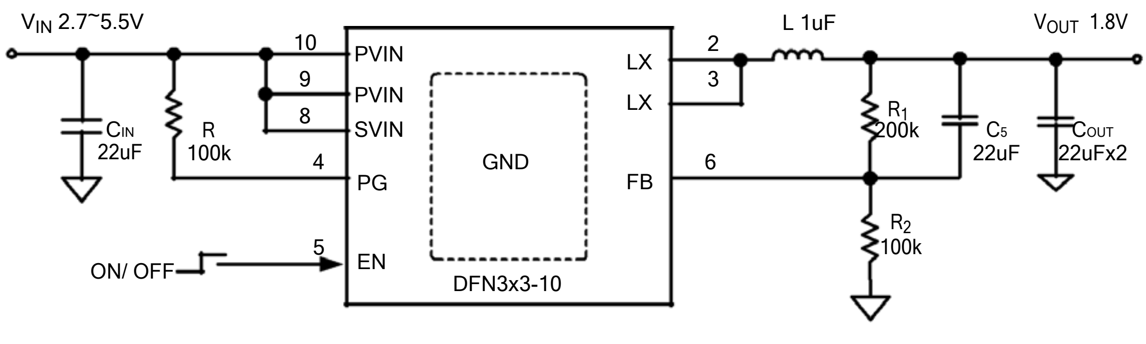
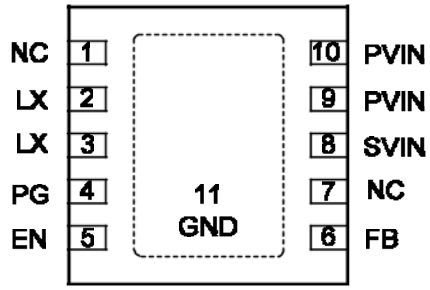


Figure 1

Pinout (top view)



Top Mark: EC*xyz* (device code: EC, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
EN	5	Enable control. Pull high to turn on. Default pull down by internal resistor.
GND	11	Ground pin
LX	2,3	Inductor pin. Connect this pin to the switching node of inductor
SVIN	8	Signal Power Input pin.
PVIN	9,10	Power Input Pin.
FB	6	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: Vout=0.6*(1+R1/R2)
PG	4	Power good indicator.
NC	1,7	No connections.

Absolute Maximum Ratings (Note 1)

Supply Input Voltage -- 6.5V
Enable, FB Voltage-- V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25°C DFN3x3 -- 2.6W
Package Thermal Resistance (Note 2)
θ_{JA} -- 38°C/W
θ_{JC} -- 8°C/W
Junction Temperature Range -- 125°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range -- -65°C to 150°C
ESD Susceptibility (Note 3)
HBM (Human Body Mode) -- 2kV
MM (Machine Mode) --- 200V
Dynamic LX voltage in 50ns duration --- IN+3V to GND-4V

Recommended Operating Conditions (Note 3)

Supply Input Voltage -- 2.7V to 5.5V
Junction Temperature Range --- -40°C to 125°C
Ambient Temperature Range --- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 2.5V, L = 2.2uH, C_{OUT} = 10uF, T_A = 25°C, I_{MAX} = 1A unless otherwise specified)

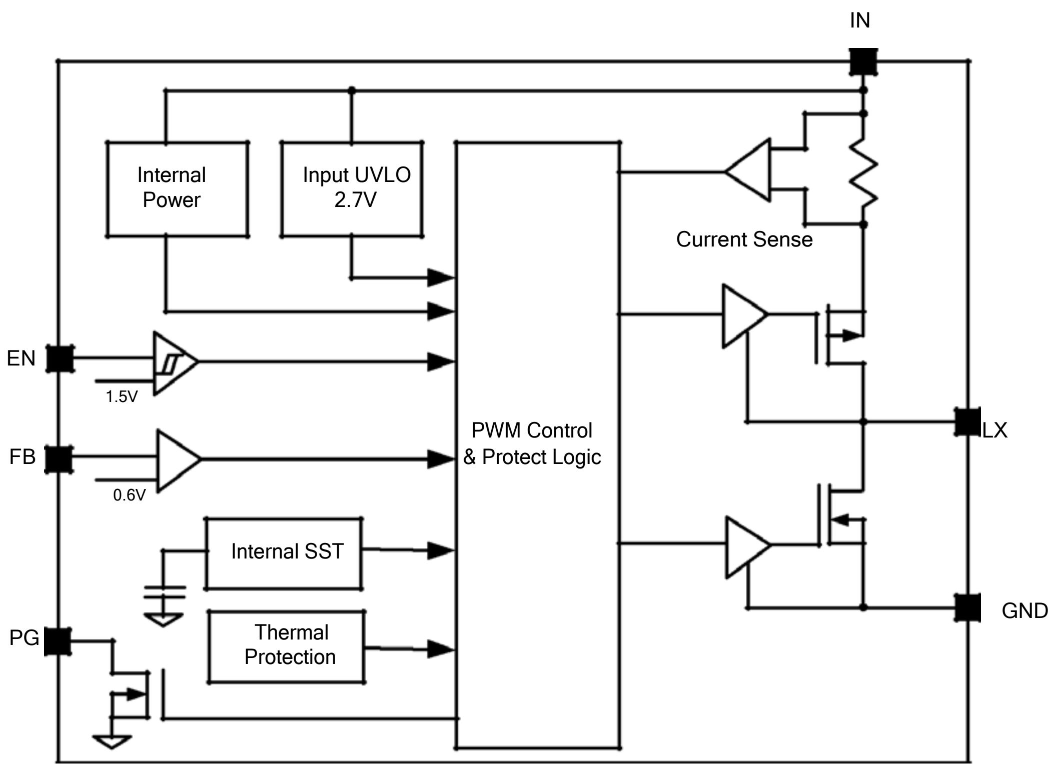
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		5.5	V
Shutdown Current	I_{SHDN}	EN=0		0.1	1	LA
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF} · 105%		80		LA
Feedback Reference Voltage	V_{REF}	0.6V, ± 1.5%	0.591	0.6	0.609	V
FB Input Current	I_{FB}	$V_{FB}=V_{IN}$	-50		50	nA
PFET RON	$R_{DS(ON),P}$			85		m<
NFET RON	$R_{DS(ON),N}$			65		m<
PFET Current Limit	I_{LIM}		4			A
EN rising threshold	V_{ENH}		1.5			V
EN falling threshold	V_{ENL}				0.4	V
Input UVLO threshold	V_{UVLO}				2.7	V
UVLO hysteresis	V_{HYS}			0.2		V
Oscillator Frequency	F_{OSC}	I_{OUT}=100mA		1		MHz
		V_{FB}=0		0.25		
Min ON Time				50		ns
Max Duty Cycle			100			%
Thermal Shutdown Temperature	T_{SD}			150		°C
Internal Soft Start Time	T_{SS}			1		ms
Power Good rising threshold				0.55		V
Power Good hysteresis				25		mV

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of DFN3X3-10 packages is the case position for θ_{JC} measurement.Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

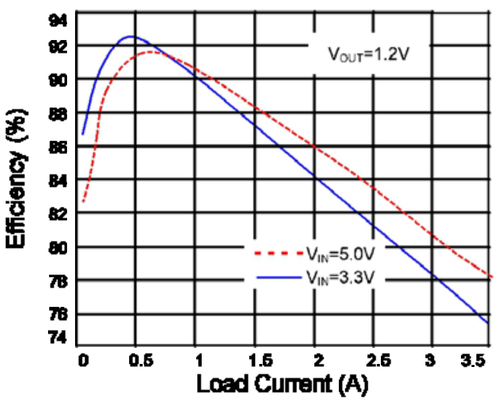
Note 3: The device is not guaranteed to function outside its operating conditions.

Function Block

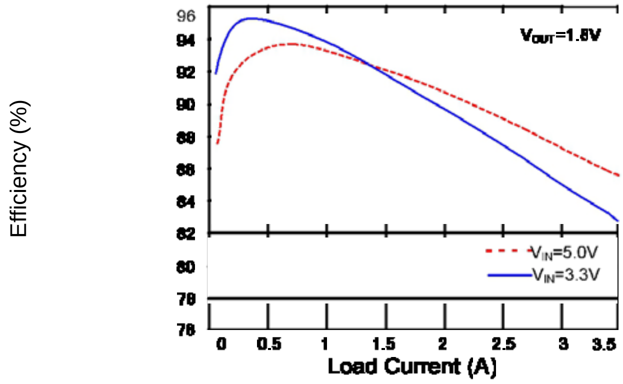


Typical Performance Characteristics

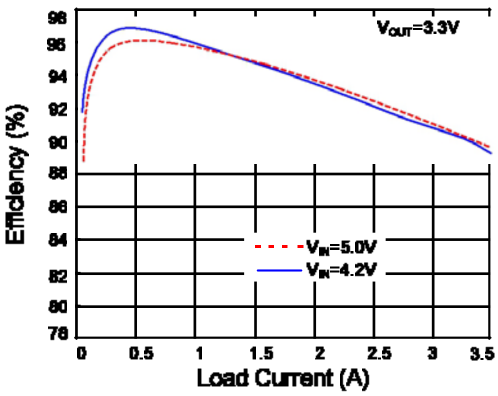
Efficiency vs. Load Current



Efficiency vs. Load Current

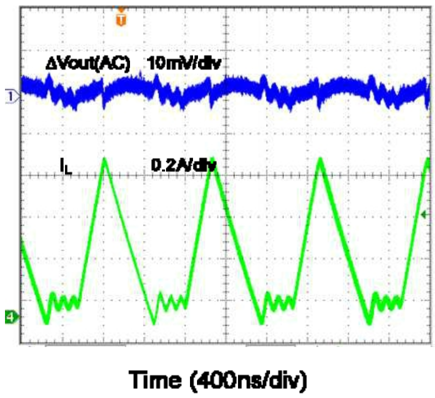


Efficiency vs. Load Current



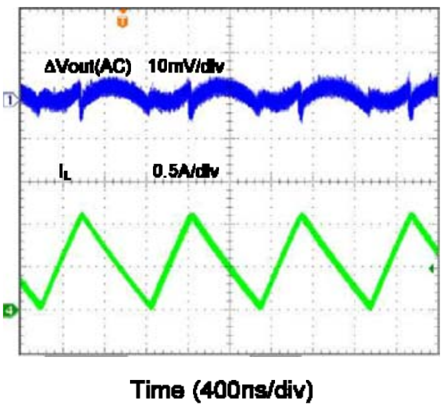
Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.2A)



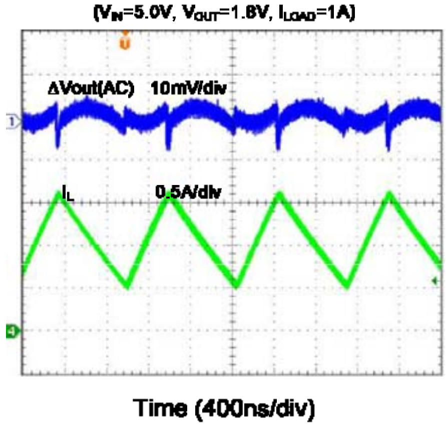
Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.5A)



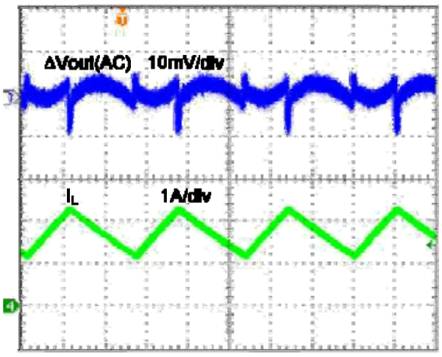
Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=1A)



Output Ripple

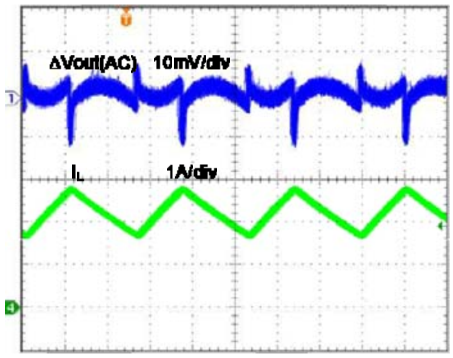
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=1.5A)



Time (400ns/div)

Output Ripple

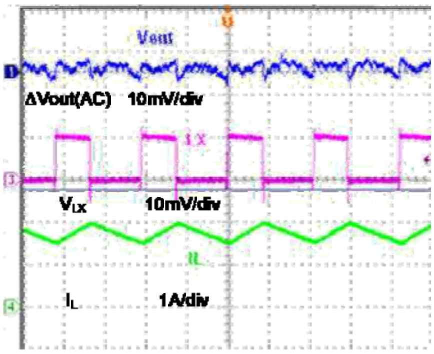
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=2A)



Time (400ns/div)

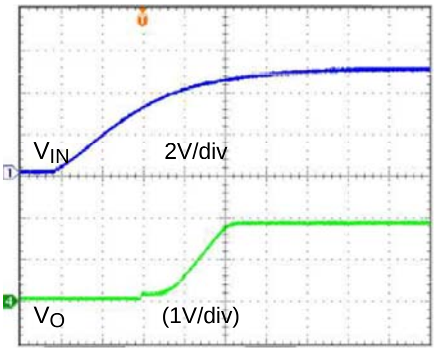
Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=2A)



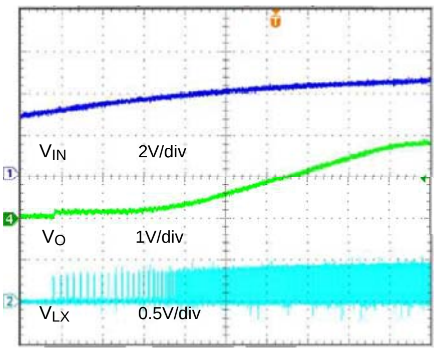
Time (400ns/div)

Soft Start (V_O)



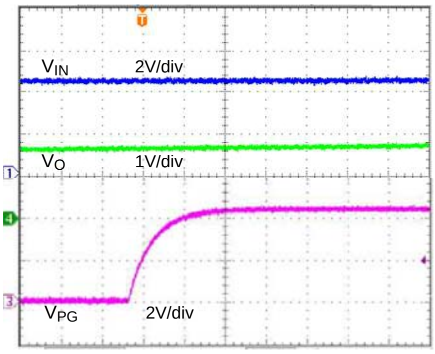
Time (400us/div)

Soft Start (V_{LX})



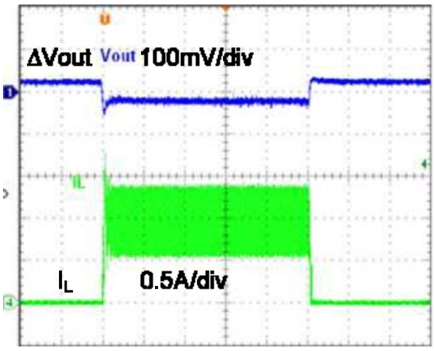
Time (100us/div)

Soft Start (V_{PG})



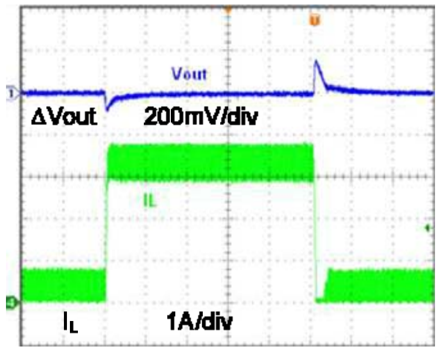
Time (4us/div)

Load Transient
V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=0-1.2A



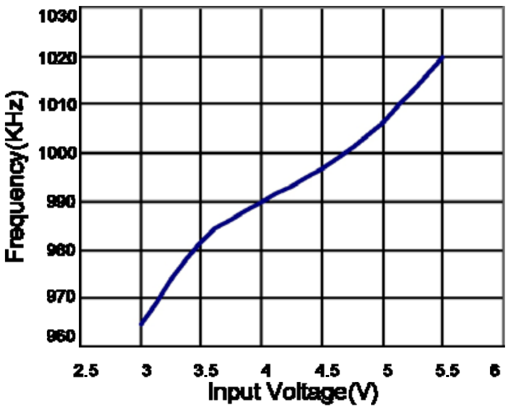
Time (40us/div)

Load Transient
V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=0.35-3.5A

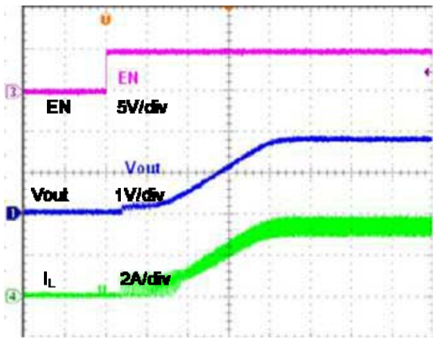


Time (40us/div)

Oscillator Frequency vs V_{IN}

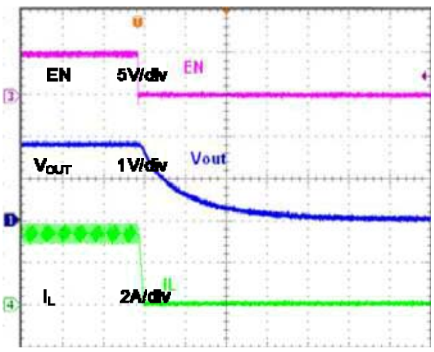


Startup
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=3.5A)



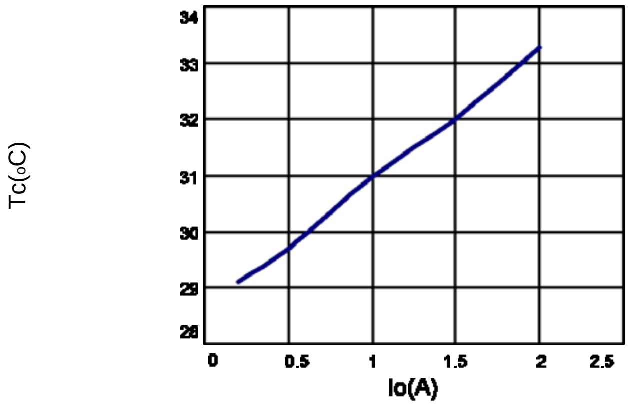
Time (200us/div)

Shutdown
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=3.5A)



Time (20us/div)

Case Temperature vs Output Current
(V_{IN}=5V,Vo=1.8V,Ta=27℃)



Operation

SY8063 is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low Rdson power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

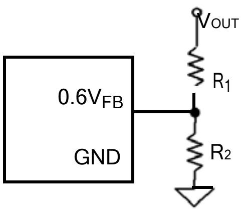
SY8063 will sense the output voltage conditions for the fault protection. If the DC output voltage is about 3% over the regulation level, both switches will turn off and remain in this OFF state. If the DC output votlage is below 33% of the regulation level, the internal softstart node is discharged and the error amplifier output is reset to minimum. Then the part will restart. When the output voltage is below 33% of the regulation, the frequency is folded back to 25% of the normal frequency and the current limit is decreased to 60% of the normal current limit to prevent the inductor current runaway and to reduce the power dissipation within the IC under true short circuit conditions.

Applications Information

Because of the high integration in the SY8063 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor CIN, output capacitor COUT, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2: Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10k and 1M is highly recommended for both resistors. If Vout is 1.8V, R1=100k is chosen, then R2 can be calculated to be 50k.:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input capacitor C_{IN}:

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \bullet \sqrt{D(1-D)}$$

This formula has a maximum at VIN=2VOUT condition, where ICIN_RMS=IOUT/2. This simple worst-case condition is commonly used for DC/DC design.

With the maximum load current at 3.5A. A typical X5R or better grade ceramic capacitor with 6.3V rating and greater than two pc s 22uF capacitance can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins

Output capacitor COUT:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6V rating and greater than 40uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and Iout,max is the maximum load current.

The SY8063 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is

desirable to choose an inductor with DCR<20mohm to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutmode, the SY8036 shutdown current drops to lower than 0.1uA. Driving the EN pin high (>1.5V) will turn on the IC again.

Soft-start

The SY8063 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC start-up. The typical soft-start time is 1ms.

PG (Power Good):

The power good is an open-drain output. Connect an above 100k pull up resistor to VIN to obtain an output voltage. The power good will output high immediately after the output voltage within 90% of normal putput voltage.

Load Transient Considerations:

The SY8063 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF~220pF ceramic capacitor in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Layout Design:

The layout design of SY8063 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: CIN, L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. The center pad of SY8063 is used as the GND, so it is desirable to make a ground plane layer on a multi-layer board. Resonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) CIN must be close to Pins IN and GND. The loop area formed by CIN and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a LiIon battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

Design Specifications

Input Voltage (V)	Output Current (A)	Output Voltage (V)	Test conditions
2.7~5.5V	0~3.5A	1.8V	K close

EVB Schematic

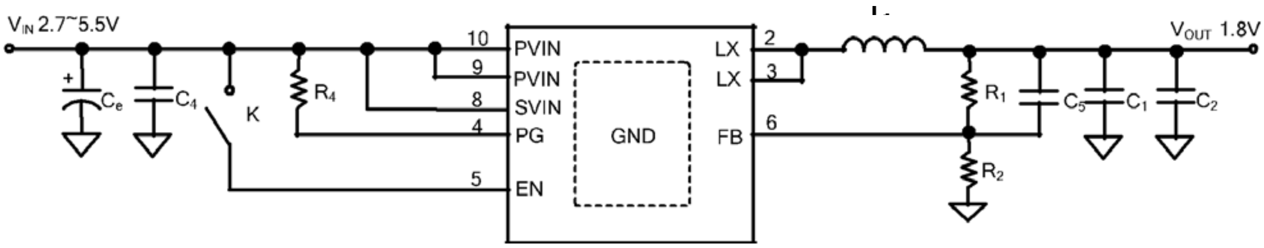


Figure 1. Schematic Diagram

Quick Start Guide (Refer to Figure 3)

1. Connect the output load to Vout and GND output connectors. Preset the load current to between 0A and 3.5A.
2. Preset the input supply to a voltage between 2.7V and 5.5V. Turn the supply off. Connect the input supply to V_{IN} and GND input connectors.
3. Turn on the input supply and measure the output voltage.

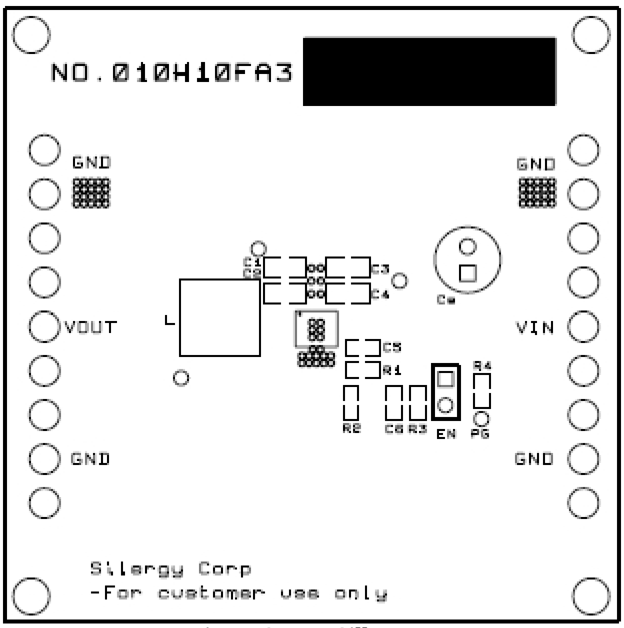
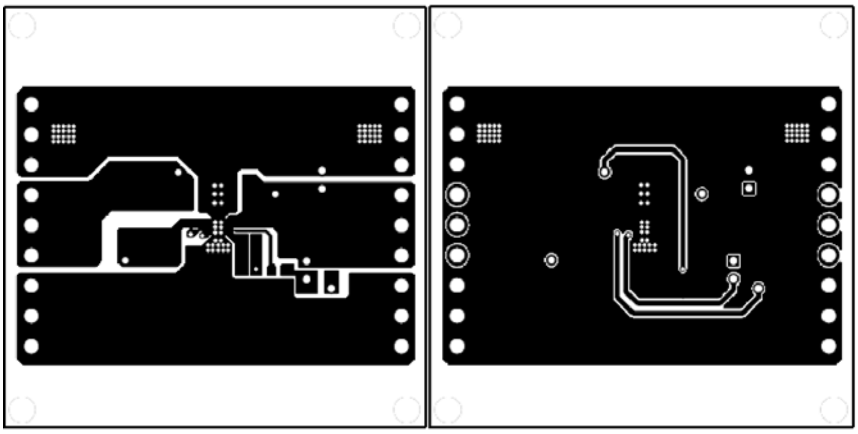


Figure 3. Top Silkscreen

PCB Layout



(a) (b)

Figure 4. PCB Layout Plots: (a) top layer, (b) bottom layer

BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	3.5A, 1MHz Sync Buck (DFN3x3-10)		
L_1	1uH/13A Inductor	SPM6530T-1R0M120	TDK
Ce	100uF/16V(electrolytic capacitor)		
C_1, C_2, C_4	22uF/6.3V, 0805, X5R	C2012X5R0J226M	TDK
C_5	22pF/50V, 0603, COG		
R_1	200k<, 1%, 0603		
R_2	100k<, 1%, 0603		
R_4	100k<, 0603		

Output voltage ripple test

A proper output ripple measurement should be done according to Figure 5 setup. Output voltage ripple should be measured across the output ceramic cap near the IC.

1. Remove the ground clip and head of the probe. Wind thin wires around the ground ring of the probe. Solder the end of the ground ring wire to the negative node of the C_{OUT}. Touch the probe tip to the positive node of the C_{OUT}. Refer to Figure 5.
2. Minimize the loop formed by C_{OUT} terminals, probe tip and ground ring.
3. Change the probing direction to decouple the electromagnetic noise generated from the nearby buck inductor (Refer to Figure 5).

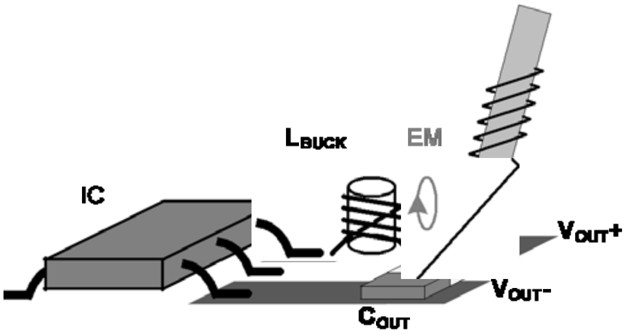
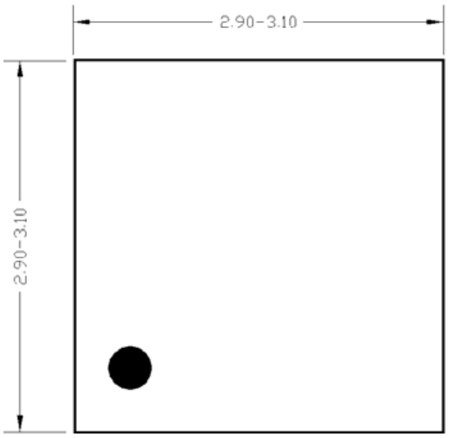
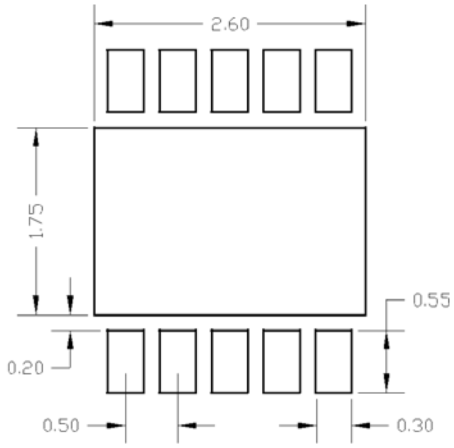


Figure 5. Recommended way to measure the output voltage ripple

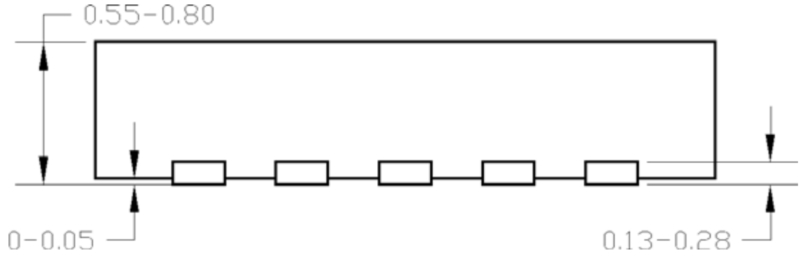
DFN3X3-10 Package outline



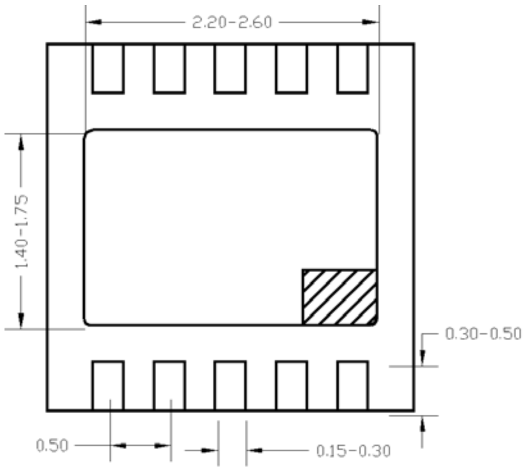
Top View

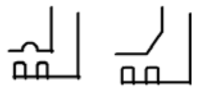


PCB layout (recommended)



Side View





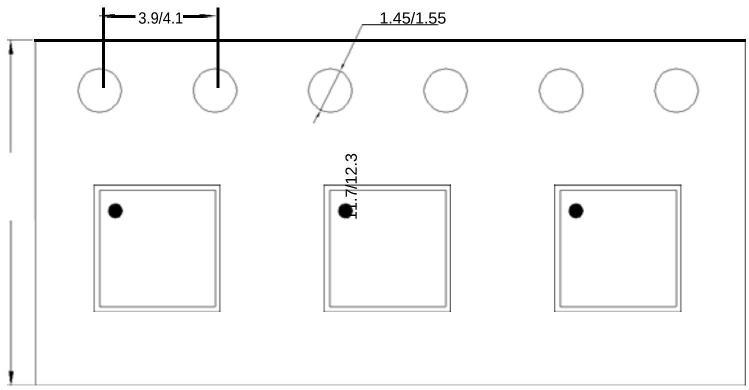
Detail A
Pin1 identifier: two options

Bottom View

Notes: All dimensions are in millimeters and exclude mold flash & metal burr.

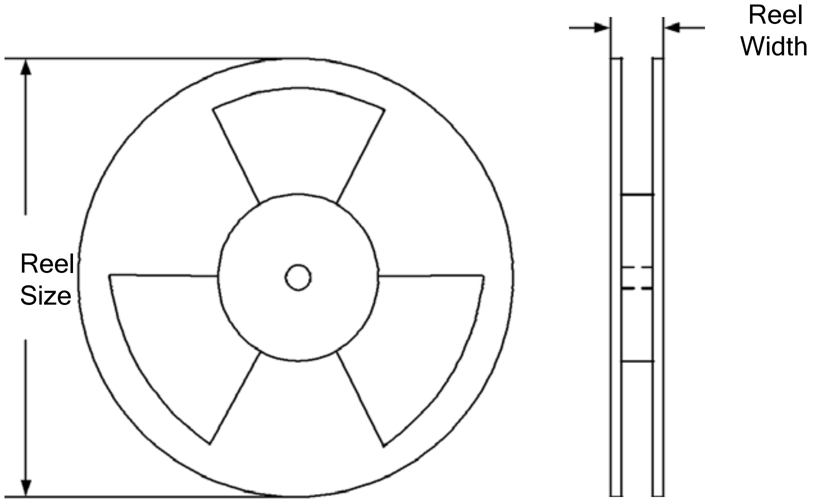
Taping & Reel Specification

1. DFN3x3-10 taping orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	10	8	13"	12.4	400	400	5000

3. Others: NA