

High Efficiency Fast Response, 6A, 24V Input Synchronous Step Down Regulator

General Description

The SY8386A develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A current over a wide input voltage range of 4.5V to 24V.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

Internal 38mΩ power and 19mΩ synchronous rectifier switches provide excellent efficiency over a range of applications, especially for low output voltages and low duty cycles. The SY8386A also integrates a bypass switch which allows the IC to be powered by external DC source. Cycle-by-cycle current limit, input under voltage lock-out, internal soft-start, output under voltage protection and over voltage protection and thermal shutdown provide safe operation in all operating conditions. The SY8386A is available in a compact QFN2.5×2.5-16 package.

Ordering Information

SY8386 □(□)□□
 □ Temperature Code
 □ Package Code
 □ Optional Spec Code

Ordering Number	Package type	Note
SY8386ARHC	QFN2.5×2.5-16	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 38/19 mΩ
- Wide Input Voltage Range: 4.5~24V
- Integrated Bypass Switch: 1.2Ω
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 600kHz
- Adjustable Output Voltage Application
- 6A Output Current Capability
- $\pm 1\%$ Internal Reference Voltage
- PFM/FCCM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Discharge Function
- Cycle-by-cycle Valley and Peak Current Limit Protection
- Programmable Valley Current Limit Threshold by ILMT Pin
- Hic-cup Mode Output Under Voltage Protection
- Auto-recovery Mode Output Over Voltage Protection
- Auto-recovery Mode Over Temperature Protection
- Input UVLO
- RoHS Compliant and Halogen Free
- Compact Package: QFN2.5×2.5-16

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

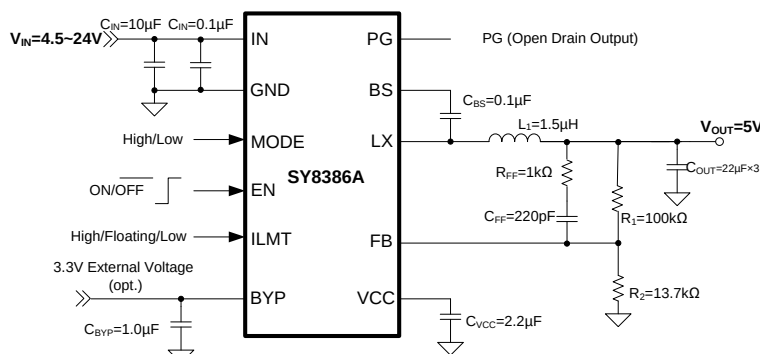


Figure1. Schematic Diagram

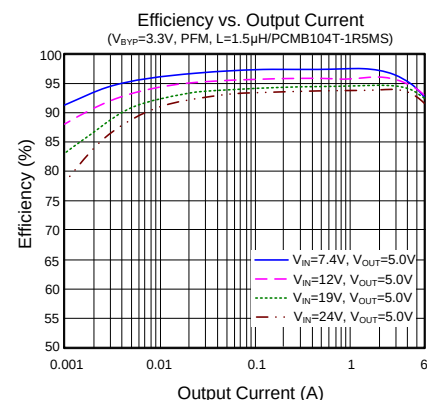
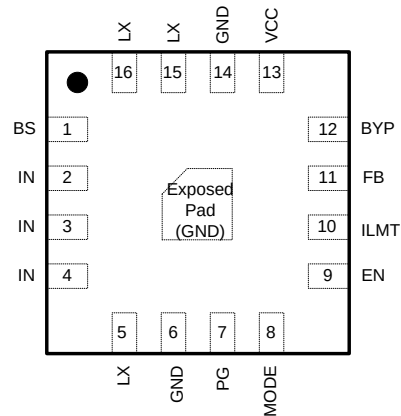


Figure2. Efficiency vs. Load Current

Pinout (top view)

(QFN2.5×2.5-16)

Top Mark: rNxyz (Device code: rN, x=*year code*, y=*week code*, z= *lot number code*)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.
IN	2, 3, 4	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor. A 0.1μF input ceramic capacitor is recommended to reduce the input noise.
LX	5, 15, 16	Inductor pin. Connect this pin to the switching node of the inductor.
GND	6, 14, EP	Ground pin.
PG	7	Power good Indicator. Open drain output when the output voltage is within 90% to 120% of regulation point.
MODE	8	Operating mode selection under light load. Pull this pin low for PFM operating and pull this pin high for FCCM operation. Do not leave this pin floating.
EN	9	Enable control of the IC. Pulled high to turn on the IC and pulled low to turn off the IC.
ILMT	10	Valley current limit threshold selection pin.
FB	11	Output feedback pin. Connect to the center point of the resistor divider.
BYP	12	External 3.3V bypass power supply input. Decouple this pin to GND with a 1μF ceramic capacitor. Leave this pin floating if it is not used.
VCC	13	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with a 2.2μF ceramic capacitor.

Block Diagram

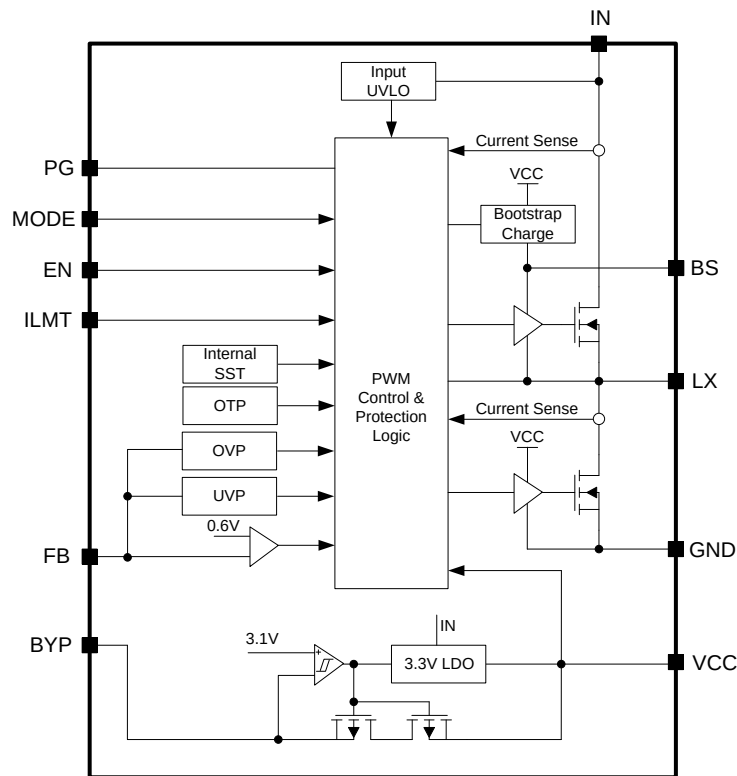


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage	-0.3V to 26V
IN-LX, LX, PG, MODE, EN Voltage	-0.3V to IN+0.3V
BS-LX, FB, VCC, ILMT Voltage	-0.3V to 4V
BYP Voltage	-0.3V to 6V
Maximum Power Dissipation, $P_{D,MAX}$, @ $T_A = 25^\circ\text{C}$ QFN2.5×2.5-16	3W
Package Thermal Resistance (Note 2)	
θ_{JA} , QFN2.5×2.5-16	33°C/W
θ_{JC} , QFN2.5×2.5-16	5.5°C/W
Junction Temperature Range	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C
Dynamic LX Voltage in 10ns Duration	GND-5V to IN+3V
Dynamic LX Voltage in 20ns Duration	GND-5V to IN+2V

Recommended Operating Conditions (Note 3)

Supply Input Voltage	4.5V to 24V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

Electrical Characteristics

($V_{IN}=12V$, $C_{OUT}=100\mu F$, $T_A=25^\circ C$, $I_{OUT}=1A$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		24	V
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			4.2	V
UVLO Hysteresis	V_{HYS}			0.3		V
Quiescent Current	I_Q	$I_{OUT}=0A$, $V_{OUT}=V_{SET}\times 105\%$		100	140	μA
Shutdown Current	I_{SHDN}	$EN=0$		5	9	μA
Feedback Reference Voltage	V_{REF}		0.594	0.600	0.606	V
FB Input Current	I_{FB}	$V_{FB}=1V$	-50		50	nA
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			38		$m\Omega$
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			19		$m\Omega$
Output Discharge Current	I_{DIS}	$V_{OUT}=5V$		100		mA
Top FET Current Limit	$I_{LMT, TOP}$		15			A
Bottom FET Current Limit	$I_{LMT, BOT}$	ILMT=Low	6			A
		ILMT=Floating	8			A
		ILMT=High	10			A
Bottom FET Reverse Current Limit	$I_{LMT, RVS}$	FCCM mode		3.6		A
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100% V_{SET} (Note 4)		1.2		ms
EN/MODE Input Voltage High	$V_{EN, H}$		1			V
EN/MODE Input Voltage Low	$V_{EN, L}$				0.4	V
ILMT Input Voltage High	$V_{ILMT, H}$		$V_{CC}-0.8$			V
ILMT Input Voltage Low	$V_{ILMT, L}$				0.4	V
Switching Frequency	f_{SW}	$V_{OUT}=5V$, CCM	510	600	690	kHz
Min ON Time	$t_{ON, MIN}$	$V_{IN}=V_{IN, MAX}$ (Note 4)		50		ns
Min OFF Time	$t_{OFF, MIN}$			150		ns
VCC Output Voltage	V_{CC}	VCC adds 1mA load	3.15	3.33	3.5	V
Output Over Voltage Threshold	V_{OVP}	V_{FB} rising	115	120	125	% V_{REF}
Output Over Voltage Hysteresis	$V_{OVP, HYS}$			5		% V_{REF}
Output OVP Delay	$t_{OVP, DLY}$	(Note 4)		20		μs
Output Under Voltage Protection Threshold	V_{UVP}		55	60	65	% V_{REF}
Output UVP Delay	$t_{UVP, DLY}$	(Note 4)		200		μs
Power Good Rising Threshold	$V_{PG, R}$	V_{FB} rising (good)	86	90	94	% V_{REF}
Power Good Falling Threshold	$V_{PG, F}$	V_{FB} falling	81	85	89	% V_{REF}
Power Good Delay	$t_{PG, R}$	Low to high (Note 4)		200		μs
	$t_{PG, F}$	High to low (Note 4)		10		μs
Power Good Low Voltage	$V_{PG, LOW}$	$V_{FB}=0V$, $I_{PG}=5mA$			0.4	V
Bypass Switch $R_{DS(ON)}$	$R_{DS(ON), BYP}$			1.2		Ω
Bypass Switch Turn-on Voltage	V_{BYP}		2.9	3.1		V
Bypass Switch Switchover Hysteresis	$V_{BYP, HYS}$			0.2		V
Bypass Switch OVP Threshold	$V_{BYP, OVP}$			120		% V_{LDO}
Thermal Shutdown Temperature	T_{OTP}	T_J rising (Note 4)		150		$^\circ C$
Thermal Shutdown Hysteresis	$T_{OTP, HYS}$	(Note 4)		15		$^\circ C$

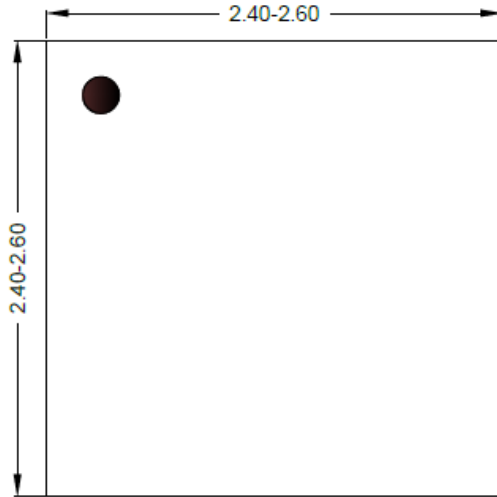
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: Package thermal resistance is measured in the natural convection at $T_A = 25^{\circ}\text{C}$ on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

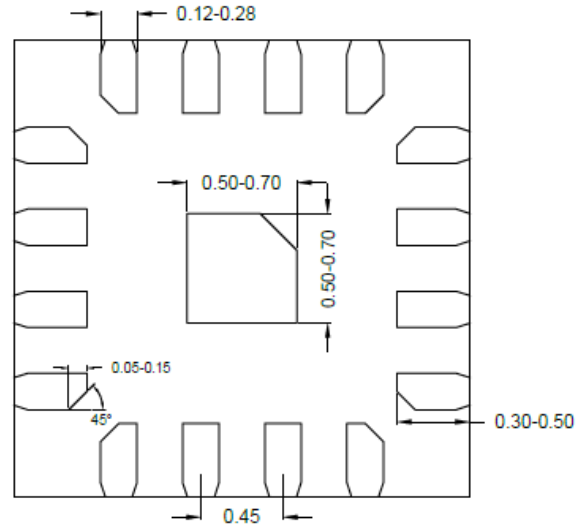
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

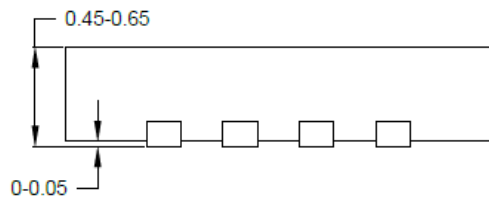
QFN2.5×2.5-16 Package Outline Drawing



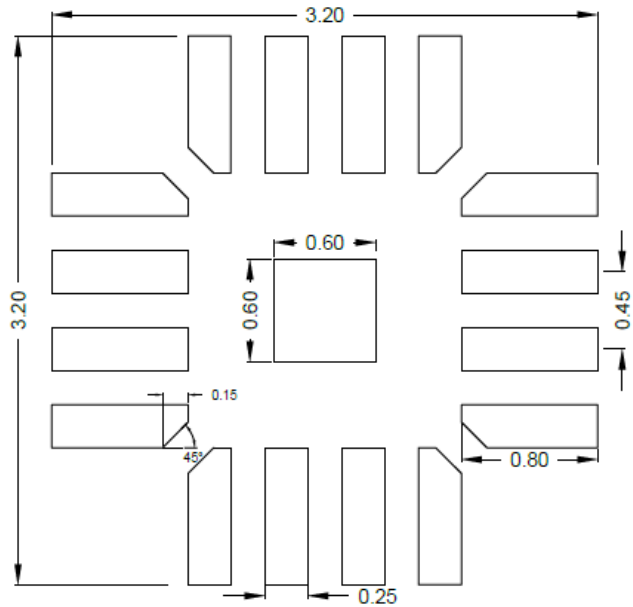
Top view



Bottom view



Side view

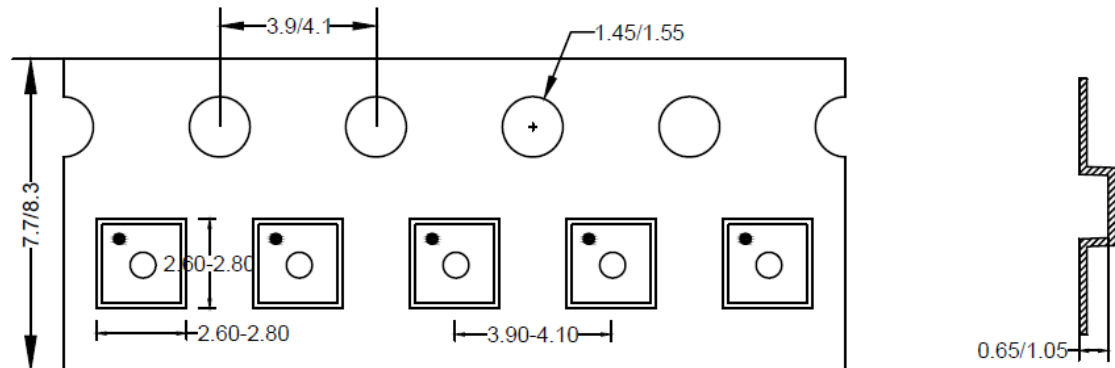


**Recommended PCB layout
(Reference only)**

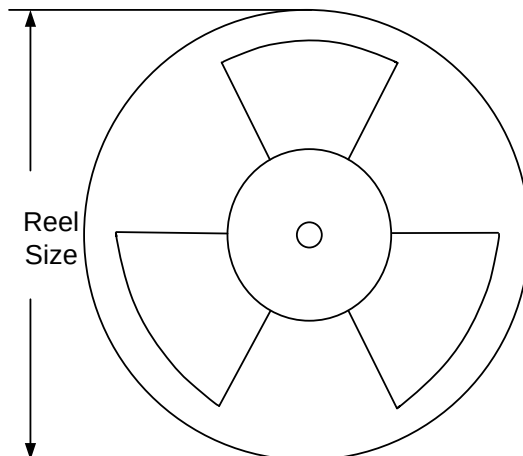
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

1. QFN2.5×2.5 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2.5×2.5	12	4	7"	400	160	3000

3. Others: NA