8A, 24V, 500kHz Synchronous Step-Down Converter

DESCRIPTION

The EUP3098 is an 8A, 24V high efficiency synchronous step-down regulator. The input voltage range is 4.5V to 24V. Internal low RON HS/LS switches of 28mΩ and 15mΩ provide excellent efficiency over a range of applications, especially for low output voltages and low duty cycles.

The EUP3098 constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. So it provides stable operation without complex compensation and even with low ESR ceramic capacitors.

The EUP3098 integrates several protection features to prevent catastrophic switch failure caused by increasing power dissipation. It offer cycle-by-cycle current limit, input under voltage lock-out, internal soft-start, output under voltage protection and over voltage protection and thermal shutdown.

The EUP3098 is available in UQFN2.5×2.5-16 package, operates over the extended (-40°C to +85°C) temperature range.

FEATURES

- 8A Output Current
- Wide Input Voltage Range: 4.5~24V
- Low HS/LS RON: 28/15mΩ
- Internal Soft-start
- Fixed Frequency 500kHz
- Adjustable Output Voltage Application
- High Precision Feedback Voltage : ±1%
- Input UVLO
- PFM/USM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Discharge Function
- Cycle-by-cycle Valley and Peak Current Limit Protection
- Programmable Valley Current Limit Threshold by ILMT Pin
- Output Under Voltage Protection
- Output Over Voltage Protection
- Over Temperature Protection
- Compact Package: UQFN2.5×2.5-16
- RoHS Compliant and Halogen-Free

APPLICATIONS

- TV
- Set Top Box
- High Power AP
- Notebook

Typical Application Circuit

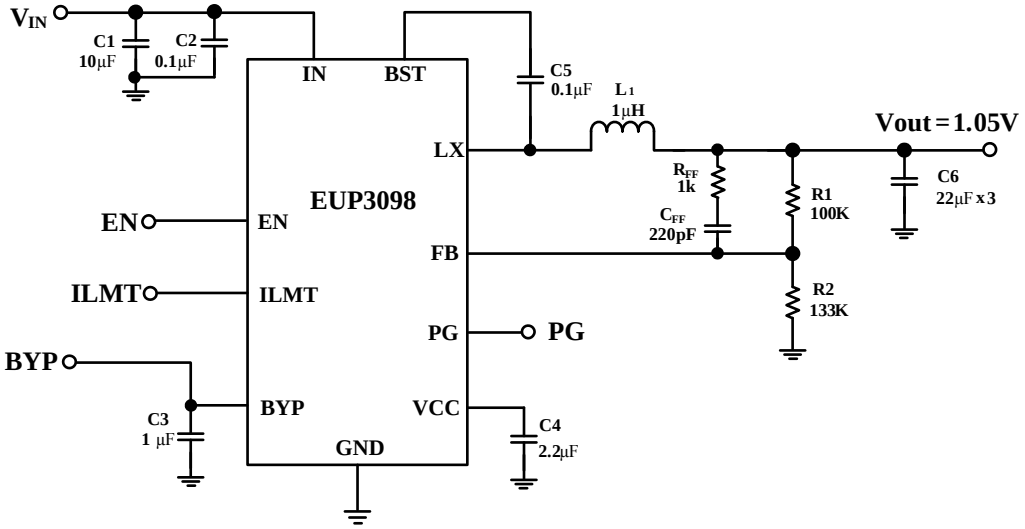
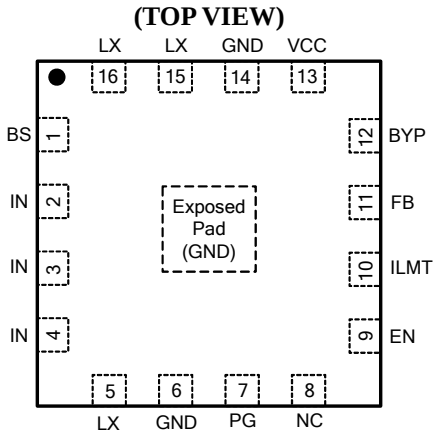


Figure 1. Application Circuit

Pin Configurations

Package Type	Pin Configurations
UQFN2.5×2.5-16	

Pin Description

Pin	Pin Name	Description
BS	1	Bootstrap pin. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin. Supply high side gate driver.
IN	2,3,4	Power supply input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
LX	5,15,16	Switching output pin. Connect this pin to the switching node of the inductor.
GND	6,14,EP	Ground pin.
PG	7	Power good Indicator. Open-drain output when the output voltage is within 90% to 120% of the regulation point. Connect PGOOD to VCC through pull-up resistor.
NC	8	Not connected.
EN	9	Enable control of the DC/DC regulator. Pulling this pin high to turn on the regulator. Do not leave this pin floating. The pin is also used for controlling operation mode of the regulator under light load condition. When its voltage is less than 1.6V, the Buck regulator works under ultra-sonic mode. When it voltage is larger than 2V, the Buck regulator works under PFM mode.
ILMT	10	Valley current limit threshold selection pin. Three choices are available: low, floating and high.
FB	11	Output voltage feedback pin.
BYP	12	External 3.3V bypass power supply input. Decouple this pin to the GND with a 1μF ceramic capacitor. Leave this pin floating if it is not used.
VCC	13	Internal 3.3V LDO output pin. Power supply for internal circuits and driving circuit. Connect a 2.2uF ceramic capacitor between VCC and GND.

Ordering Information

Order Number	Package Type	Marking	Quantity per Reel	Operating Temperature Range
EUP3098SIR1	UQFN-16	xxx d00	3000	-40 °C to +85°C

EUP3098 **S I R 1**

- **1**: Lead Free Code
  1: Lead Free, Halogen-Free
- **R**: Packing
  R: Tape & Reel
- **I**: Operating temperature range
  I: Industry Standard
- **S**: Package Type
  S: UQFN

Block Diagram

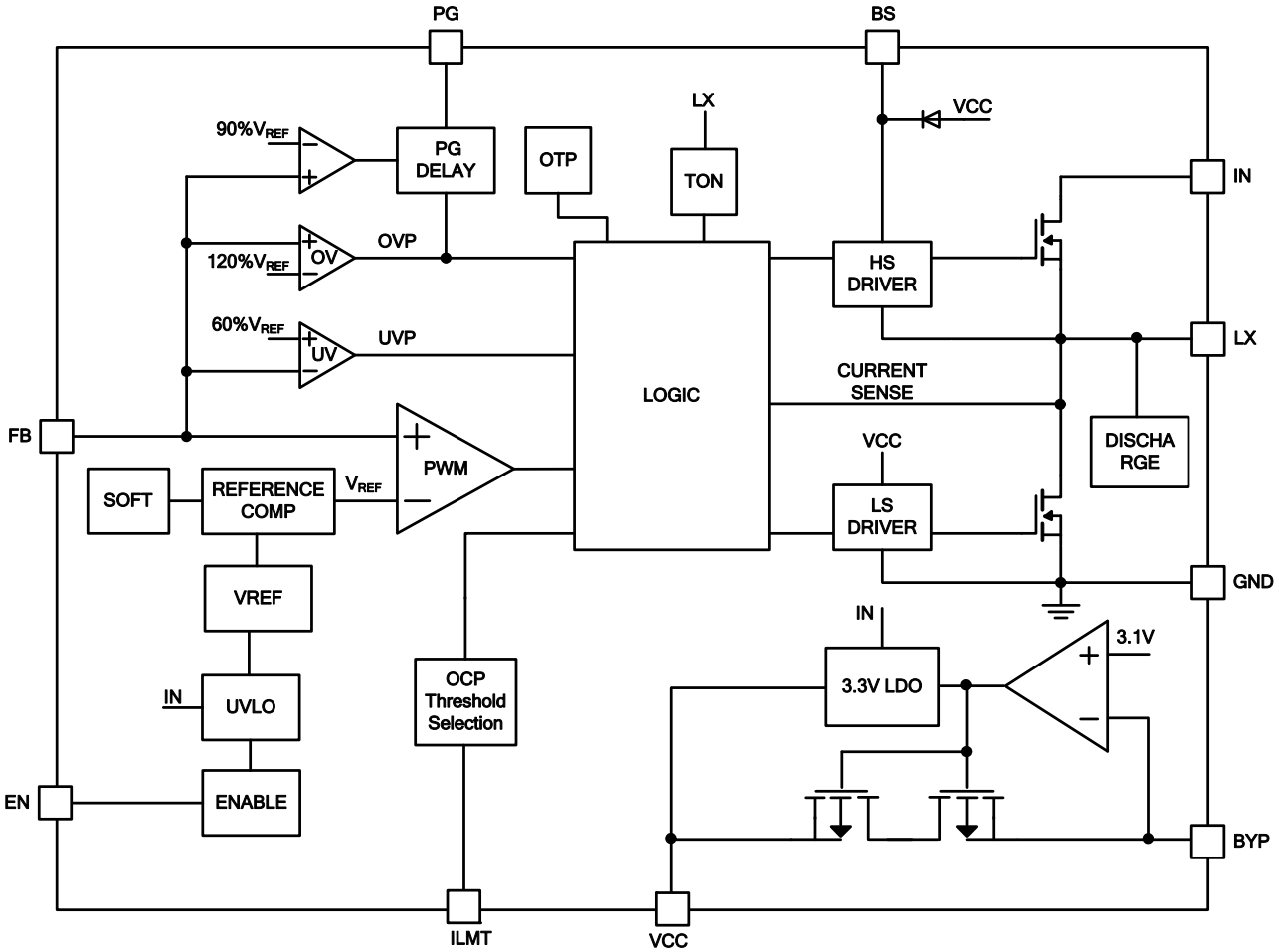


Figure 2. Functional Block Diagram

Absolute Maximum Ratings(1)

- Input Voltage (V_{IN}) ---------- -0.3V to 28V
- LX, PG, EN Voltage ---------- -0.3V to 28V
- FB, VCC, ILMT, BYP Voltage ---------- -0.3V to 6V
- Bootstrap Voltage(V_{BS}) ---------- V_{LX}-0.3V to V_{LX}+6V
- Junction Temperature Range ---------- -40°C to +150°C
- Storage Temperature ---------- -65°C to +150°C
- Lead Temp(Soldering, 10sec) ---------- 260°C
- Thermal Resistance θ_{JA} ---------- 33°C/W
- Thermal Resistance θ_{JC} ---------- 5.5°C/W

Recommend Operating Conditions(2)

- Supply Voltage (V_{IN}) ---------- 4.5V to 24V
- Ambient Operating Temperature ---------- -40°C to +85°C

Note(1):Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.
Note(2):The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

(V_{IN}=12V, TA=+25°C, unless otherwise specified)

Symbol	Parameter	Conditions	EUP3098			unit
			min	typ	max	
V_{IN}	VIN range		4.5		24	V
V_{UVLO}	VIN UVLO	vin rising		4	4.2	V
V_{HYS}	VIN UVLO Hysteresis			0.3		V
I_Q	Quiescent Current	Iout=0		100		μA
I_{SHDN}	Shutdown Current	EN=0		5	9	μA
V_{FB}	Feedback Voltage		0.594	0.6	0.606	V
R_{ONH}	High Side RON			28		mΩ
R_{ONL}	Low Side RON			15		mΩ
R_{DIS}	Discharge Resistor			26		Ω
I_{LMTHS}	HS Current Limit (Peak)		15	17.5	20	A
I_{LMTLS}	LS Current Limit (Valley)	ILMT=low	8	10		A
		ILMT=floating	10	12		A
		ILMT=high	12	14		A
I_{LMTRVS}	LS Reverse Current Limit	USM mode		3		A
t_{SS}	Soft-Start Time			500		μs
V_{EN}	Enable Threshold	On state	1			V
		Off state			0.4	V
V_{EN_USM}	EN USM Threshold		1		1.6	V
V_{EN_PFM}	EN PFM Threshold		2			V
f_{SW}	Frequency	Vout=1.2V, CCM		500		kHz
f_{USM}	USM Frequency	Iout=0, USM	20			kHz
t_{ON_MIN}	Minimum on Time			50		ns
t_{OFF_MIN}	Minimum off Time			200		ns
V_{CC}	VCC Output Voltage		3.15	3.3	3.45	V

Electrical Characteristics (Continued)

(VIN=12V, T_A=+25°C, unless otherwise specified)

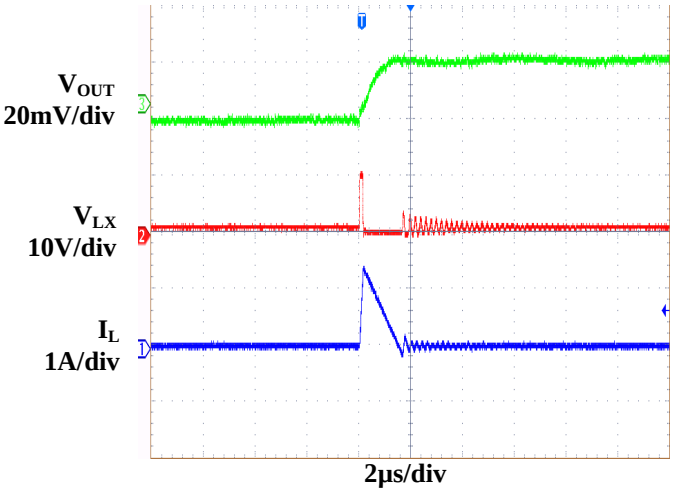
V_{OVP}	Output OVP Threshold	FB rising	116	120	124	$\%V_{FB}$
V_{OVP_HYS}	VOUT OV Hysteresis	FB falling		5		$\%V_{FB}$
t_{OVP}	Output OVP Delay Time			20		μs
V_{UVP}	Output UVP threshold	FB falling	55	60	65	$\%V_{FB}$
t_{UVP}	Output UVP Delay Time			200		μs
V_{PGR}	PGOOD Low to High Threshold	FB rising	85	90	95	$\%V_{FB}$
V_{PGF}	PGOOD High to Low Threshold	FB falling	80	85	90	$\%V_{FB}$
t_{PGR}	PGOOD Delay Time	low to high		200		μs
t_{PGF}		high to low		10		μs
V_{PG_LOW}	PGOOD Low Voltage	I_{PG}=5mA			0.4	V
V_{BYP}	BYP Switch Turn on Voltage			3.1		V
V_{BYP_HYS}	BYP Switch Turn on Hysteresis			0.2		V
V_{BYP_OVP}	BYP OVP Threshold			120		%VCC
T_{OTP}	Thermal Shutdown Threshold			160		℃
T_{OTP_HYS}	Thermal Shutdown Hysteresis			40		℃

Typical Operating Characteristics

T_A=25°C, V_{IN}=12V, V_{OUT}=1.05V, L=1µH, C_{OUT}=22µF×3, unless otherwise specified.

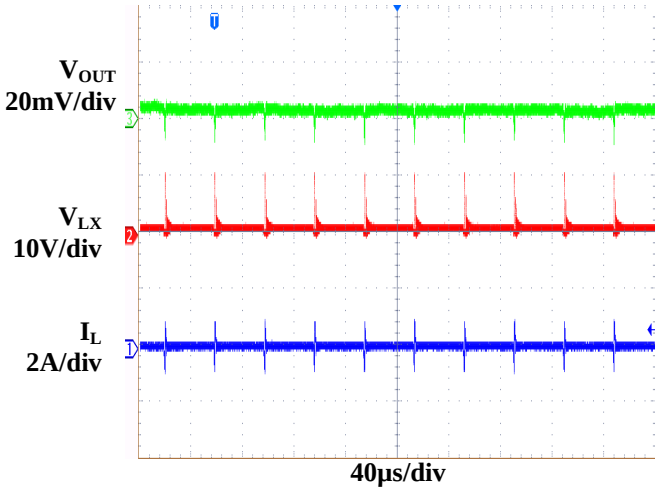
Output Ripple

V_{IN}=12V, V_{OUT}=1.05V, No load, PFM



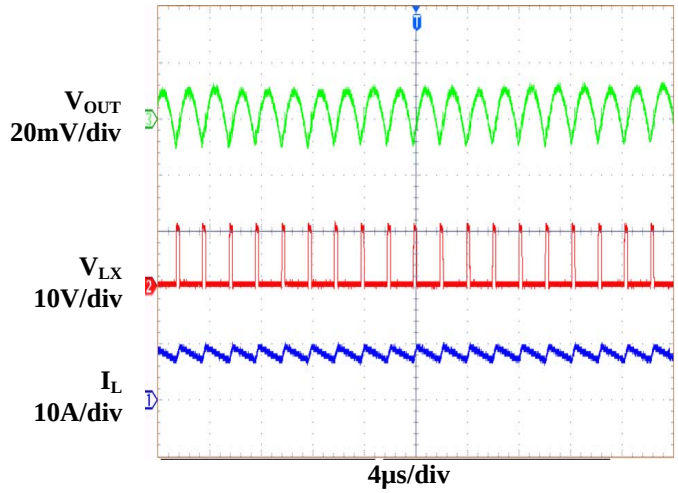
Output Ripple

V_{IN}=12V, V_{OUT}=1.05V, No load, USM



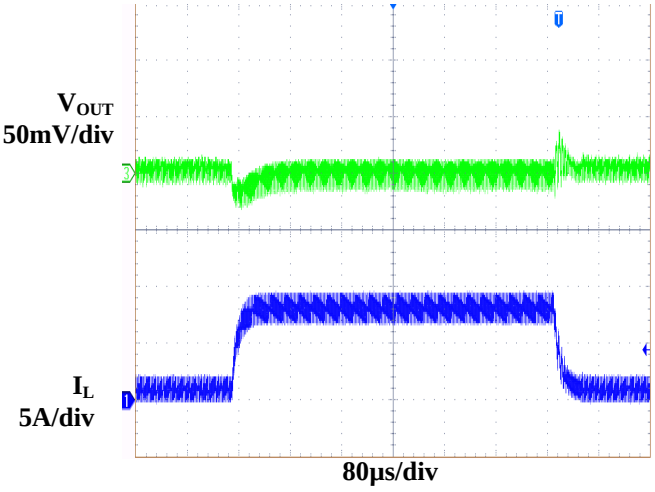
Output Ripple

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A



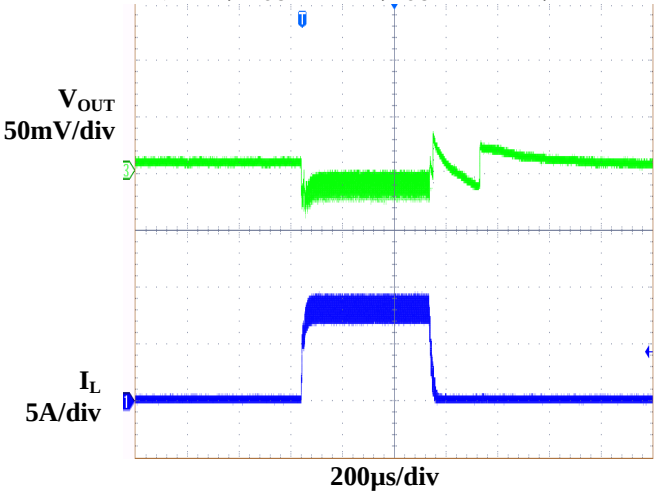
Load Transient

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=0.8-8A, PFM



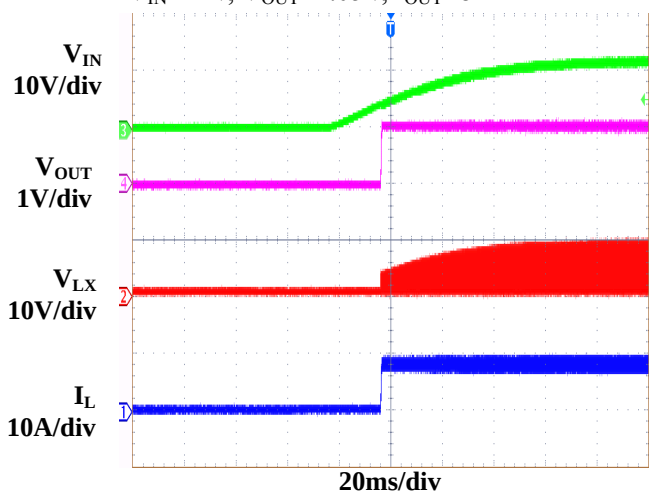
Load Transient

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=0 to 8A, PFM



Startup through V_{IN}

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A

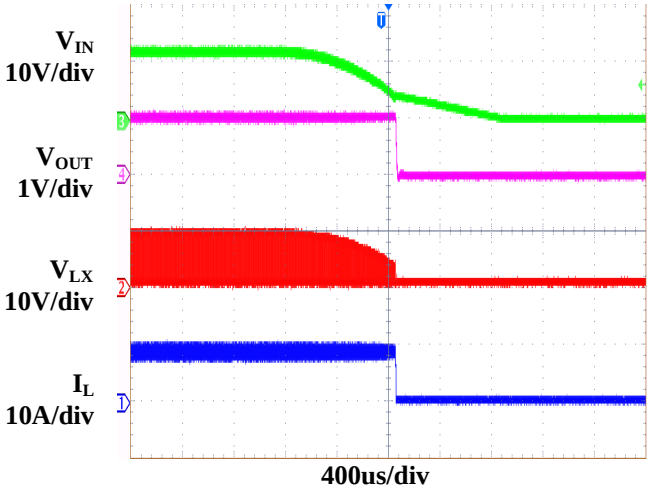


Typical Operating Characteristics

T_A=25°C, V_{IN}=12V, V_{OUT}=1.05V, L=1µH, C_{OUT}=22µF×3, unless otherwise specified.

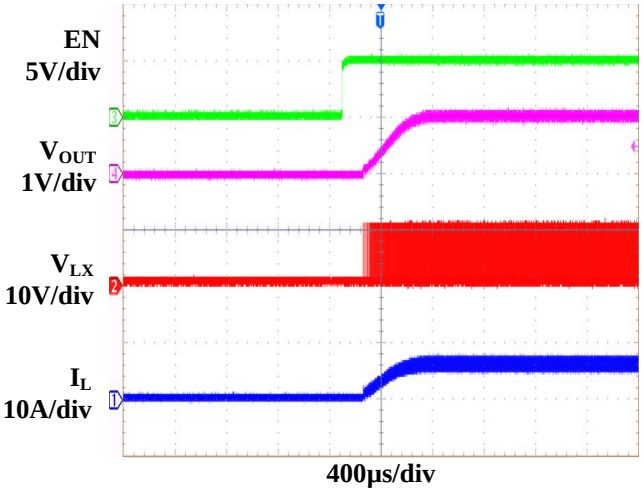
Shutdown through V_{IN}

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A



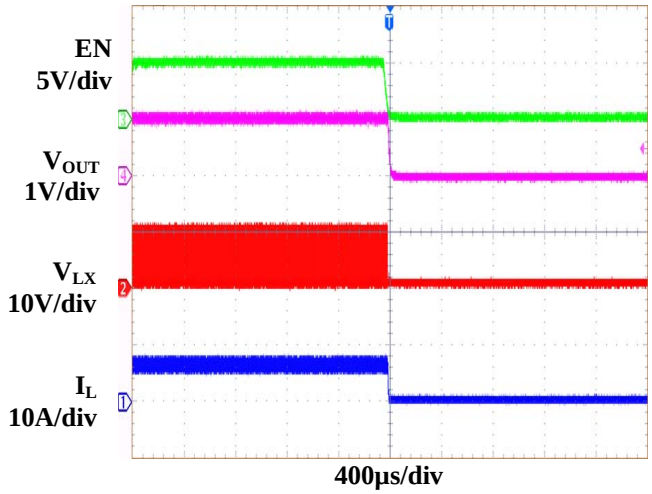
Startup through Enable

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A



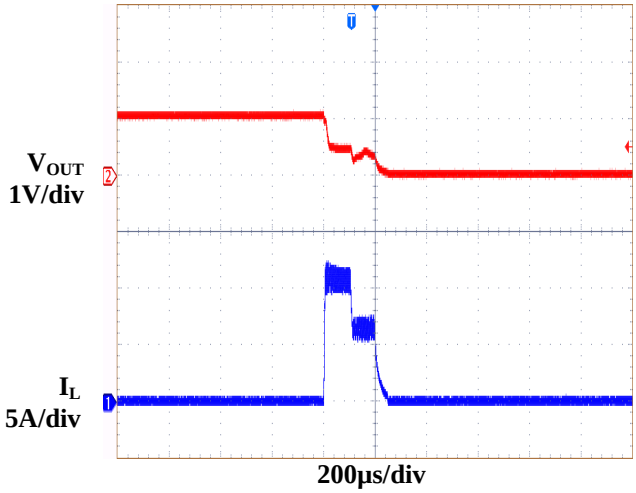
Shutdown through Enable

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A,



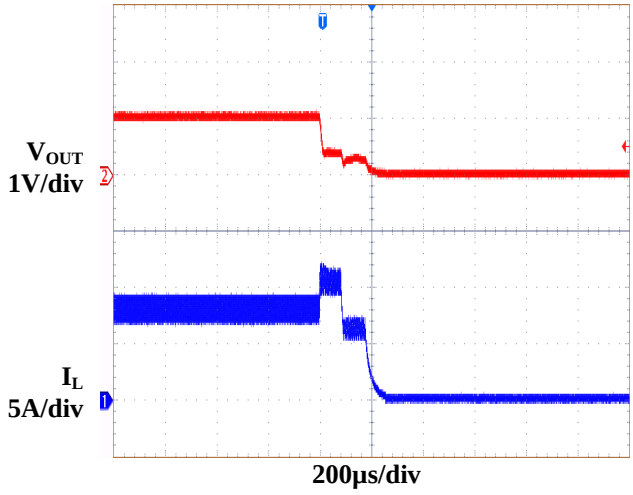
Short Circuit Protection

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=0A, ILMT=Low



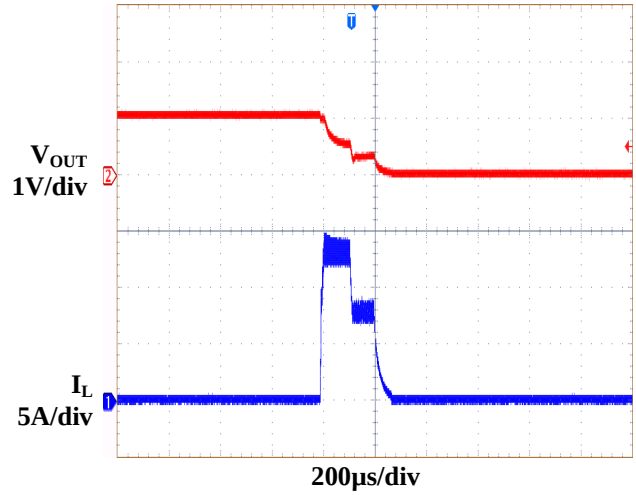
Short Circuit Protection

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A, ILMT=Low



Short Circuit Protection

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=0A, ILMT=Float

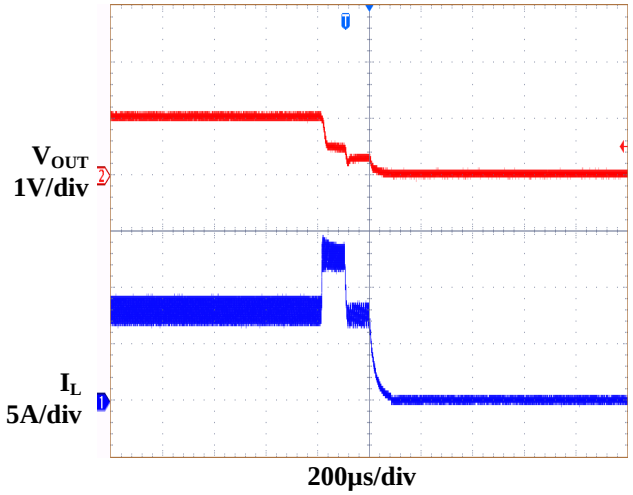


Typical Operating Characteristics

T_A=25°C, V_{IN}=12V, V_{OUT}=1.05V, L=1µH, C_{OUT}=22µF×3, unless otherwise specified.

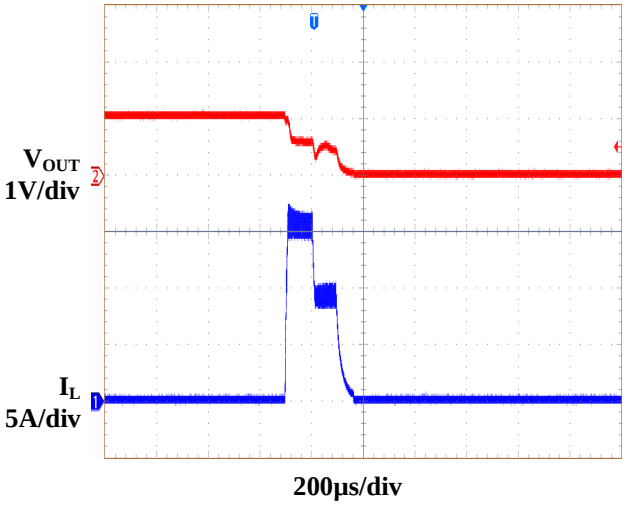
Short Circuit Protection

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A, ILMT=Float



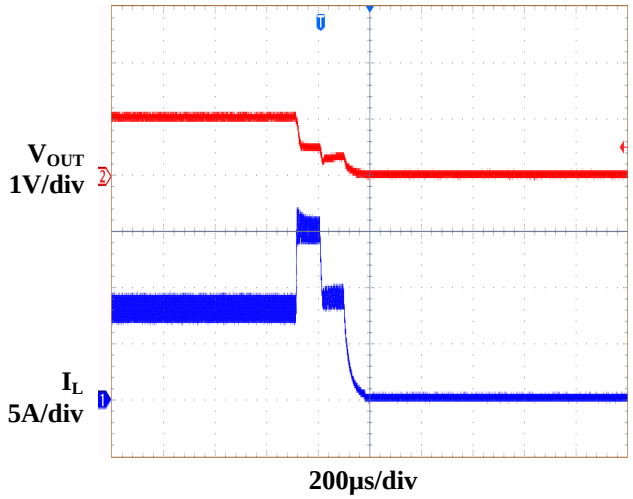
Short Circuit Protection

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=0A, ILMT=High

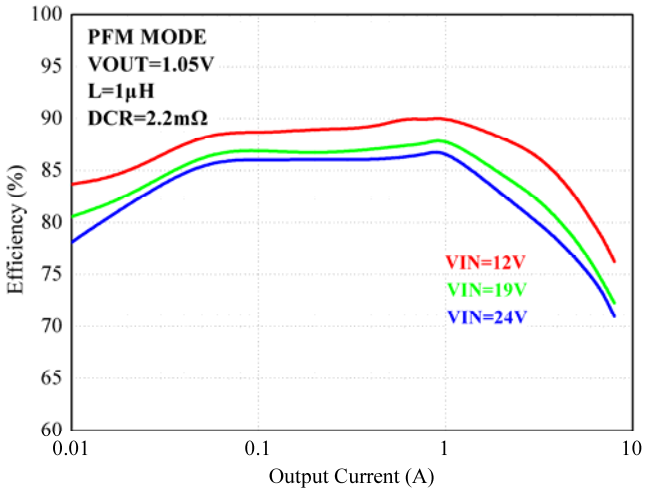


Short Circuit Protection

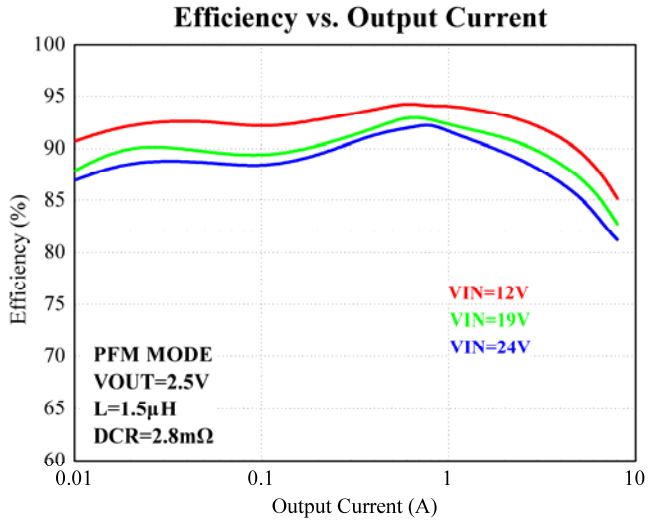
V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A, ILMT=High



Efficiency vs. Output Current



Efficiency vs. Output Current



Functional Description

The EUP3098 is a constant on-time synchronous step-down converter with 4.5V to 24V input power supply. The device can provide up to 8A continuous current to the output. This architecture provides very fast on-time response to output load transients. In a COT architecture, there is no fixed clock, so the high-side power switch can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between LX and BS is needed to drive the high side gate. The bootstrap capacitor is charged from the VCC pin when LX is low. At light loads, the inductor current may reach zero or reverse on each pulse. The bottom MOS is turned off by the current reversal comparator and the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for the switching regulator. At light load, the EUP3098 will automatically skip pulses in pulse frequency modulation (PFM) mode to maintain output regulation and increases efficiency.

When the FB pin voltage exceeds 20% of the nominal regulation value of 0.6V, the over voltage comparator is tripped and forcing the high-side switch off.

Constant On-time Architecture with Reference Compensation

The EUP3098 uses constant on-time control method with reference compensation as shown below:

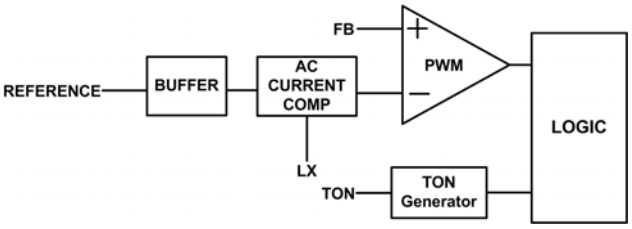


Figure 3. Simplified control topology of EUP3098

The on-time of EUP3098 is determined by TON generator whose pulse width can be determined by duty cycle. And this pulse is triggered when the feedback voltage (V_{FB}) reaches the compensation reference voltage, which is the internal reference voltage further processed by the AC current information of inductor. This compensation reference voltage can help the loop stability in pure ceramic output capacitors application, for low ESR of ceramic capacitor would cause unstable condition.

The constant on-time control architecture is a pseudo-fixed frequency and does not use a clock signal to produce trigger signal. The on-time of high-side switch is set by internal circuits, which is proportional to output voltage V_{OUT} and inverse proportional to input voltage V_{IN}. As in buck DC-DC converter we have:

$$T_{ON} = D \times T = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{LX}}$$

For example, considering that a hypothetical converter targets 1.2V output from a 12V input at 500kHz, the target on-time is (1.2V/12V)×(1/500kHz) = 200ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage drops below the target value. After one t_{ON} period, a minimum off-time (t_{OFF_MIN}) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids the making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

Soft-Start

The EUP3098 has internal soft start feature to minimize the inrush supply current and the output overshoot at initial startup. When the EUP3098 starts up, the internal reference voltage which is compared with V_{FB} ramps up gradually, so the output voltage ramps up as well. The typical soft-start time is around 500µs.

Light Load Operation Mode

PFM or USM light load operation is selected by EN pin. EN is not only the enable pin but also mode selection pin to control operation mode of the regulator under light load condition after the output of Buck regulator is within the regulation range. If the voltage on this pin is lower than 1.6V and higher than its rising threshold, the EUP3098 regulator works under ultra-sonic mode (USM). If the voltage on this pin is greater than 2V, the EUP3098 works under pulse-frequency modulation mode (PFM).

If the EUP3098 works under PFM mode and light load conditions, the current through the low-side NMOS will reach to near zero before the next t_{ON} time. The device enters continuous conduction mode（CCM） once the load current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range. The critical level of the load current is determined with

$$I_{out\_hys} = \frac{\Delta I_L}{2} = \frac{V_{out} \times (1 - D)}{2 \times F_{lx} \times L_1}$$

If USM light load operation is selected, it keeps the switching frequency above an audible frequency area even under light load or null load conditions. Once the device detects that both the high-side Power MOS and the low-side MOS turn off for more than one certain time, it forces the low-side MOS turn on and discharge the output capacitor so that the switching frequency is

out of audio range.

Output Discharge

The EUP3098 discharges the output voltage when the converter shuts down from VIN or EN, or thermal shutdown, so that output voltage can be discharged in a minimal time, even load current is zero. The discharge FET in parallel with the low-side MOS turns on when shut down logic is triggered. The output discharge resistor is typically 26Ω.

VCC Linear Regulator

The EUP3098 integrates one high performance, low drop-out linear regulator 3.3V VCC, which can power the internal circuitry and charge the bootstrap capacitor when LX is low. VCC is supplied by IN voltage. Connect a 2.2μF low ESR ceramic capacitor from VCC to GND.

BYP Input Mode

The internal circuit can also be powered by external 3.3V power supply. When a 3.3V external power supply is connected to the BYP pin, the VCC LDO is disabled and the switch between BYP and VCC is turned on. The efficiency may be improved by connecting the BYP pin to external 3.3V power supply especially when VIN is very high. Connect a 1.0μF low ESR ceramic capacitor from BYP pin to GND if an external 3.3V power supply is used. Leave BYP pin floating if this feature is not used.

Over Current Protection

If the sensed current value is above the over current (low side MOS valley current limit) setting, the converter delays the next on-time pulse until the current drops below the OC limit. Current limiting occurs on a pulse-by-pulse basis. The EUP3098 uses a valley current limiting scheme where the DC current point is the OC limit plus half of the inductor ripple current.

$$I_{OC\_DC} = I_{OC\_vally} + \frac{1}{2} \times I_{Peak-to-Peak}$$

The device supports programmable valley current limit threshold through ILMT pin. Three typical current limit value of 10A, 12A, 14A can be chosen when the ILMT pin pulled low, floating and high.

Over Voltage Protection

OVP (over voltage protection) function with fixed OV (over voltage) threshold is provided. If the output voltage exceeds over voltage protection threshold and keeps for about 20μs, the output over voltage protection (OVP) will be triggered, and the device will latch off. Recycling EN input to re-enable the device.

Under Voltage Protection

UVP (under voltage protection) function continually monitors the FB voltage after soft-start is completed. If output voltage is lower than 60% of the set point for approximately 200μs occurring when the output short circuit or the load current is heavier than the maximum current capacity, the UVP will be triggered, and the device will latch off. Recycling EN input to re-enable the device.

Power Good

The EUP3098 has one open-drain power good (PGOOD) pin. The PGOOD pin de-asserts as soon as the EN pin is pulled low, it should be connected to V_{IN} or another voltage source through a 100kΩ resistor. After V_{IN} exceeds its own UVLO (rising) threshold, the PG FET is turned on so that PG is pulled to GND before output voltage is ready. After feedback voltage VFB reaches V_{PGR}, PG is pulled high after a delay time of 200μs. When V_{FB} drops to V_{PGF}, or rises to V_{OVP} for one OVP delay time, PG is pulled low after a delay time of 10μs.

Thermal Shutdown

The EUP3098 stops switching when its junction temperature exceeds 160°C. The device will latch off. Recycling EN input to re-enable the device when the temperature has dropped by 40°C to protect the device.

Application Information

Setting the Output Voltage

The output voltage is set through a resistive voltage divider and can be expressed by the equation as follows

$$V_{out} = 0.6 \times \frac{R_1 + R_2}{R_2}$$

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will in turn result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{LX} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{LX} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current. Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times F_{LX} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where I_{LOAD} is the load current. The choice of which style inductor to use mainly depends on the price v.s. size requirements and any EMI constraints.

When in the USM mode, make sure the inductor value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors. Since the input capacitor (C_1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{C1} = I_{LOAD}/2$. For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current.

When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C_1 \times F_{LX}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_1 is the input capacitance value. For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current. The capacitance value is less important than the RMS current rating. In most applications a single 10µF X5R capacitor is sufficient. Take care to locate the ceramic input capacitor as close to the device IN and GND pin as possible.

Output Capacitor

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{out} = \frac{V_{out}}{F_{lx} \times L} \times \left(1 - \frac{V_{out}}{V_{in}}\right) \times \left(R_{esr} + \frac{1}{8 \times F_{lx} \times Cout}\right)$$

Where C_{OUT} is the output capacitance value and R_{esr} is the equivalent series resistance (ESR) value of the output capacitor. When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance which is the main cause for the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{out} = \frac{V_{out}}{8 \times F_{lx}^2 \times L \times Cout} \times \left(1 - \frac{V_{out}}{V_{in}}\right)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{LX} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The EUP3098 can be optimized for a wide range of capacitance and ESR values.

Thermal Considerations

To avoid the EUP3098 from exceeding the maximum junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = P_D \times \theta_{JA}$$

$$P_D = V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT} - I_{OUT}^2 \times R_{DCR}$$

Where P_D is the power dissipated by the regulator; θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature; R_{DCR} is resistor of inductor. Then the junction temperature, T_J, is given by:

$$T_J = T_A \times T_R$$

where T_A is the ambient temperature. T_J should be below the maximum junction temperature of 150°C.

PCB Layout Checklist

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems. When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3098.

1. The input capacitor should place to VIN pin as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
2. The C_{OUT} negative sides are connected with GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
3. The power traces, consisting of the GND trace, the LX trace and the VIN trace should be kept short, direct and wide.
4. Place the VCC capacitor close to VCC using short, direct copper trace to one nearest device GND pin.
5. Place the BYP capacitor close to BYP using short, direct copper trace to one nearest device GND pin if bypass function is used.
6. The resistive divider R1/R2 and the R_{FF} and C_{FF} must be connected as close as possible between the FB and GND. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive.
7. Keep the switching node, LX, away from the sensitive VOUT/FB node. Keep LX area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance.
8. Place the BS capacitor on the same layer as the device; keep the BS voltage path as short as possible.

An example of PCB layout guide is shown in the figure below for reference.

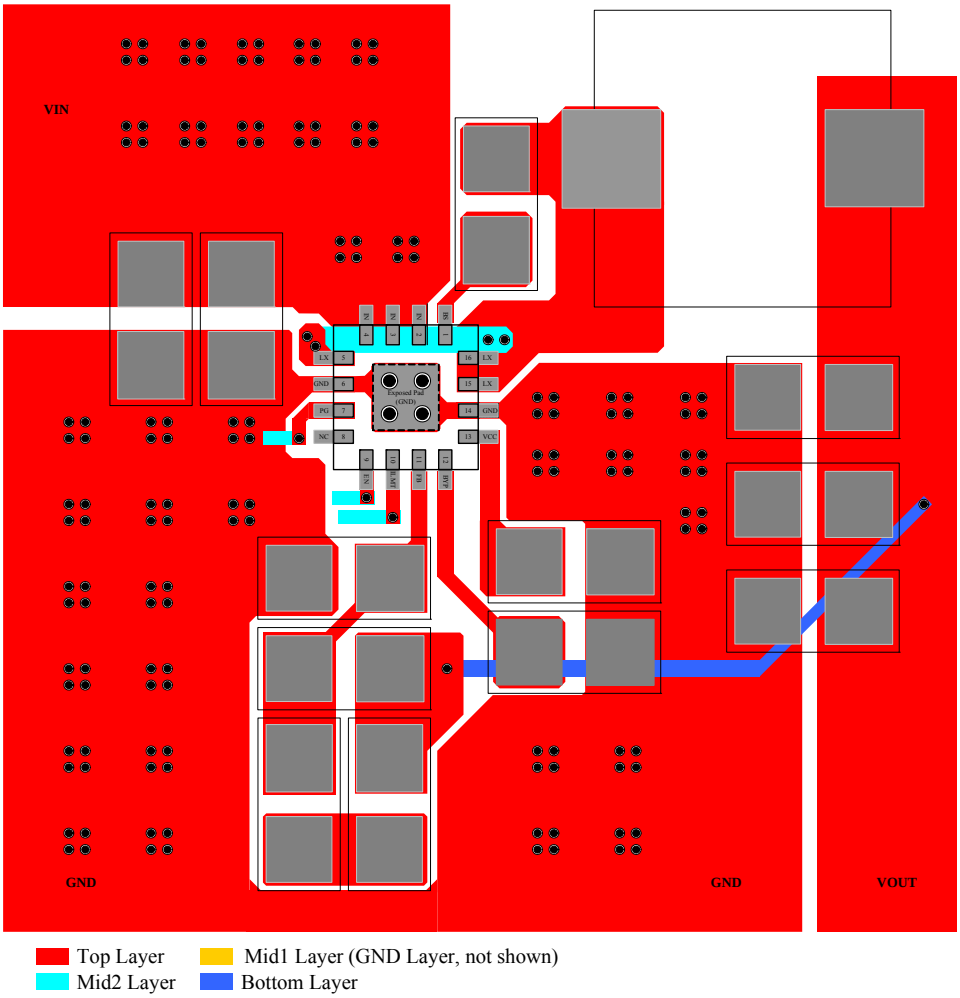
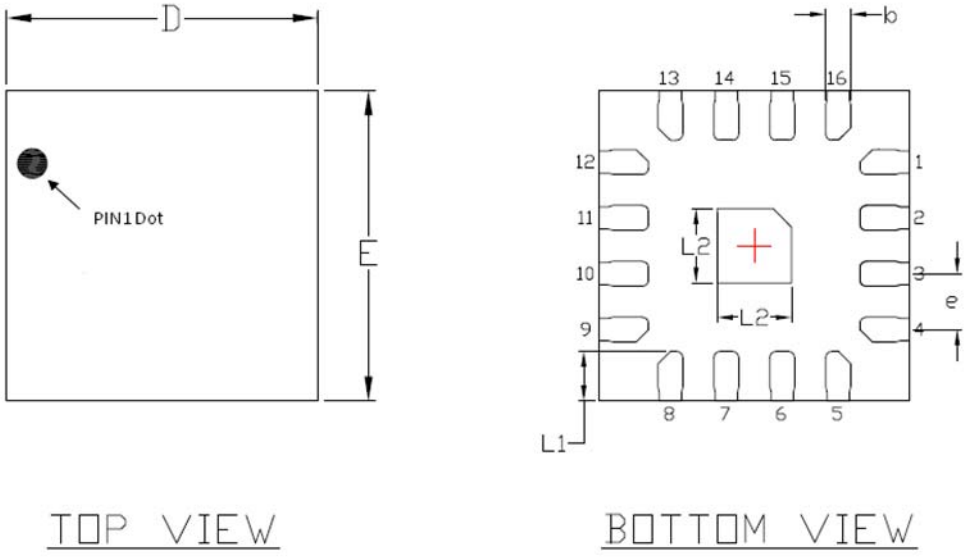
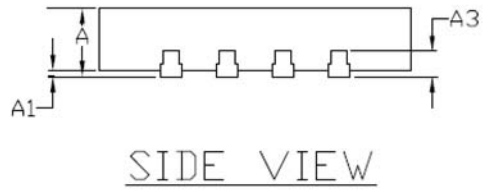


Figure 4. PCB Layout Example

Packaging Information

UQFN-16L(2.5×2.5)





Note: The exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.500	0.550	0.600	0.020	0.022	0.024
A1	0.000	-	0.050	0.000	-	0.002
A3	0.152 REF			0.006 REF		
D	2.450	2.500	2.550	0.096	0.098	0.100
E	2.450	2.500	2.550	0.096	0.098	0.100
e	0.450 REF			0.018 REF		
b	0.150	0.200	0.250	0.006	0.008	0.010
L1	0.350	0.400	0.450	0.014	0.016	0.018
L2	0.550	0.600	0.650	0.022	0.024	0.026