# SGMM2060
# 6A, High Efficiency, 3D Buck PowerSoC

## GENERAL DESCRIPTION

The SGMM2060 device is a 2.7V to 5.5V synchronous Buck power module with AHP-COT architecture that is an optimized solution for high efficiency and compact size. The device integrates switches capable of delivering an output current up to 6A.

For SGMM2060, the device operates in force PWM mode at light and heavy loads. In shutdown state, the current consumption is reduced to 0.03μA (TYP).

The compact and low profile device is in a package of 3mm × 3mm × 1.72mm, allowing the system to achieve high density.

The SGMM2060 is available in a Green EMSIP-3×3-20L package.

## FEATURES

- **AHP-COT Control**
- **6A Continuous Output Current**
- **2.7V to 5.5V Input Voltage Range**
- **1.2MHz Switching Frequency**
- **Low Dropout with 100% Duty Cycle**
- **Adjustable Output Voltage from 0.6V to $V_{IN}$**
- **Output Discharge Function**
- **1.3ms Internal Soft-Start Time and Pre-Biased Startup**
- **Cycle-by-Cycle Over-Current Protection**
- **Hiccup Mode OCP/Short-Circuit Protection**
- **Stable with Low ESR Output Ceramic Capacitors**
- **Thermal Shutdown Protection**
- **Available in a Green EMSIP-3×3-20L Package**

## APPLICATIONS

Field-Programmable Gate Array (FPGA)
Power Systems
Optical Modules
Telecom
Networking
Industrial Equipment



## SIMPLIFIED SCHEMATIC

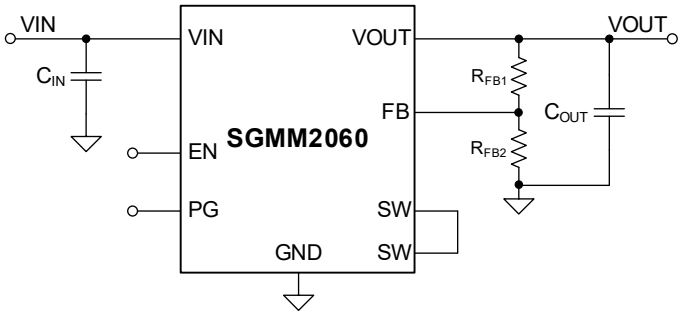



**Figure 1. Simplified Schematic**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGMM2060 | EMSIP-3×3-20L | -40℃ to +125℃ | | | |

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Pin Voltages Referred to GND

VIN, FB, EN, PG ..... -0.3V to 6V

SW (DC) ..... -0.3V to $V_{IN}$ + 0.3V

SW (AC, Less than 10ns) while Switching ..... -3V to 8V

Junction Temperature Range ..... -40℃ to +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (1) (2)

HBM ..... ±4000V

CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

## RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, $V_{IN}$ ..... 2.7V to 5.5V

Output Voltage Range, $V_{OUT}$ ..... 0.6V to $V_{IN}$

Maximum $V_{PG}$ ..... 5.5V

Output Current Range, $I_{OUT}$ ..... 0A to 6A

Operating Junction Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

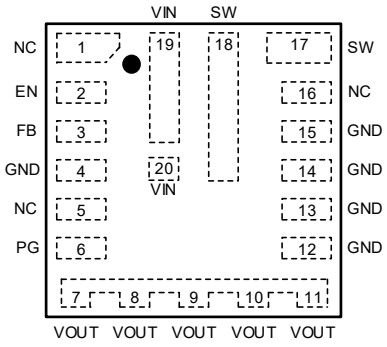
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




EMSIP-3×3-20L

## PIN DESCRIPTION

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 1, 5, 16 | NC | — | Not connected internally. |
| 2 | EN | I | Device Enable Input. Enable: high voltage level. |
| 3 | FB | I | Feedback Pin for Internal Control Loop. Connect this pin to an external feedback divider. |
| 4, 12, 13, 14, 15 | GND | G | Ground Pin. Connect these pins to larger copper areas to the negative terminals of the input and output capacitors. |
| 6 | PG | O | Power Good Open-Drain Output Pin. The output of this pin is an open-drain with an internal 570kΩ pull-up resistor to VIN. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level, otherwise it is low. There is a 105μs delay between the time $V_{FB}$ reaches PG threshold and the time PG pin goes high. |
| 7, 8, 9, 10, 11 | VOUT | O | Output Voltage Pin. |
| 17,18 | SW | O | Switch Output. Use a wide PCB trace to connect the two SW pins together. |
| 19, 20 | VIN | P | Power Supply Voltage Input. A decoupling capacitor is required to ground to reduce switching spikes. The input capacitor should be placed as close as possible to the IC pins. Use a wide PCB trace to connect the two VIN pins together. |

NOTE: I = input, O = output, P = power, G = ground.

# ELECTRICAL CHARACTERISTICS

($V_{IN}$ = 3.6V and $T_J$ = -40℃ to +125℃, and all typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | |
| Input Voltage Range | $V_{IN}$ | | | 2.7 | | 5.5 | V |
| Quiescent Current into VIN Pin | $I_Q$ | Not switching, $V_{IN}$ = 3.6V, $V_{EN}$ = 2V, $V_{FB}$ = 0.65V | $T_J$ = +25℃ | | 620 | | μA |
| | | | $T_J$ = -40℃ to +125℃ | | 630 | | |
| Shutdown Current into VIN Pin | $I_{SD}$ | $V_{EN}$ = 0V | $T_J$ = +25℃ | | 0.03 | | μA |
| | | | $T_J$ = -40℃ to +125℃ | | TBD | | |
| Input Under-Voltage Lockout Threshold | $V_{UVLO}$ | $V_{IN}$ rising, no load | | | 2.55 | | V |
| Input Under-Voltage Lockout Hysteresis | | $V_{IN}$ falling hysteresis, no load | | | 300 | | mV |
| Thermal Shutdown | $T_{SD}$ | Junction temperature rising | | | 165 | | ℃ |
| | | Junction temperature falling | | | 135 | | |
| **EN Input** | | | | | | | |
| High-Level Threshold at EN Pin | $V_{IH}$ | | | 1.2 | | | V |
| Low-Level Threshold at EN Pin | $V_{IL}$ | | | | | 0.4 | V |
| EN Input Leakage Current | $I_{ENLKG}$ | $V_{EN}$ = 3.6V | | | 3.6 | | μA |
| **Soft-Start, Power Good** | | | | | | | |
| Soft-Start Time | $t_{SS}$ | Time from $V_{EN}$ high to 95% of $V_{OUT}$ nominal | | | 1.3 | | ms |
| Power Good Threshold | $V_{PG}$ | $V_{FB}$ rising, referenced to $V_{FB}$ nominal | | | 90 | | % × $V_{FB\_NOM}$ |
| | | $V_{FB}$ falling, referenced to $V_{FB}$ nominal | | | 85 | | |
| Power Good Over-Voltage Threshold | $V_{PG\_OV}$ | PG OV threshold rising | | | 115 | | |
| | | PG OV threshold falling | | | 110 | | |
| Power Good Low-Level Output Voltage | $V_{PG\_OL}$ | $I_{SINK}$ = 1mA | | | 0.1 | | V |
| PG Internal Pull-up Resistor | $R_{PG}$ | | | | 570 | | kΩ |
| Power Good Delay Time | $t_{PG\_DLY}$ | PG rising edge | | | 105 | | μs |
| **Output and Feedback** | | | | | | | |
| Feedback Regulation Voltage (ADJ) | $V_{FB\_NOM}$ | $V_{IN}$ = 2.7V to 5.5V, $T_J$ = +25℃ | | | 0.600 | | V |
| Feedback Input Leakage Current | $I_{FB\_LKG}$ | $V_{FB}$ = 0.65V | | | 1 | | nA |
| Output Discharge Resistor | $R_{DIS}$ | $V_{EN}$ = low, $V_{OUT}$ = 1.8V | | | 140 | | Ω |
| **Power Switch** | | | | | | | |
| Inductance of the Integrated Inductor | L | | | | 470 | | nH |
| Input Capacitor | C | | | | 100 | | nF |
| Total PWM-On Resistance | $R_{DSON}$ | $V_{IN}$ = 2.7V, PWM-On, resistance from VIN to VOUT | | | 35 | | mΩ |
| | | $V_{IN}$ = 3.6V, PWM-On, resistance from VIN to VOUT | | | 30 | | |
| Total PWM-Off Resistance | | $V_{IN}$ = 2.7V, PWM-Off, resistance from VIN to VOUT | | | 23 | | |
| | | $V_{IN}$ = 3.6V, PWM-Off, resistance from VIN to VOUT | | | 20 | | |
| PMOS SW Leakage Current | $I_{SW\_LKG}$ | $V_{IN}$ = 5.5V | | | 0.4 | | μA |
| NMOS SW Leakage Current | | | | | -0.08 | | |
| High-side Peak Current Limit | $I_{LIM\_H}$ | $T_J$ = -40℃ to +125℃ | | | 13 | | A |
| Low-side Valley Current Limit | $I_{LIM\_L}$ | | | | 11 | | |
| Low-side Negative Current Limit | $I_{LIM\_LN}$ | OVP | | | -5 | | |
| Switching Frequency | $f_{SW}$ | $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A | | | 1.2 | | MHz |
| **Controller** | | | | | | | |
| Minimum Off-Time | $t_{OFF\_MIN}$ | $V_{IN}$ = 3.4V, $V_{OUT}$ = 3.3V | | | 45 | | ns |

## FUNCTIONAL BLOCK DIAGRAM

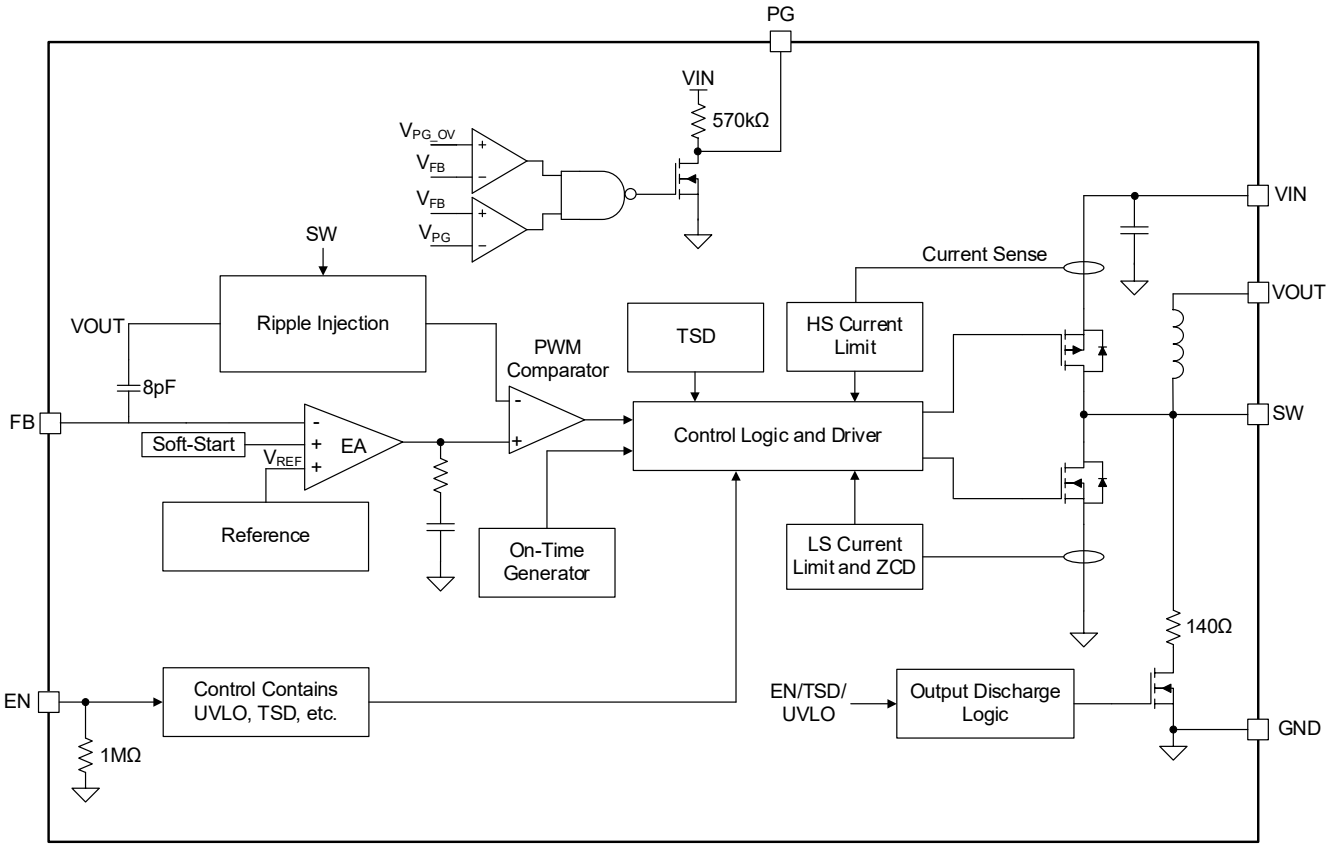



**Figure 2. Block Diagram**

# DETAILED DESCRIPTION

## Overview

The SGMM2060 is a high efficiency synchronous Buck switching power module. The device operates in an AHP-COT control scheme. The device operates at a typically 1.2MHz switching frequency. Based on the $V_{IN}/V_{OUT}$ ratio, a simple circuit sets the required on-time for the high-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current at PWM state.

## Under-Voltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, under-voltage lockout is implemented that shuts down the device when input voltage lower than $V_{UVLO}$ (when $V_{IN}$ voltage falls) with 300mV (TYP) hysteresis. When the input voltage is higher than 2.55V (TYP), the device will recover to normal operation.

## Soft-Start and Pre-Biased Output

A 1.3ms internal soft-start circuit is included to prevent input inrush current and input voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage ($V_{REF}$ = 0.6V) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The SGMM2060 is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turning on, a bias on the output is likely to exist due to other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output voltage cannot drop too much during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device cannot be able to start up properly. The output ramp is automatically initiated to the bias voltage and ramps up to the nominal output value.

## Device Enable and Disable

The SGMM2060 is enabled by setting the EN pin input to higher than 1.2V (TYP). It is disabled when EN pin falls lower than 0.4V (TYP). If the device is enabled, the internal power stage starts switching and regulates the output voltage to the setting point voltage. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. The output discharge FET is turned on.

## Power Good Output (PG)

The SGMM2060 has a power good output. The PG pin is pulled to high-level once FB voltage reaches 90% of the reference voltage, and is driven low once FB voltage falls below typically 85% of the reference voltage. If the FB voltage is higher than 115% of the reference voltage, the PG pin becomes low, then the FB voltage is reduced to 110% of the reference voltage, and the PG pin is pulled to the high-level. The PG pin is an open-drain output with internal pull-up resistor connected to $V_{IN}$. It is recommended that the sink current should not exceed 1mA. There is a 105μs delay between when $V_{FB}$ reaches PG threshold to when the PG pin is pulled to high. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

**Table 1. PG Output State in Different Conditions**

| Reason | Conditions | PG State | |
|---|---|---|---|
| | | High | Low |
| FB Voltage | EN = High, $V_{PG\_OV} \geq V_{FB} \geq V_{PG}$ | √ | |
| | EN = High, $V_{FB} < V_{PG}$ | | √ |
| | EN = High, $V_{FB} > V_{PG\_OV}$ | | √ |
| Shutdown by EN | EN = Low | | √ |
| Thermal Shutdown | $T_J > T_{SD}$ | | √ |
| UVLO (1) | $1.4V < V_{IN} < V_{UVLO}$ | | √ |
| Power Supply Removal (1) | $V_{IN} \leq 1.4V$ | Uncertain | |

NOTE: 1. PG pin is connected to VIN pin with an external 570kΩ resistor.

## DETAILED DESCRIPTION (continued)

### Low Dropout Operation (100% Duty Cycle)

When the input voltage gradually drops to the regulation output voltage, the SGMM2060 can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 1:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times R_{PWM\_ON} \quad (1)$$

where:

$V_{IN\_MIN}$ is minimum input voltage to maintain output voltage in regulation.

$I_{OUT\_MAX}$ is maximum output current.

$R_{PWM\_ON}$ is PWM on, resistance from VIN to VOUT

### Current Limit and Hiccup Mode Short-Circuit Protection

The switch current limit avoids high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The SGMM2060 keeps sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to reduce the inductor current until the current is lower than low-side valley current limit threshold.

If the current limit persists uninterrupted for more than 16 cycles, the device stops switching and turns the output discharge circuit on. A new soft-start is initiated automatically (hiccup) after 1.3ms (TYP). The hiccup repeats until the overload or short-circuit fault is cleared.

### Output Over-Voltage Protection (OVP)

The device contains an over-voltage protection circuit to avoid high overshoots of the output voltage during operation. To minimize the overshoots, the device monitors the FB pin voltage and compares it to the internal OVP threshold. OVP is triggered while the FB voltage rising above 115% of reference voltage, and is released while the FB voltage falls below typically 110% of reference voltage. When the FB voltage drops below the OVP threshold, the high-side MOSFET can be turned on again in the next cycle.

### Output Discharge Function

If the device is in any of the following states: UVLO, shutdown by EN, OTP, an internal output discharge FET is turned on and discharges the output through the SW pin smoothly, the resistance of discharge FET is about 140Ω (TYP).

### Thermal Shutdown

Thermal protection is designed to protect the die against over-heating damage. If the junction temperature exceeds $T_{SD}$ threshold, the switching stops and the device shuts down. Automatic recovery with a soft-start will begin when the junction temperature drops below the +135℃ falling threshold.

# APPLICATION INFORMATION

In this section, power supply design with the SGMM2060 synchronous Buck power module and selection of the external components will be explained based on the typical application that is applicable for various input and output voltage combinations.

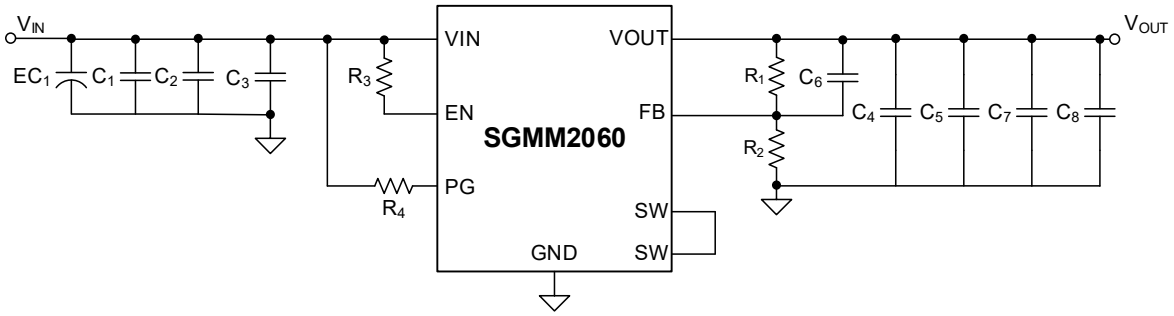



**Figure 3. SGMM2060 Circuit**

## Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 3. The selected components are given in Table 3.

**Table 2. Design Parameters for the Application Example**

| Design Parameter | Example Value |
|---|---|
| Input Voltage | 2.7V to 5.5V |
| Output Voltage | 0.9V |
| Output Current | ≤ 6A |

**Table 3. Selected Components for the Design Example**

| Ref | Description | Manufacturer |
|---|---|---|
| U1 | SGMM2060,<br>2.7V to 5.5V Input, 6A<br>Synchronous Buck power module,<br>LGA-3×3-20L | SGM |
| $EC_1$ | NS | NS |
| $C_1$, $C_2$ | 10μF,10V,10%,0603, X5R | muRata |
| $C_3$ | 0.1μF,16V,10%,0603,X7R | muRata |
| $C_4$, $C_5$, $C_7$, $C_8$ | 22μF, 16V, X5R, 0805, Ceramic | muRata |
| $C_6$ | NS | NS |
| $R_1$ | 59.8kΩ, ±1%, 0603 | Standard |
| $R_2$ | 120kΩ, ±1%, 0603 | Standard |
| $R_3$, $R_4$ | 100kΩ, 1%, 0603 | Standard |

NOTE: If the long input power cable is used, or the input voltage is on/off by air-break switch, $EC_1$ should be installed.

## Input Capacitor Selection ($C_{IN}$)

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. In most cases, two 22μF input capacitor is recommended, a larger value reduces input voltage ripple and improves system stability. Usually a 0.1μF low ESR ceramic capacitor needs to be connected between the VIN and GND pins as closely as possible.

## Output Capacitor Selection ($C_{OUT}$)

The architecture of the SGMM2060 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep the resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Bias voltage can cause significant capacitance drops in the ceramic capacitors. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value. $C_{OUT}$ = 3 × 22μF is the recommended values for the typical application.

## Output Voltage Setting

Use Equation 2 to select the $R_1/R_2$ resistor divider to set the $V_{OUT}$. The parasitic capacitance of the FB pin and $R_1$ form a low-pass filter, which can effectively filter out high-frequency interference input from the FB pin. However, it also adds a pole to the control loop, and if the frequency of this pole is too low, the stability of the system will be reduced.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

## APPLICATION INFORMATION (continued)

The recommended resistors values for common output voltages are listed in Table 4.

**Table 4. Resistor Values for Common Output Voltages**

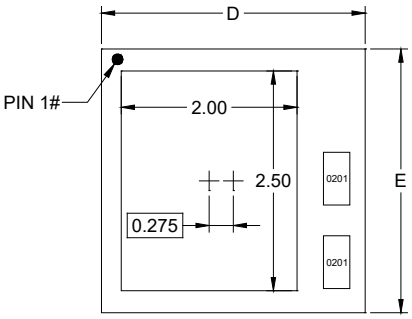
| $V_{OUT}$ (V) | $R_1$ (kΩ) | $R_2$ (kΩ) |
|---|---|---|
| 0.9 | 60.4 (1%) | 121 (1%) |
| 1.2 | 100 (1%) | 100 (1%) |
| 1.8 | 200 (1%) | 100 (1%) |
| 3.3 | 390 (1%) | 86.6 (1%) |

### Load Transient Optimization

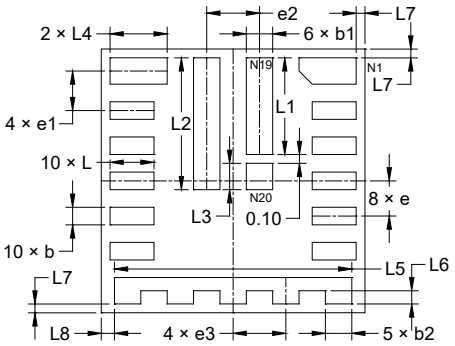
If it is necessary to reduce the drop of output voltage at load transient, the response speed of the system can be improved by increasing the $C_{FF}$ ($C_6$) capacitance value. However, excessive $C_{FF}$ ($C_6$) capacitance will reduce the stability of the system, which can be compensated by increasing the output capacitance value.

# PACKAGE OUTLINE DIMENSIONS

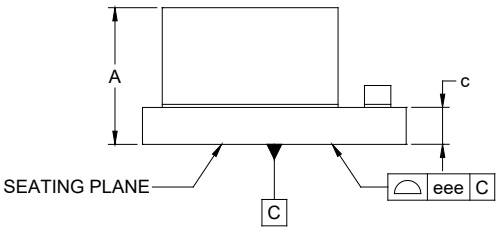
## EMSIP-3×3-20L



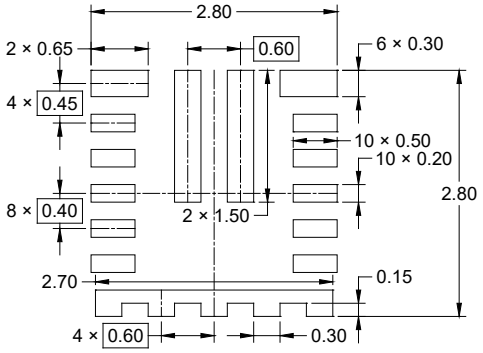

TOP VIEW




BOTTOM VIEW




SIDE VIEW




**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | 1.555 | 1.720 |
| b | 0.150 | - | 0.250 |
| b1 | 0.250 | - | 0.350 |
| b2 | 0.250 | - | 0.350 |
| c | | 0.420 REF | |
| D | 2.900 | - | 3.100 |
| E | 2.900 | - | 3.100 |
| e | | 0.400 BSC | |
| e1 | | 0.450 BSC | |
| e2 | | 0.600 BSC | |
| e3 | | 0.600 BSC | |
| L | 0.450 | - | 0.550 |
| L1 | 1.050 | - | 1.150 |
| L2 | 1.450 | - | 1.550 |
| L3 | 0.250 | - | 0.350 |
| L4 | 0.600 | - | 0.700 |
| L5 | 2.650 | - | 2.750 |
| L6 | | 0.150 REF | |
| L7 | 0.050 | - | 0.150 |
| L8 | 0.100 | - | 0.200 |
| eee | | 0.100 | |

NOTE: This drawing is subject to change without notice.