TLV431x-Q1 Low-Voltage Adjustable Precision Shunt Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Low-Voltage Operation, V_{REF} = 1.24 V
- Adjustable Output Voltage, V_O = V_{REF} to 6 V
- Reference Voltage Tolerances at 25°C
  - 0.5% for TLV431B
  - 1% for TLV431A
- Typical Temperature Drift
  - 11 mV (–40°C to 125°C)
- Low Operational Cathode Current, 80 µA Typ
- 0.25-Ω Typical Output Impedance
- See TLVH431 and TLVH432 for:
  - Wider V_{KA} (1.24 V to 18 V) and I_K (80 mA)
  - Multiple Pinouts for SOT-23-3 and SOT-89 Packages

2 Applications

- Adjustable Voltage and Current Referencing
- Secondary Side Regulation in Flyback SMPSs
- Zener Replacement
- Voltage Monitoring
- Comparator with Integrated Reference

3 Description

The TLV431 device is a low-voltage 3-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to 1.24V on stand alone mode or any value between V_{REF} (1.24 V) and 6 V with two external resistors (see Figure 23). These devices operate from a lower voltage (1.24 V) than the widely used TL431 and TL1431 shunt-regulator references.

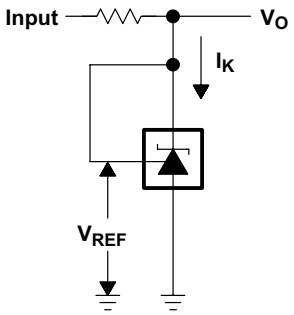
When used with an optocoupler, the TLV431 device is an ideal voltage reference in isolated feedback circuits for 3-V to 3.3-V switching-mode power supplies. These devices have a typical output impedance of 0.25 Ω. Active output circuitry provides a very sharp turn-on characteristic, making them excellent replacements for low-voltage Zener diodes in many applications, including on-board regulation and adjustable power supplies.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
TLV431x-Q1	SOT-23 (3)	2.90 mm x 1.30 mm
	SOT-23 (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Thermal Information ... 4
6.4 Recommended Operating Conditions ... 4
6.5 Electrical Characteristics for TLV431A-Q1 ... 5
6.6 Electrical Characteristics for TLV431B-Q1 ... 6
6.7 Typical Characteristics ... 7
7 Parameter Measurement Information ... 15
8 Detailed Description ... 16
8.1 Overview ... 16
8.2 Functional Block Diagram ... 16
8.3 Feature Description ... 16
8.4 Device Functional Modes ... 17
9 Applications and Implementation ... 18
9.1 Application Information ... 18
9.2 Typical Applications ... 19
10 Power Supply Recommendations ... 23
11 Layout ... 23
11.1 Layout Guidelines ... 23
11.2 Layout Example ... 23
12 Device and Documentation Support ... 24
12.1 Related Links ... 24
12.2 Receiving Notification of Documentation Updates 24
12.3 Community Resources ... 24
12.4 Trademarks ... 24
12.5 Electrostatic Discharge Caution ... 24
12.6 Glossary ... 24
13 Mechanical, Packaging, and Orderable Information ... 24

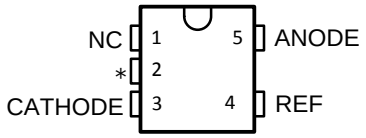
4 Revision History

Changes from Original (December 2008) to Revision A **Page**

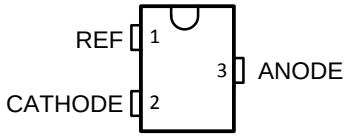
- Added Automotive AEC-Q100 feature ... 1
- Added New typical curves ... 15

5 Pin Configuration and Functions

DBV (SOT-23-5) PACKAGE
(TOP VIEW)



DBZ (SOT-23-3) PACKAGE
(TOP VIEW)



NC−No internal connection
* For TLV431A: NC − No internal connection
* For TLV431B: Pin 2 is attached to Substrate and must be connected to ANODE or left open.

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	DBV		
CATHODE	2	3	I/O	Shunt Current/Voltage input
REF	1	4	I	Threshold relative to common anode
ANODE	3	5	O	Common pin, normally connected to ground
NC	—	1	I	No Internal Connection
*	—	2	I	Substrate Connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{KA}	Cathode voltage(2)		7	V
I_K	Continuous cathode current range	–20	20	mA
I_{ref}	Reference current range	–0.05	3	mA
	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the anode terminal, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Thermal Information

THERMAL METRIC(1)		TLV431x		UNIT
		DBV	DBZ	
		5 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	206	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	131	76	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{KA}	Cathode voltage		V_{REF}	6	V
I_K	Cathode current		0.1	15	mA
T_A	Operating free-air temperature range	TLV431x-Q1	–40	125	°C

6.5 Electrical Characteristics for TLV431A-Q1

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV431AQ			UNIT
				MIN	TYP	MAX	
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10 mA	T_A = 25°C	1.228	1.24	1.252	V
			T_A = full range(1) (see Figure 22)	1.209		1.271	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range(2)	$V_{KA} = V_{REF}$, I_K = 10 mA(1) (see Figure 22)			11	31	mV
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6 V, I_K = 10 mA (see Figure 23)			–1.5	–2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 23)			0.15	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range(2)	I_K = 10 mA, R1 = 10 kΩ, R2 = open(1) (see Figure 23)			0.15	0.5	µA
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see Figure 22)			55	100	µA
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6 V (see Figure 24)			0.001	0.1	µA
$\lvert z_{KA} \rvert$	Dynamic impedance(3)	$V_{KA} = V_{REF}$, f ≤ 1 kHz, I_K = 0.1 mA to 15 mA (see Figure 22)			0.25	0.4	Ω

(1) Full temperature range is –40°C to 125°C for TLV431x-Q1.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.

αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as $\left|z_{ka}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors (see Figure 23), the total dynamic impedance of the circuit is defined as:

$$\left|z_{ka}\right|' = \frac{\Delta V}{\Delta I} \approx \left|z_{ka}\right| \times \left(1 + \frac{R1}{R2}\right)$$

6.6 Electrical Characteristics for TLV431B-Q1

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV431BQ			UNIT
				MIN	TYP	MAX	
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10 mA	T_A = 25°C	1.234	1.24	1.246	V
			T_A = full range[1] (see Figure 22)	1.221		1.265	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range[2]	$V_{KA} = V_{REF}$, I_K = 10 mA[1] (see Figure 22)			11	31	mV
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6 V, I_K = 10 mA (see Figure 23)			–1.5	–2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 23)			0.1	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range[2]	I_K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 23)			0.15	0.5	µA
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see Figure 22)			55	100	µA
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6 V (see Figure 24)			0.001	0.1	µA
$\|z_{KA}\|$	Dynamic impedance[3]	$V_{KA} = V_{REF}$, f ≤ 1 kHz, I_K = 0.1 mA to 15 mA (see Figure 22)			0.25	0.4	Ω

(1) Full temperature range is –40°C to 125°C for TLV431x-Q1.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.

αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors (see Figure 23), the total dynamic impedance of the circuit is defined as:

$$|z_{ka}|' = \frac{\Delta V}{\Delta I} \approx |z_{ka}| \times \left(1 + \frac{R1}{R2}\right)$$

6.7 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

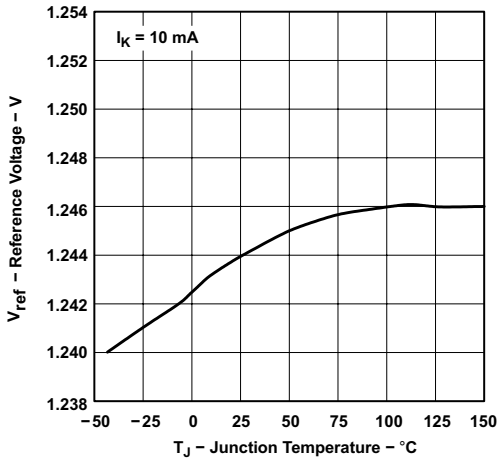


Figure 1. Reference Voltage vs Junction Temperature

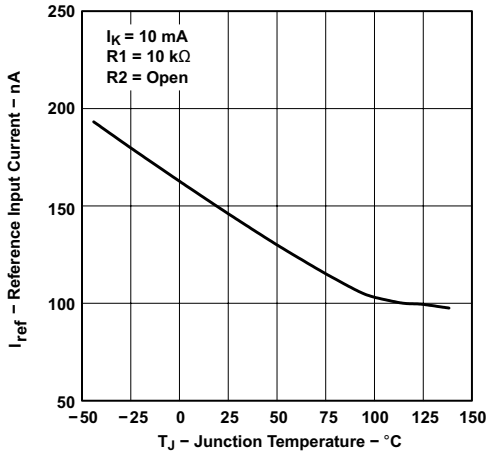


Figure 2. Reference Current vs Free- air Temperature (TLV431A)

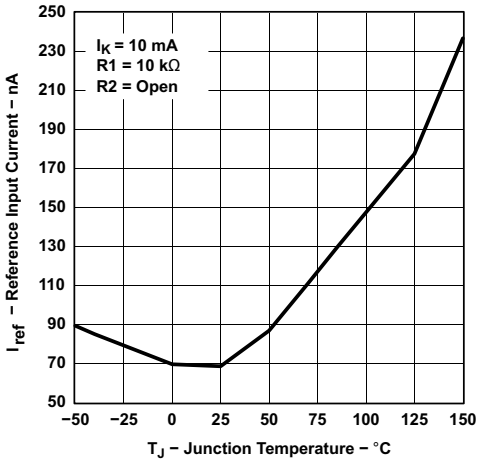


Figure 3. Reference Input Current vs Junction Temperature (for TLV431B)

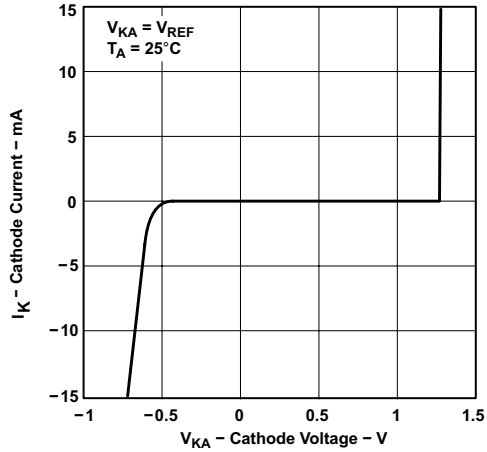


Figure 4. Cathode Current vs Cathode Voltage

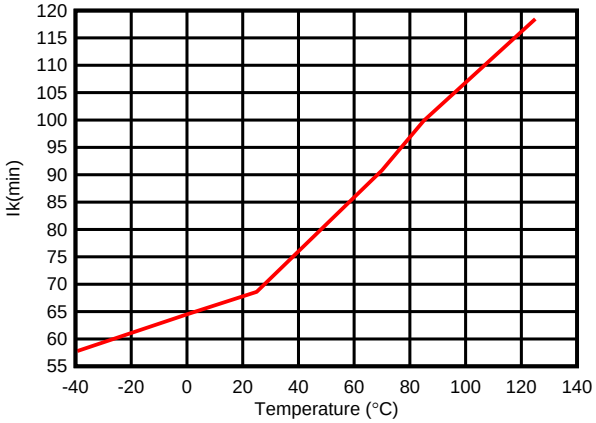


Figure 5. Minimum Cathode Current (µA) vs Temperature

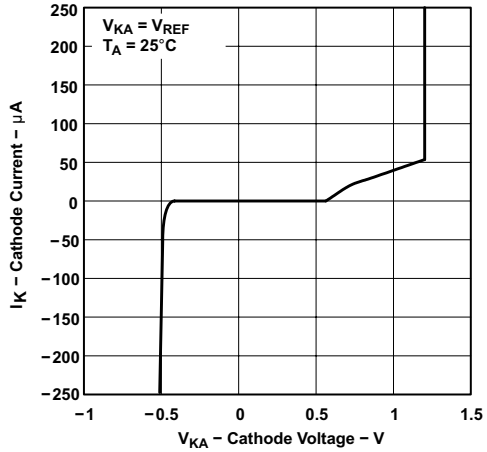


Figure 6. Cathode Current vs Cathode Voltage

Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

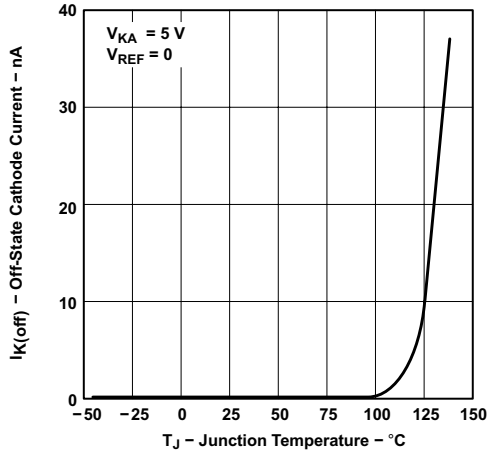


Figure 7. Off-State Cathode Current vs Junction Temperature for TLV431A

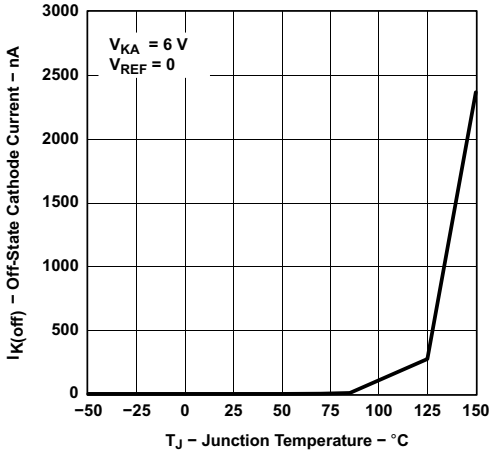


Figure 8. Off-State Cathode Current vs Junction Temperature for TLV431B

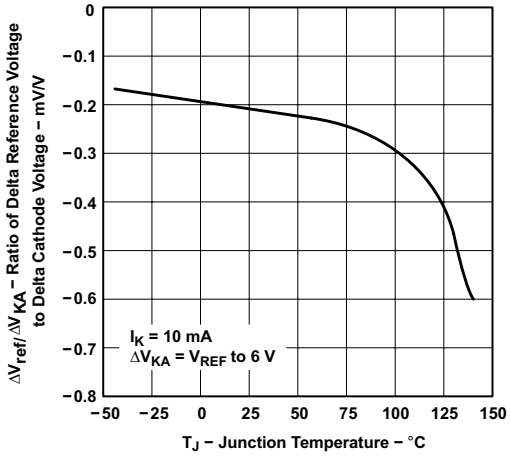


Figure 9. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature for TLV431A

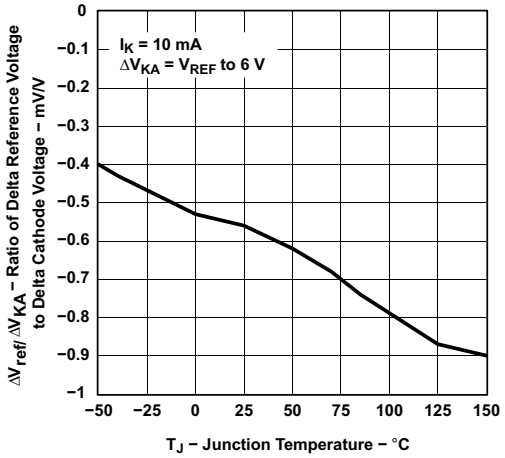
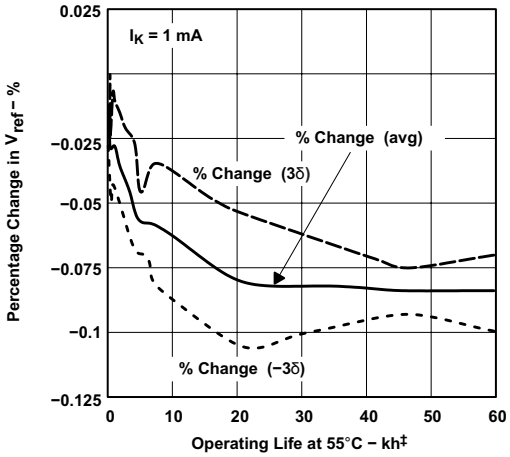


Figure 10. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature (for TLV431B)

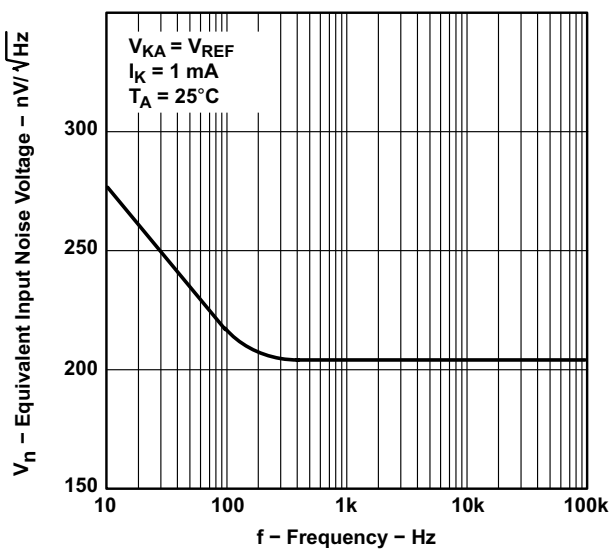


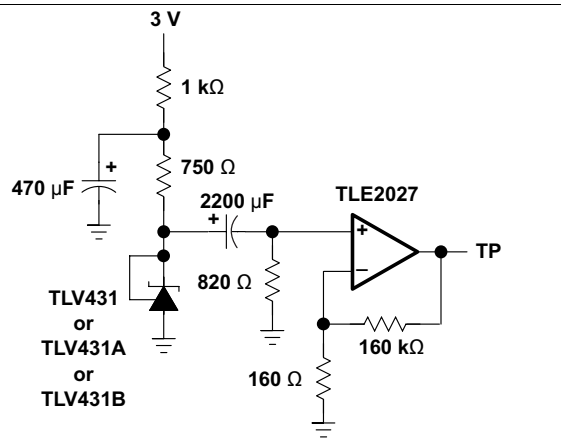
‡ Extrapolated from life-test data taken at 125°C; the activation energy assumed is 0.7 eV.

Figure 11. Percentage Change in V_{REF} vs Operating Life at 55°C

Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.



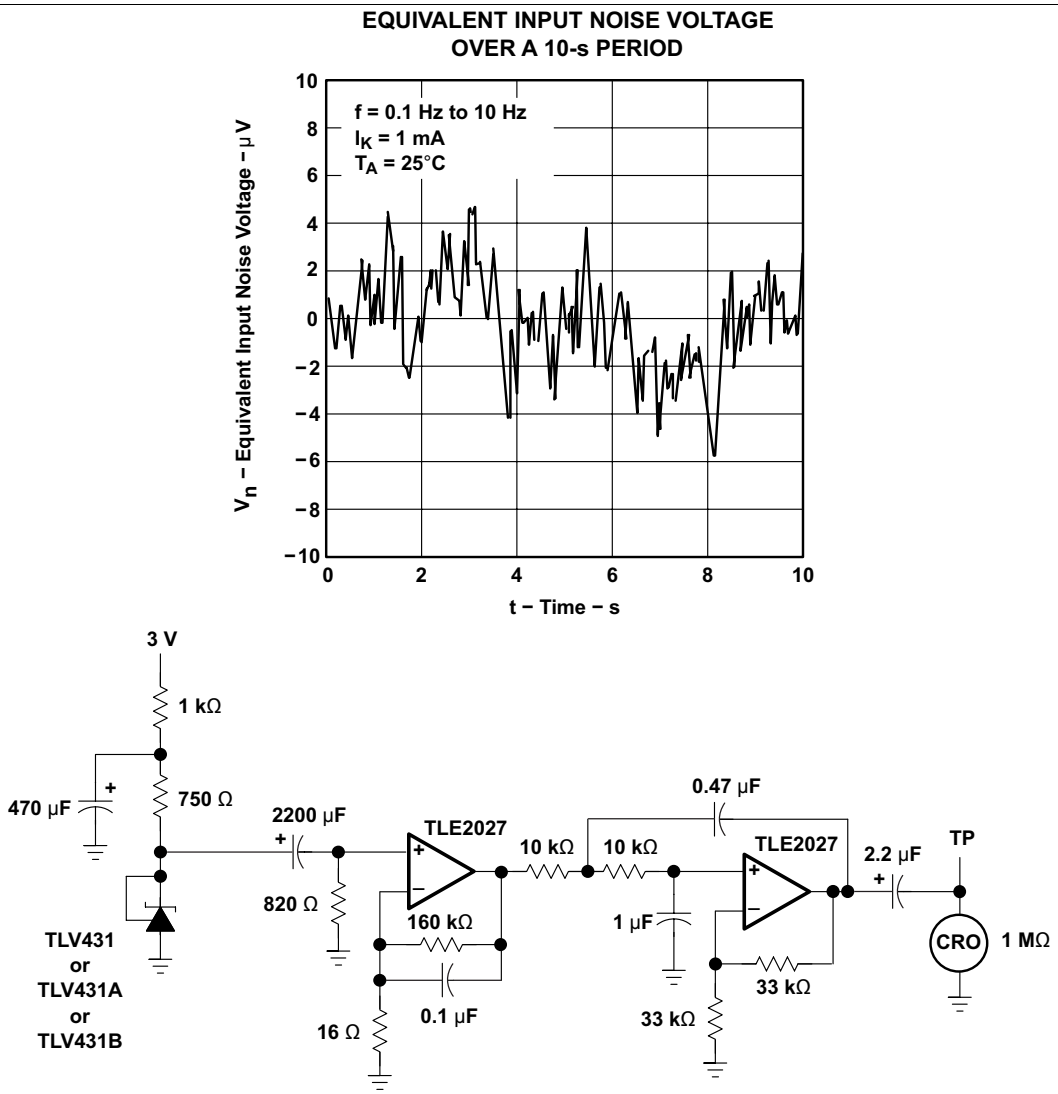


TEST CIRCUIT FOR EQUIVALENT INPUT NOISE VOLTAGE

Figure 12. Equivalent Input Noise Voltage

Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

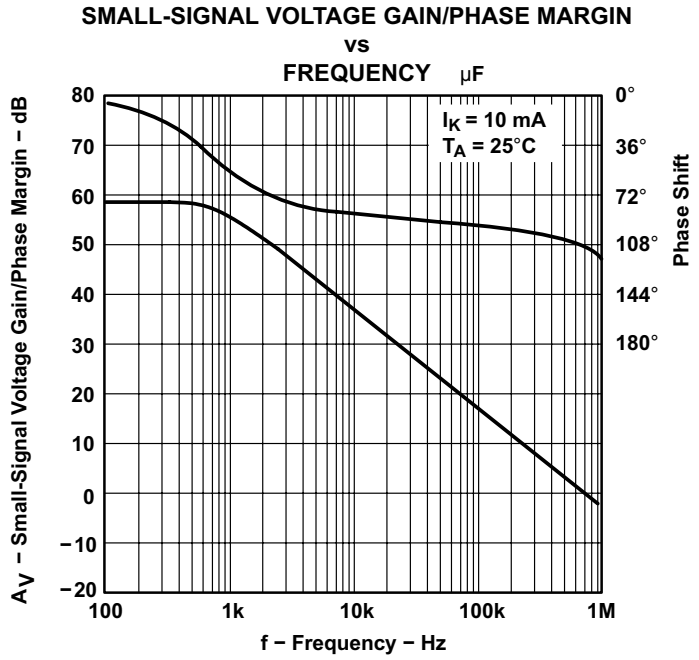


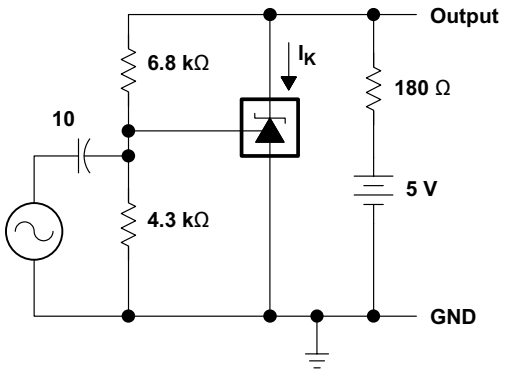
TEST CIRCUIT FOR 0.1-Hz TO 10-Hz EQUIVALENT NOISE VOLTAGE

Figure 13. Equivalent Noise Voltage over a 10s Period

Typical Characteristics (continued)

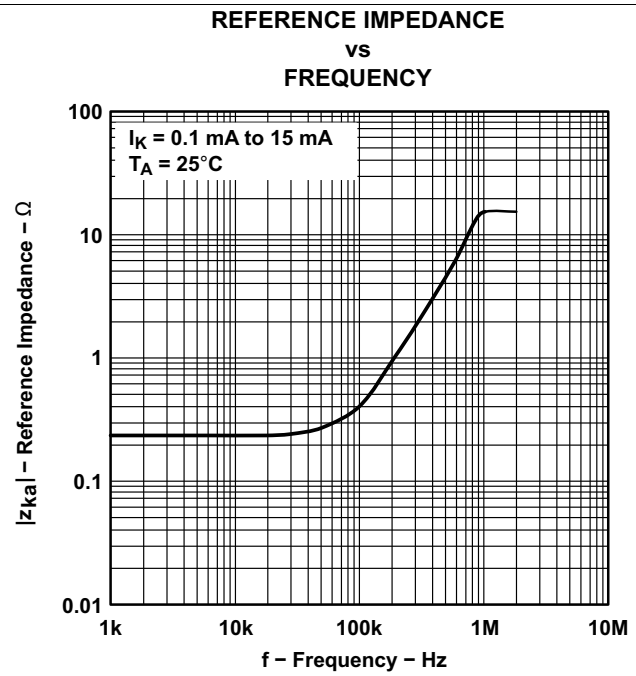
Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

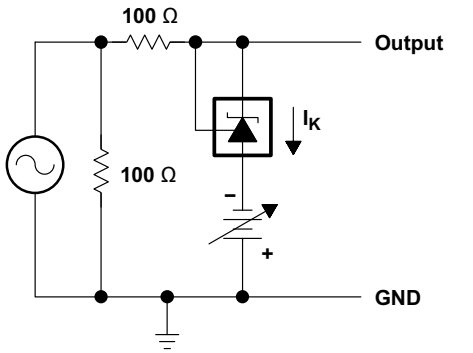




TEST CIRCUIT FOR VOLTAGE GAIN AND PHASE MARGIN

Figure 14. Voltage Gain and Phase Margin





TEST CIRCUIT FOR REFERENCE IMPEDANCE

Figure 15. Reference Impedance vs Frequency

Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

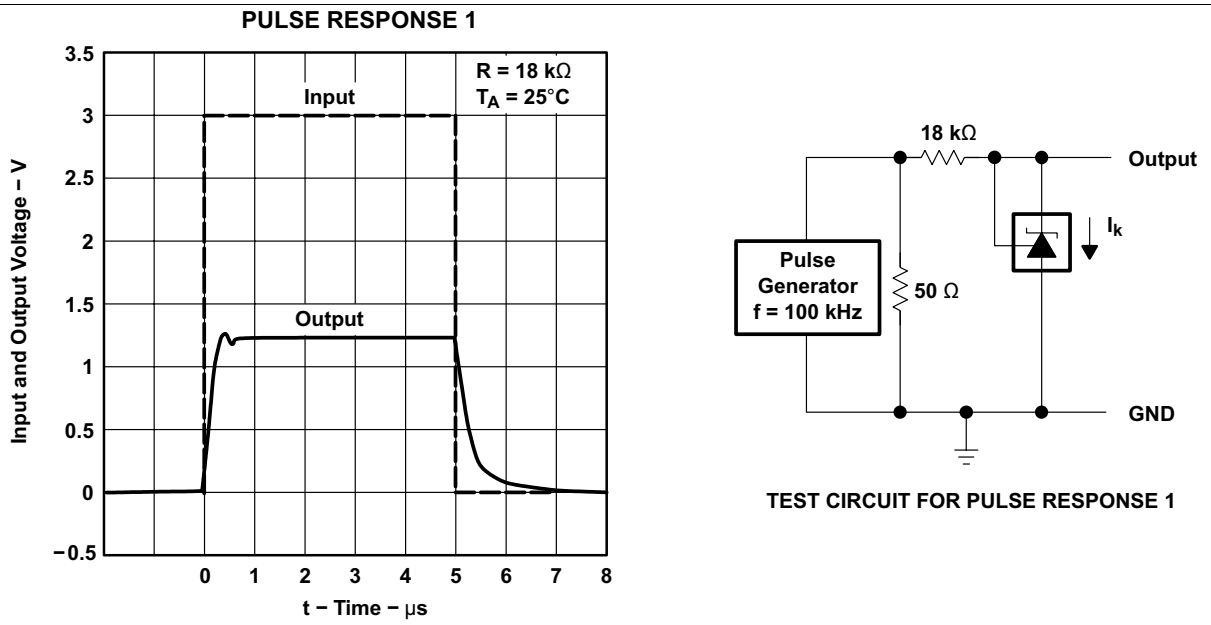


Figure 16. Pulse Response 1

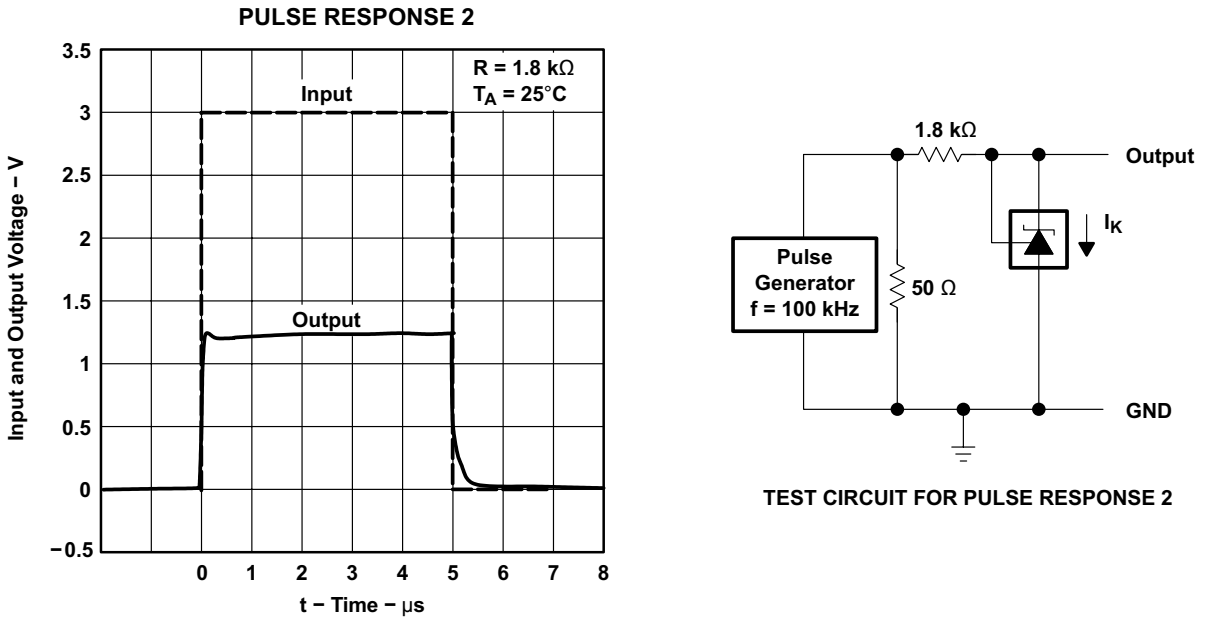
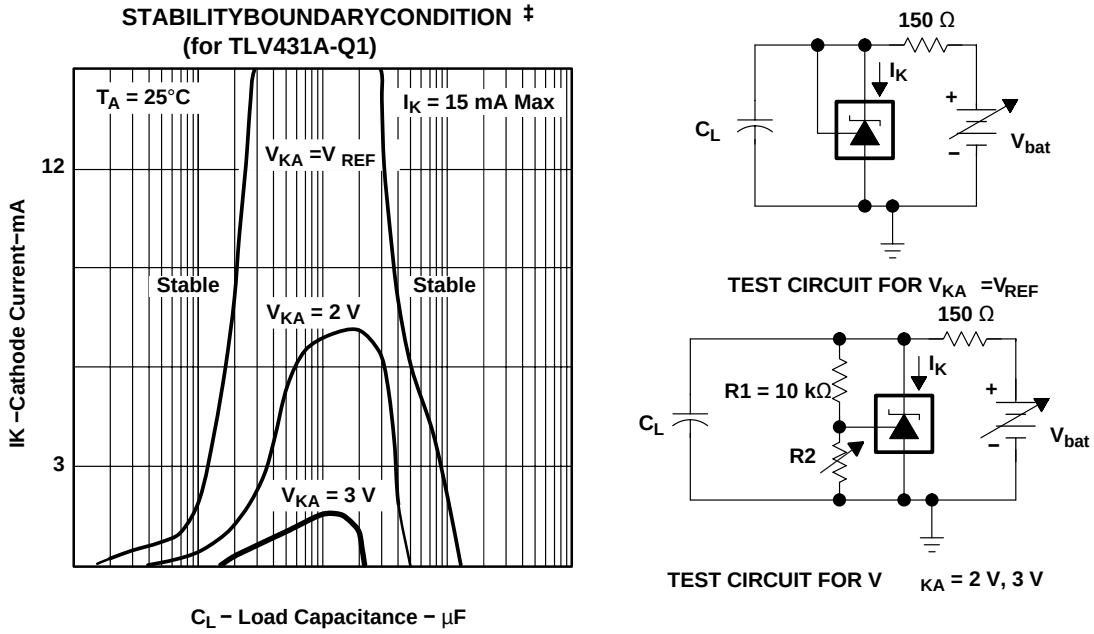


Figure 17. Pulse Response 2

Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.



‡ The areas under the curves represent conditions that may cause the device to oscillate. For V_{KA} = 2-V and 3-V curves, R2 and V_{bat} were adjusted to establish the initial V_{KA} and I_K conditions with C_L = 0. V_{bat} and C_L then were adjusted to determine the ranges of stability.

Figure 18. Stability Boundary Conditions

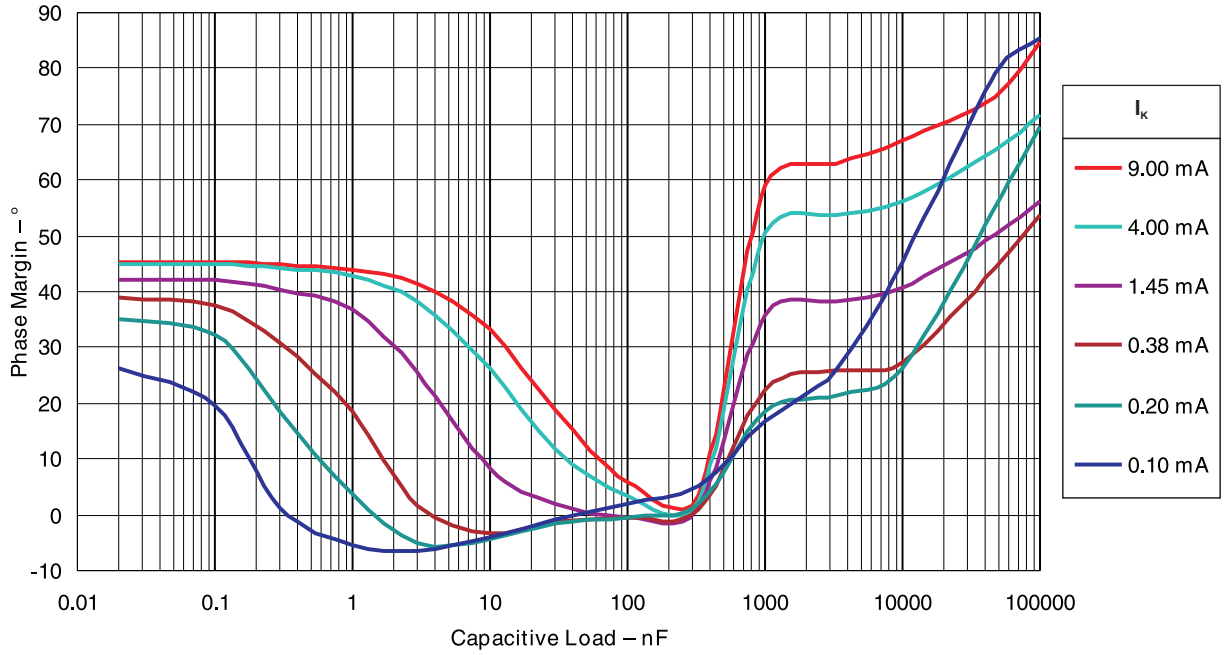


Figure 19. Phase Margin vs Capacitive Load V_{KA} = V_{REF} (1.25 V), T_A= 25°C (For TLV431B-Q1)

Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

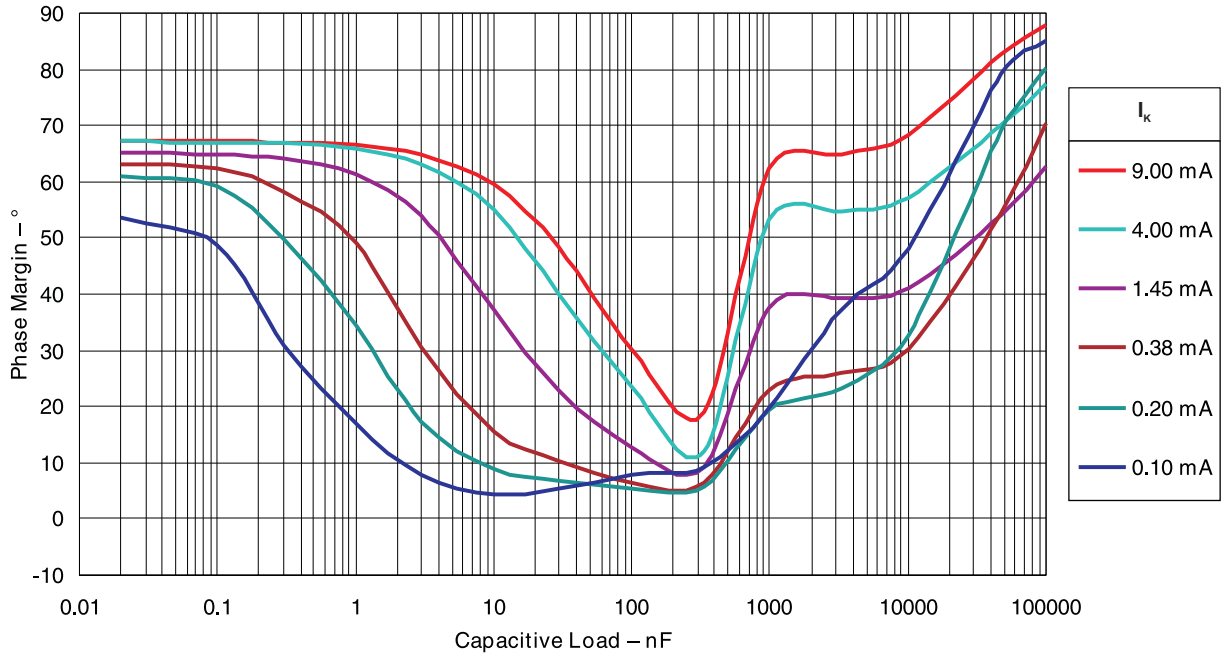


Figure 20. Phase Margin vs Capacitive Load V_{KA} = 2.50 V, T_A= 25°C (For TLV431B-Q1)

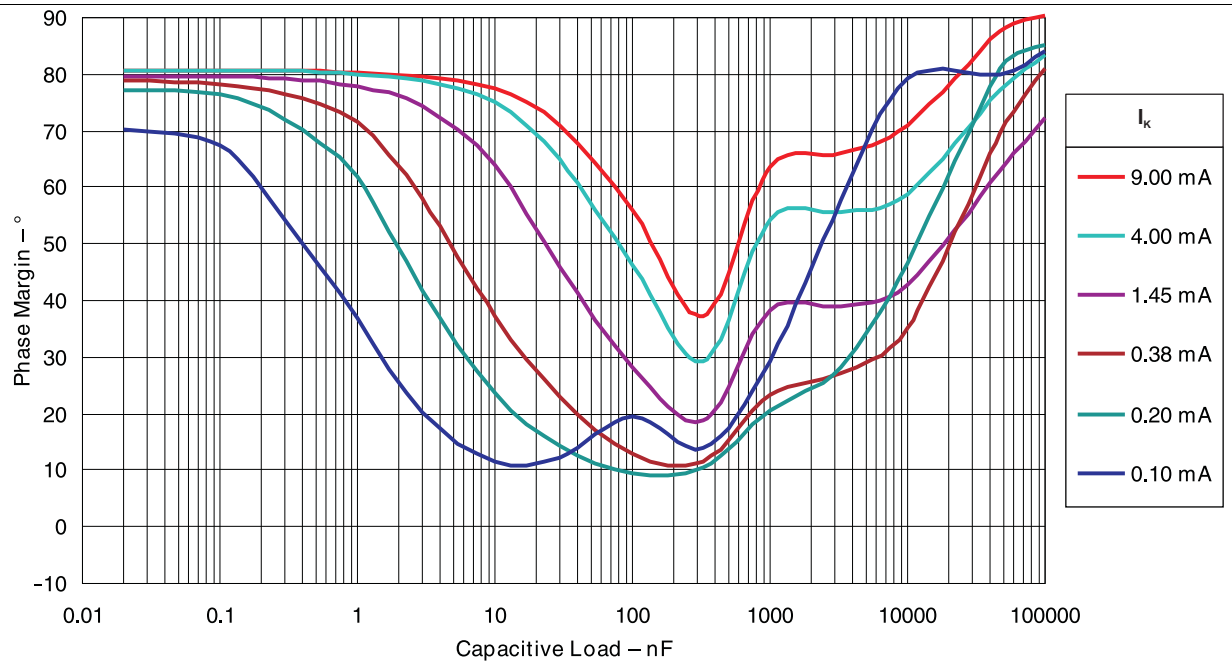


Figure 21. Phase Margin vs Capacitive Load V_{KA} = 5.00 V, T_A= 25°C (For TLV431B-Q1)

7 Parameter Measurement Information

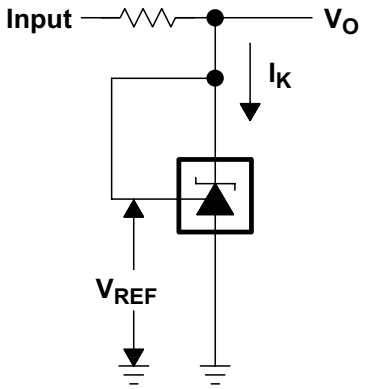


Figure 22. Test Circuit for $V_{KA} = V_{REF}$, $V_O = V_{KA} = V_{REF}$

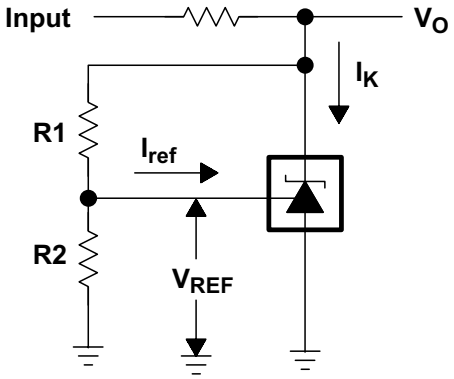


Figure 23. Test Circuit for $V_{KA} > V_{REF}$, $V_O = V_{KA} = V_{REF} \times (1 + R1/R2) + I_{ref} \times R1$

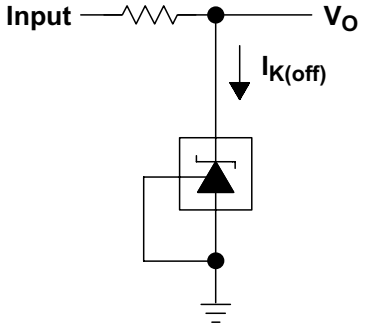


Figure 24. Test Circuit for $I_{K(off)}$

8 Detailed Description

8.1 Overview

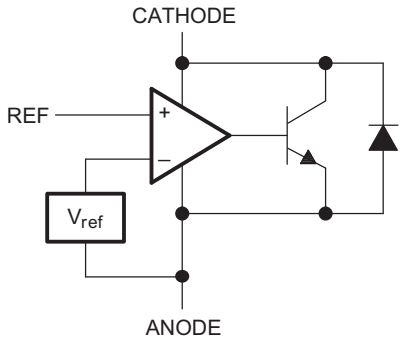
TLV431 is a low power counterpart to TL431, having lower reference voltage (1.24 V vs 2.5 V) for lower voltage adjustability and lower minimum cathode current ($I_{k(min)}$=100 µA vs 1 mA). Like TL431, the TLV431 is used in conjunction with it's key components to behave as a single voltage reference, error amplifier, voltage clamp or comparator with integrated reference.

TLV431 can be operated and adjusted to cathode voltages from 1.24V to 6V, making this part optimum for a wide range of end equipments in industrial, auto, telecom & computing. In order for this device to behave as a shunt regulator or error amplifier, > 100 µA (I_{min}(max)) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage.

Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.5%, and 1%. These reference options are denoted by B (0.5%) and A (1.0%) after the TLV431x-Q1.

The TLV431x-Q1 devices are characterized for operation from –40°C to 125°C.

8.2 Functional Block Diagram



8.3 Feature Description

TLV431 consists of an internal reference and amplifier that outputs a sink current base on the difference between the reference pin and the virtual internal pin. The sink current is produced by an internal darlington pair.

When operated with enough voltage headroom (≥ 1.24 V) and cathode current (Ika), TLV431 forces the reference pin to 1.24 V. However, the reference pin can not be left floating, as it needs I_{ref} ≥ 0.5 µA (please see the *Functional Block Diagram*). This is because the reference pin is driven into an npn, which needs base current in order operate properly.

When feedback is applied from the Cathode and Reference pins, TLV431 behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo or error amplifying implementations in order for it to be in the proper linear region giving TLV431 enough gain.

Unlike many linear regulators, TLV431 is internally compensated to be stable without an output capacitor between the cathode and anode. However, if it is desired to use an output capacitor Figure 18 can be used as a guide to assist in choosing the correct capacitor to maintain stability.

8.4 Device Functional Modes

8.4.1 Open Loop (Comparator)

When the cathode/output voltage or current of TLV431 is not being fed back to the reference/input pin in any form, this device is operating in open loop. With proper cathode current (Ika) applied to this device, TLV431 will have the characteristics shown in Figure 6. With such high gain in this configuration, TLV431 is typically used as a comparator. With the reference integrated makes TLV431 the preferred choice when users are trying to monitor a certain level of a single signal.

8.4.2 Closed Loop

When the cathode/output voltage or current of TLV431 is being fed back to the reference/input pin in any form, this device is operating in closed loop. The majority of applications involving TLV431 use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished via resistive or direct feedback.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 25 shows the TLV431A, or TLV431B used in a 3.3-V isolated flyback supply. Output voltage V_O can be as low as reference voltage V_{REF} (1.24 V ± 1%). The output of the regulator, plus the forward voltage drop of the optocoupler LED (1.24 + 1.4 = 2.64 V), determine the minimum voltage that can be regulated in an isolated supply configuration. Regulated voltage as low as 2.7 Vdc is possible in the topology shown in Figure 25.

The 431 family of devices are prevalent in these applications, being designers go to choice for secondary side regulation. Due to this prevalence, this section will further go on to explain operation and design in both states of TLV431 that this application will see, open loop (Comparator + Vref) & closed loop (Shunt Regulator).

Further information about system stability and using a TLV431 device for compensation can be found in the application note *Compensation Design With TL431 for UCC28600,* SLUA671.

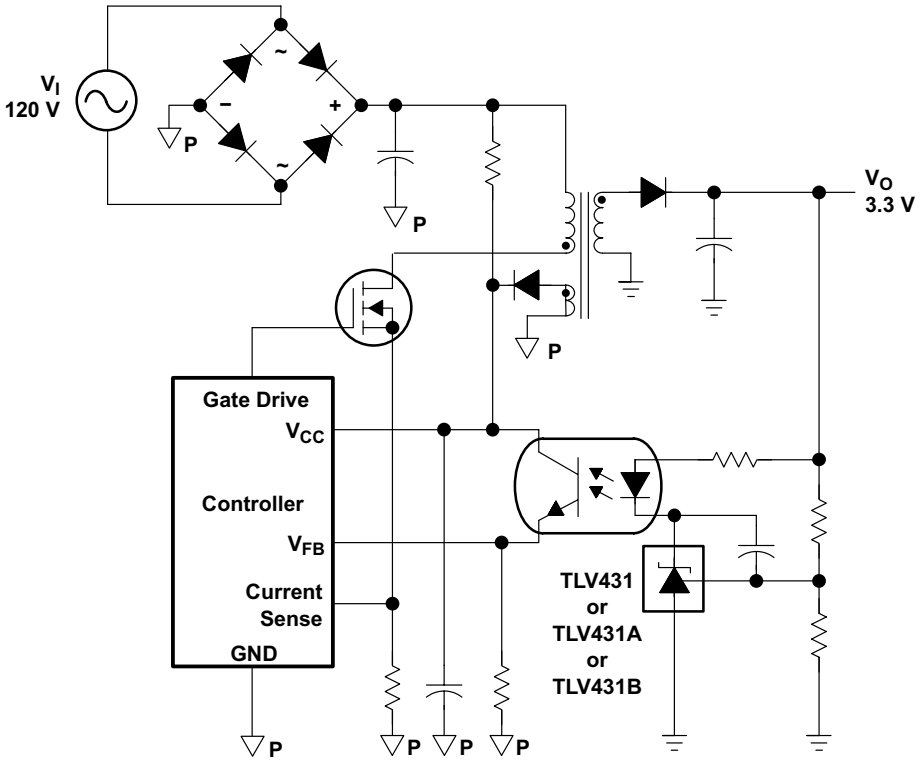


Figure 25. Flyback With Isolation Using TLV431, TLV431A, or TLV431B as Voltage Reference and Error Amplifier

9.2 Typical Applications

9.2.1 Comparator with Integrated Reference (Open Loop)

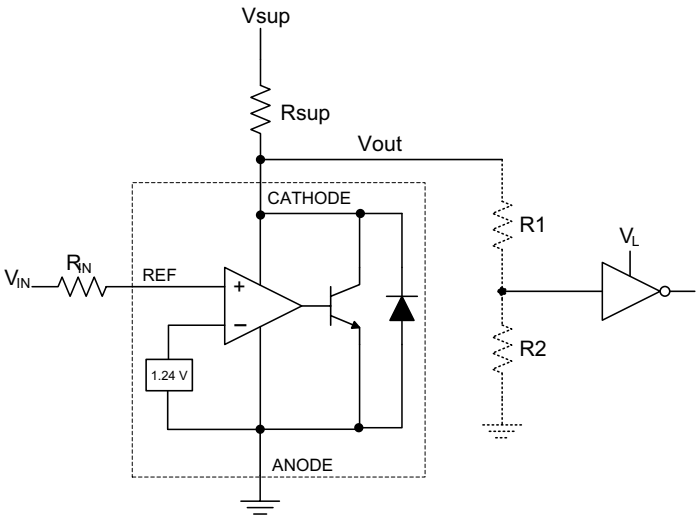


Figure 26. Comparator Application Schematic

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to 5 V
Input Resistance	10 kΩ
Supply Voltage	5 V
Cathode Current (Ik)	500 µA
Output Voltage Level	~1 V - Vsup
Logic Input Thresholds VIH/VIL	VL

9.2.1.2 Detailed Design Procedure

When using TLV431 as a comparator with reference, determine the following:

- Input voltage range
- Reference voltage accuracy
- Output logic input high and low level thresholds
- Current source resistance

9.2.1.2.1 Basic Operation

In the configuration shown in Figure 26 TLV431 will behave as a comparator, comparing the V_{ref} pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_k), TLV431 will have enough open loop gain to provide a quick response. With the TLV431's min Operating Current maximum (Imin) being 55 uA to 100 uA over temperature, operation below that could result in low gain, leading to a slow response.

9.2.1.2.2 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The internal virtual reference voltage will be within the range of 1.24V ±(0.5% or 1.0%) depending on which version is being used.

The more overdrive voltage provided, the faster the TLV431 will respond. This can be seen in figures Figure 27 and Figure 28, where it displays the output responses to various input voltages.

For applications where TLV431 is being used as a comparator, it is best to set the trip point to greater than the positive expected error (i.e. +1.0% for the A version). For fast response, setting the trip point to > 10% of the internal V_{ref} should suffice.

For minimal voltage drop or difference from Vin to the ref pin, it is recommended to use an input resistor < 10 kΩ to provide I_{ref}.

9.2.1.2.3 Output Voltage and Logic Input Level

In order for TLV431 to properly be used as a comparator, the logic output must be readable by the recieving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} & V_{IL}.

As seen in Figure 27, TLV431's output low level voltage in open-loop/comparator mode is ~1 V, which is sufficient for some 3.3V supplied logic. However, would not work for 2.5 V and 1.8 V supplied logic. In order to accommodate this a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low voltage logic device.

TLV431's output high voltage is approximately V_{sup} due to TLV431 being open-collector. If V_{sup} is much higher than the receiving logic's maximum input voltage tolerance, the output must be attenuated to accommodate the outgoing logic's reliability.

When using a resistive divider on the output, be sure to make the sum of the resistive divider (R1 & R2 in Figure 26) is much greater than R_{sup} in order to not interfere with TLV431's ability to pull close to V_{sup} when turning off.

9.2.1.2.3.1 Input Resistance

TLV431 requires an input resistance in this application in order to source the reference current (I_{ref}) needed from this device to be in the proper operating regions while turning on. The actual voltage seen at the ref pin will be $V_{ref}=V_{in}-I_{ref}*R_{in}$. Since I_{ref} can be as high as 0.5 µA it is recommended to use a resistance small enough that will mitigate the error that I_{ref} creates from V_{in}.

9.2.1.3 Application Curves

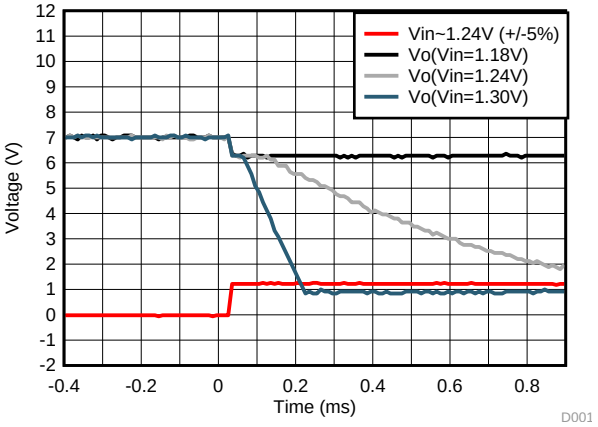


Figure 27. Output Response with Small Overdrive Voltages

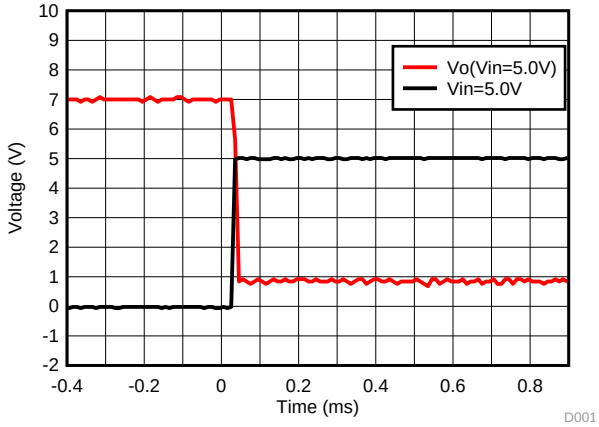


Figure 28. Output Response with Large Overdrive Voltage

9.2.2 Shunt Regulator/Reference

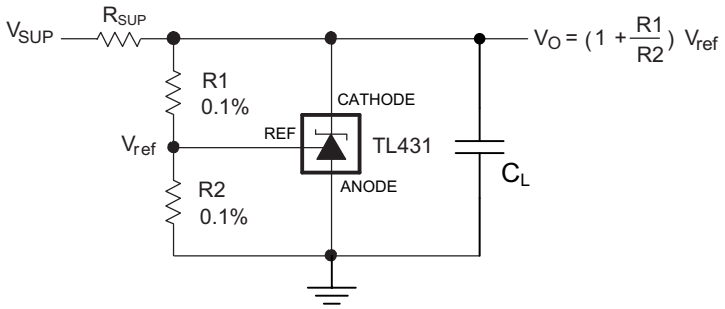


Figure 29. Shunt Regulator Schematic

9.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Reference Initial Accuracy	1.0%
Supply Voltage	6 V
Cathode Current (Ik)	1 mA
Output Voltage Level	1.24 V - 6 V
Load Capacitance	100 nF
Feedback Resistor Values and Accuracy (R1 & R2)	10 kΩ

9.2.2.2 Detailed Design Procedure

When using TLV431 as a Shunt Regulator, determine the following:

- Input voltage range
- Temperature range
- Total accuracy
- Cathode current
- Reference initial accuracy
- Output capacitance

9.2.2.2.1 Programming Output/Cathode Voltage

In order to program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in Figure 29, with R1 & R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in Figure 29. The cathode voltage can be more accuratel determined by taking in to account the cathode current:

$V_O=(1+R1/R2)*V_{ref}–I_{ref}*R1$

In order for this equation to be valid, TLV431 must be fully biased so that it has enough open loop gain to mitigate any gain error. This can be done by meeting the I_{min} spec denoted in *Recommended Operating Conditions* table.

9.2.2.2.2 Total Accuracy

When programming the output above unity gain (Vka=Vref), TLV431 is susceptible to other errors that may effect the overall accuracy beyond V_{ref}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ - Change in reference voltage over temperature
- ΔV_{ref} / ΔV_{KA} - Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ - Dynamic impedance, causing a change in cathode voltage with cathode current

Worst case cathode voltage can be determined taking all of the variables in to account. Application note SLVA445 assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

9.2.2.2.3 Stability

Though TLV431 is stable with no capacitive load, the device that receives the shunt regulator's output voltage could present a capacitive load that is within the TLV431 region of stability, shown in Figure 18. Also, designers may use capacitive loads to improve the transient response or for power supply decoupling.

9.2.2.3 Application Curves

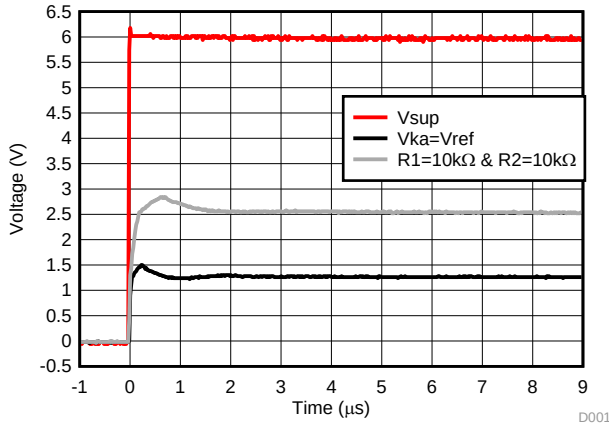


Figure 30. TLV431 Start-Up Response

10 Power Supply Recommendations

When using TLV431 as a Linear Regulator to supply a load, designers will typically use a bypass capacitor on the output/cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in Figure 18.

In order to not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed it's absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

11 Layout

11.1 Layout Guidelines

Place decoupling capacitors as close to the device as possible. Use appropriate widths for traces when shunting high currents to avoid excessive voltage drops.

11.2 Layout Example

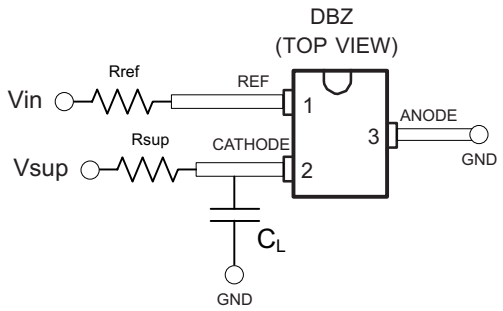


Figure 31. DBZ Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV431A-Q1	Click here	Click here	Click here	Click here	Click here
TLV431B-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VONQ	Samples
TLV431BQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOMQ	Samples
TLV431BQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOQQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV431A-Q1, TLV431B-Q1 :

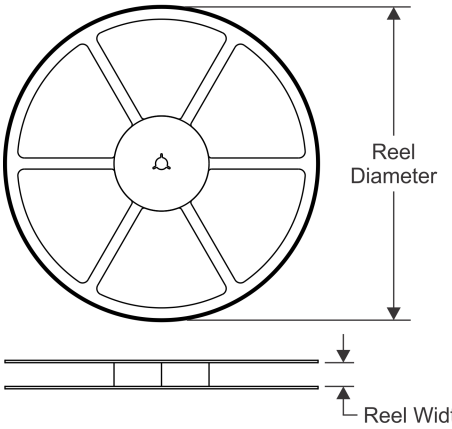
- Catalog: TLV431A, TLV431B

NOTE: Qualified Version Definitions:

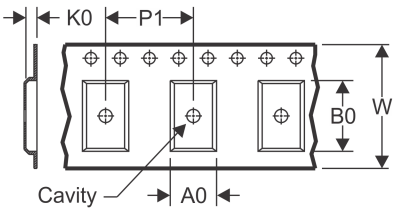
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

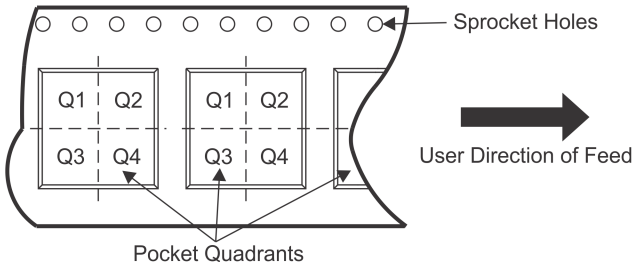


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



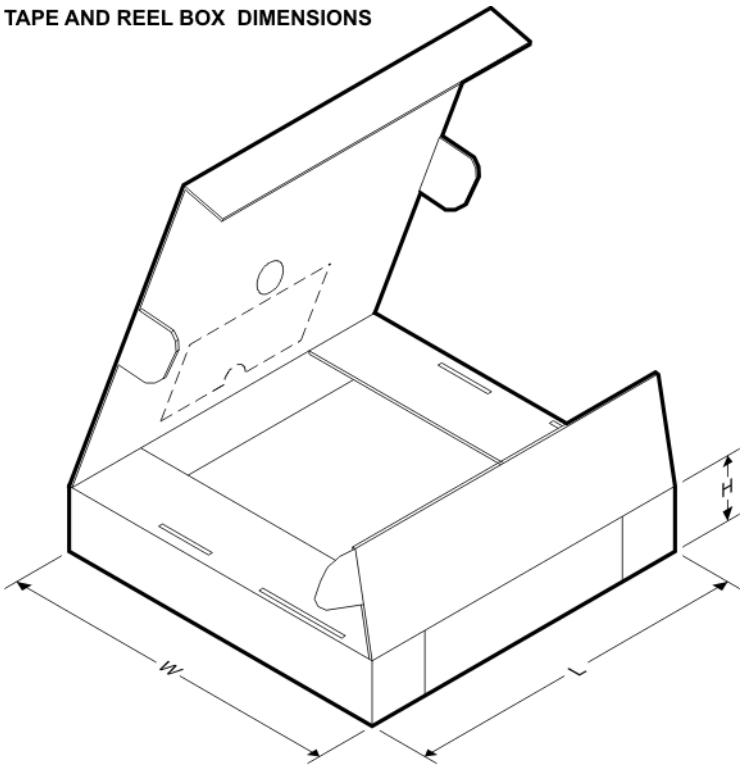
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431AQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

5-Jan-2021

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

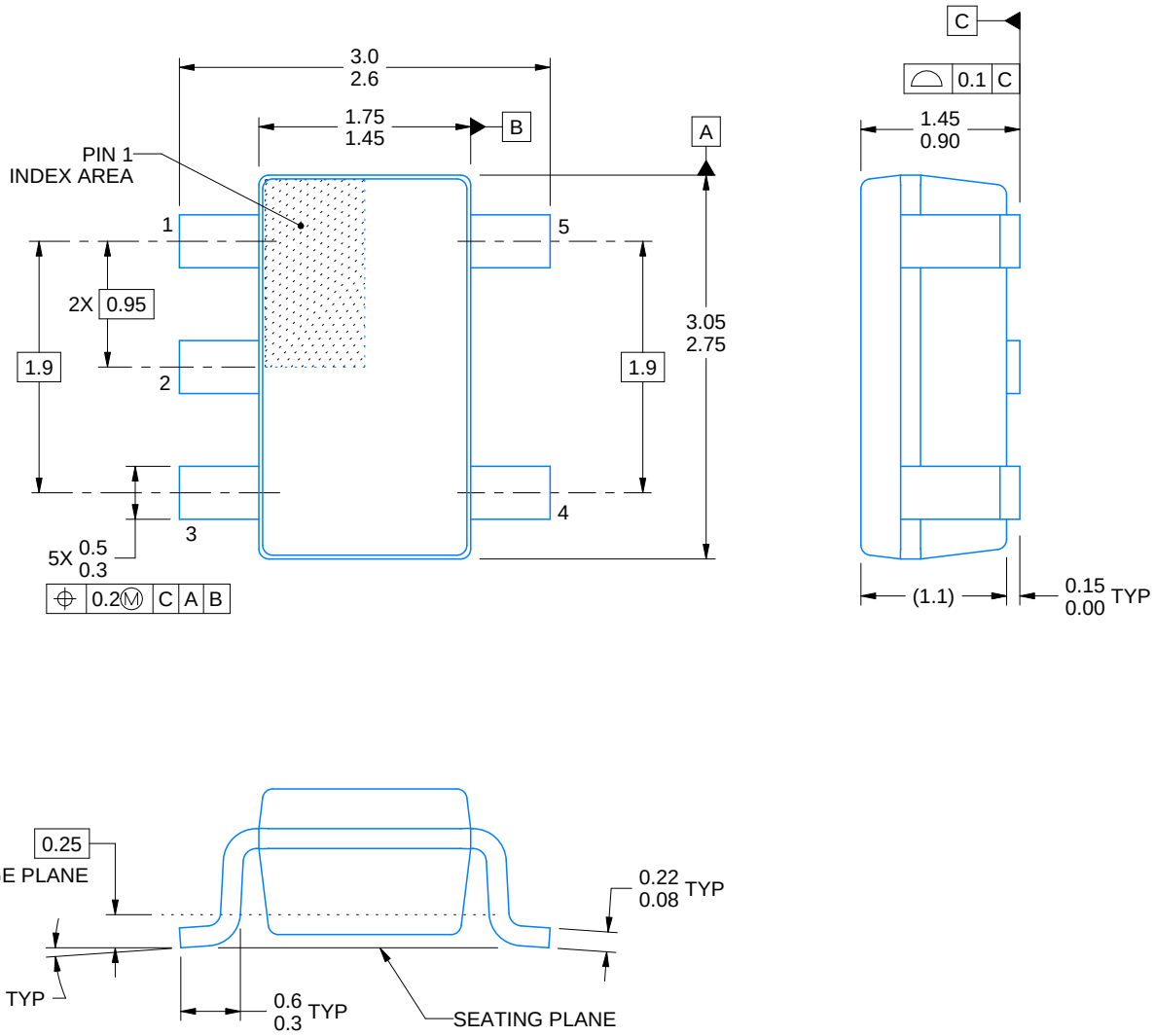
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431AQDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TLV431BQDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TLV431BQDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

NOTES:

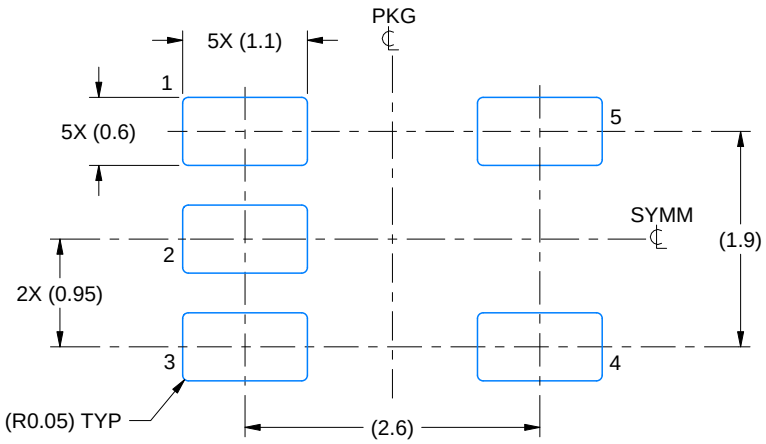
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

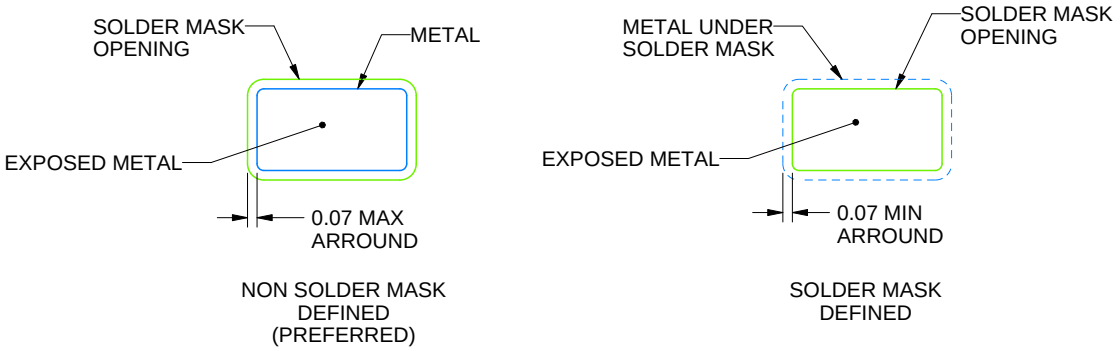
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

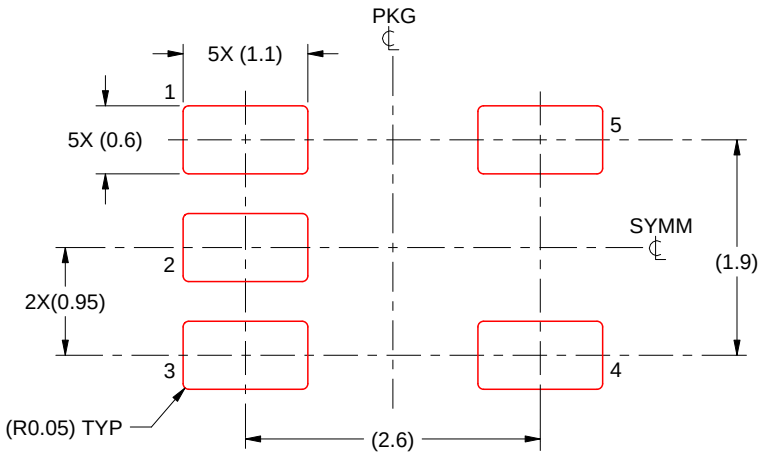
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

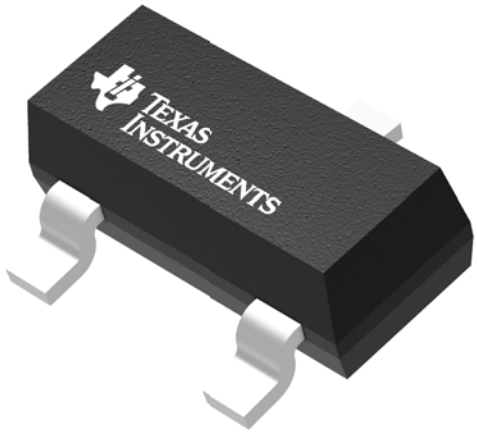
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

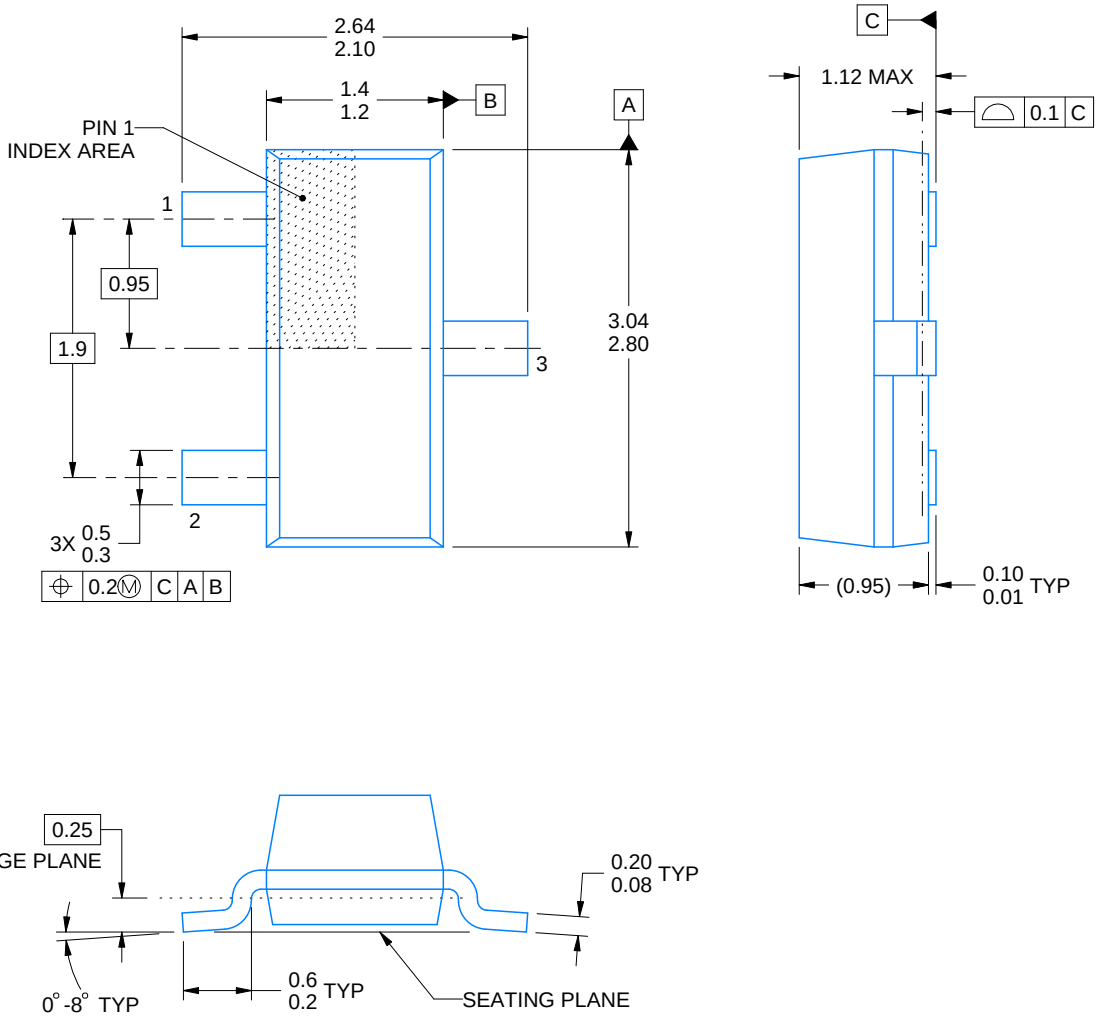
DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/C 04/2017

NOTES:

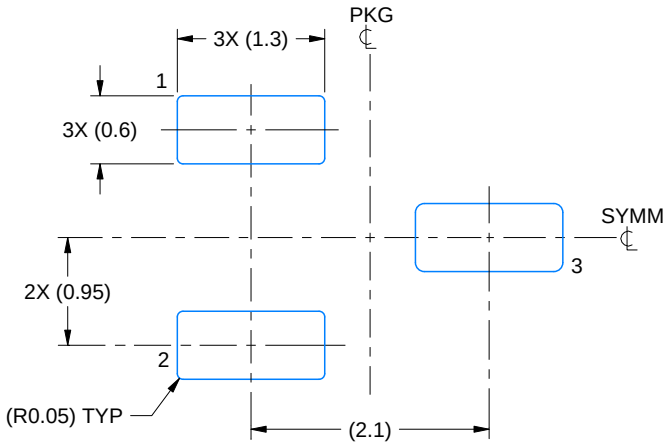
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

EXAMPLE BOARD LAYOUT

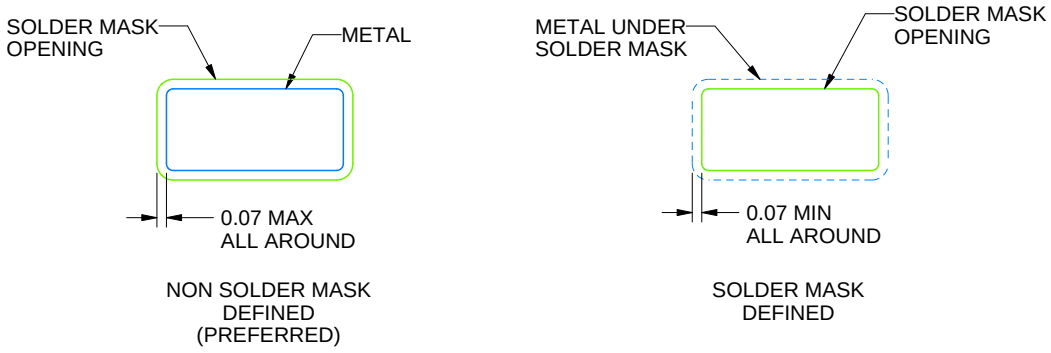
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

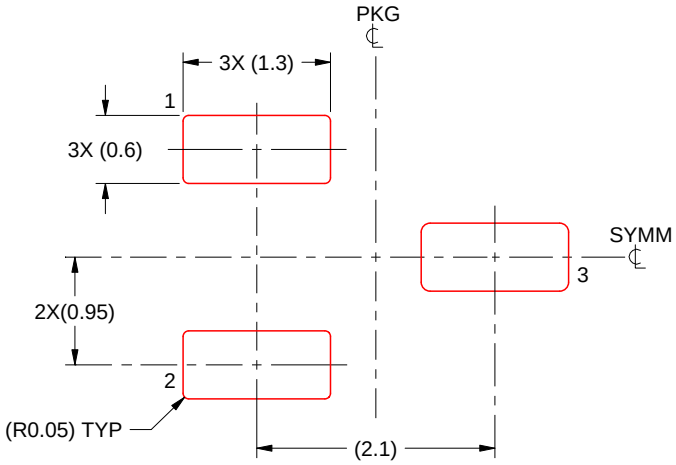
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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