TLV360x-Q1 325 MHz High-Speed Comparators with 2.5 ns Propagation Delay

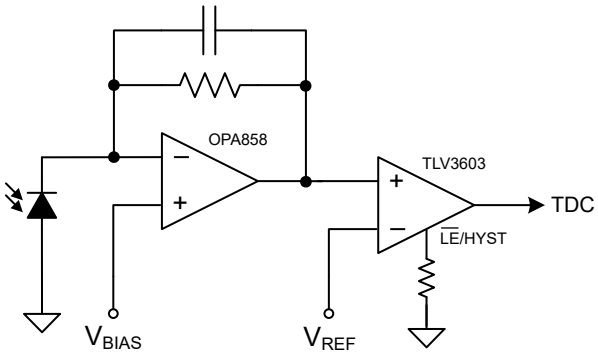
1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C3
- Fast propagation delay: 2.5 ns
- Low overdrive dispersion: 600 ps
- High toggle frequency: 325 MHz
- Narrow pulse width detection capability: 1.25 ns
- Push-pull output
- Wide supply range: 2.4 V to 5.5 V
- Input common-mode range extends 200 mV beyond both rails
- Low input offset voltage: ±5 mV
- Known startup condition at output
- TLV3603 specific features:
  - Adjustable hysteresis control pin
  - Latch function
- Packages: TLV3601 (SC70-5), (SOT23-5), TLV3603 (SC70-6),

  TLV3602 (VSSOP-8), (WSON-8)
- Functional Safety Capable
  - Documentation available to aid functional safety system design [TLV3601/2-Q1]
  - Documentation available to aid functional safety system design [TLV3603-Q1]

2 Applications

- DC/DC converter
- Inverter and motor control
- Fuel Cell Control Unit (FCCU)
- Battery Management System (BMS)
- Mechanically scanning LIDAR
- Audio amplifier



TLV3603 Application Circuit

3 Description

The TLV360x are a family of 325 MHz, high-speed comparators with rail-to-rail inputs and a propagation delay of 2.5 ns. The combination of fast response and wide operating voltage range make the comparators suitable for narrow signal pulse detection and data and clock recovery applications in LIDAR, range finders, and line receivers.

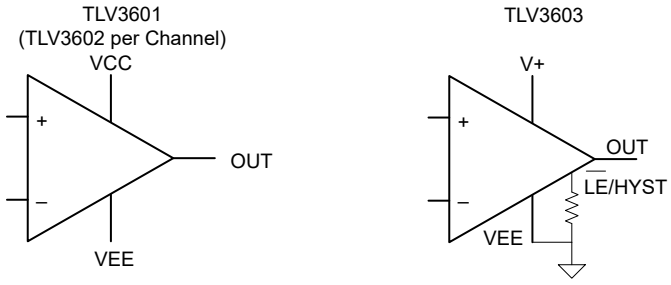
The push-pull (single-ended) outputs of the TLV360x family simplify and save cost on board-to-board wiring for I/O interfaces while reducing power consumption when compared to alternative high-speed differential output comparators. They can directly interface most prevailing digital controllers and IO expanders in the downstream circuit.

The TLV3601-Q1 is available in tiny 5-pin SC70 and SOT23 packages which makes it well suited for space constrained equipment that benefit from the comparators fast response time. TLV3603-Q1 is packaged in a 6-pin SC70 package and maintains the same speed and size as TLV3601-Q1 while offering the additional features of adjustable hysteresis control and output latch capability. The TLV3602-Q1 is a dual channel version of the TLV3601-Q1 and is packaged in 8-pin VSSOP and WSON packages.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TLV3601-Q1	SC70 (5)	1.25 mm × 2.00 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
TLV3603-Q1	SC70 (6)	1.25 mm × 2.00 mm
TLV3602-Q1	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8) (Preview)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagrams

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2022) to Revision D (August 2022)	Page
• Removed Preview from VSSOP package for the TLV3602-Q1	1

Changes from Revision B (November 2021) to Revision C (July 2022)	Page
• Added VSSOP and WSON package options for TLV3602-Q1 in Preview	1
• Removed Preview from SOT-23 package from TLV3601-Q1	1

Changes from Revision A (August 2021) to Revision B (November 2021)	Page
• Remove Preview from TLV3603-Q1	1
• Add DBV package option for TLV3601-Q1 in Preview	1
• Added typical performance curves	10

Changes from Revision * (June 2021) to Revision A (August 2021)	Page
• Production Data Release	1

5 Pin Configuration and Functions

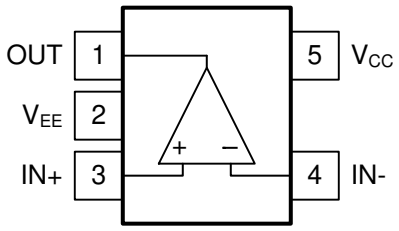


Figure 5-1. DCK, DBV Package
5-Pin SC70, SOT-23
Top View

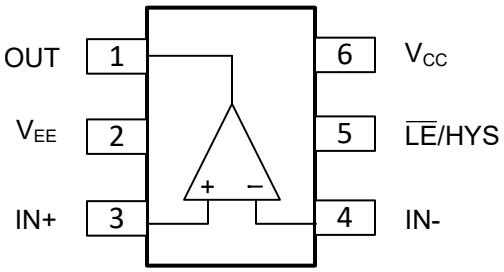


Figure 5-2. DCK Package
6-Pin SC70
Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	TLV3601	TLV3603		
IN+	3	3	I	Non-inverting input
IN–	4	4	I	Inverting input
OUT	1	1	O	Output (Push-pull)
V_{EE}	2	2	I	Negative power supply
V_{CC}	5	6	I	Positive power supply
$\overline{LE}$/HYS	-	5	I	Adjustable hysteresis control and latch

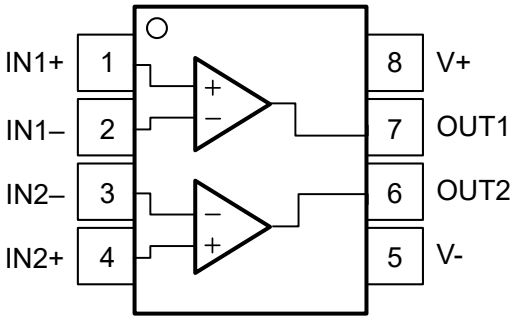


Figure 5-3. TLV3602 DGK, DSG Packages
8-Pin VSSOP, WSON

Table 5-2. Pin Functions: TLV3602 (Dual)

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2–	3	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	7	O	Output, channel 1
OUT2	6	O	Output, channel 2
V-	5	P	Negative (lowest) supply or ground
V+	8	P	Positive (highest) supply
Thermal PAD		-	Connect directly to V- pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input Supply Voltage: V_{CC} – V_{EE}	–0.3	6	V
Input Voltage (IN+, IN–)(2)	V_{EE} – 0.3	V_{CC} + 0.3	V
Differential Input Voltage (V_{DI} = IN+ – IN–)	–(V_{CC} – V_{EE} + 0.3)	+ (V_{CC} –V_{EE} + 0.3)	V
Output Voltage (OUT)(3)	V_{EE} – 0.3	V_{CC} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CC} + 0.3	V
Current into Input pins (IN+, IN–, $\overline{LE}$/HYS)(2)		±10	mA
Current into Output pins (OUT)(3)		±50	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 50 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
TLV3601(DCK), TLV3603				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
TLV3601(DBV)				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	
TLV3602				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Supply Voltage: V_{CC} – V_{EE}	2.4	5.5	V
Input Voltage Range (IN+, IN–)	V_{EE} – 0.3	V_{CC} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CC} + 0.3	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information

THERMAL METRIC		TLV3601 DBV (SOT-23) 5 PINS	TLV3601 DCK (SC70) 5 PINS	TLV3602 DGK (VSSOP) 8 PINS	TLV3602 DSG (WSON) 8 PINS	TLV3603 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.5	187.5	170.5	64.9	165.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.7	139.2	61.7	83.9	129.1	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	5.5	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.4	65.8	92.4	32.0	58.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.7	43.0	8.9	2.1	39.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.1	65.5	90.8	32.0	58.7	°C/W

6.5 Electrical Characteristics

V_{CC} = 2.5, 3.3 and 5 V, V_{EE} = 0 V, V_{CM} = V_{EE} + 300 mV, C_L = 5 pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO}	Input offset voltage	T_A = –40°C to +125°C	–5	±0.5	5	mV
dV_{IO}/dT	Input offset voltage drift			±3.0		µV/°C
V_{CM}	Input common mode voltage range	T_A = –40°C to +125°C	V_{EE} – 0.2		V_{CC} + 0.2	V
V_{HYST} (TLV3601)	Input hysteresis voltage	T_A = –40°C to +125°C	1.5	3	5(1)	mV
C_{IN}	Input capacitance			1		pF
R_{DM}	Input differential mode resistance			67		kΩ
R_{CM}	Input common mode resistance			5		MΩ
I_B	Input bias current	T_A = –40°C to +125°C		1	5	uA
I_{OS}	Input offset current			±0.03		uA
CMRR	Common-mode rejection ratio	V_{CM} = V_{EE} – 0.2V to V_{CC} + 0.2V		80		dB
PSRR	Power-supply rejection ratio	V_{CC} = 2.4 to 5.5V		80		dB
DC Output Characteristics						
V_{OH}	Output high voltage from V_{CC}	I_{SOURCE} = 1 mA T_A = –40°C to +125°C		60	80	mV
V_{OL}	Output low voltage from V_{EE}	I_{SINK} = 1 mA T_A = –40°C to +125°C		60	80	mV
I_{SC_SOURCE}	Output Short-Circuit Current - Source	T_A = –40°C to +125°C	10	30		mA
I_{SC_SINK}	Output Short-Circuit Current - Sink	T_A = –40°C to +125°C	10	30		mA
Power Supply						
I_{CC} (TLV3601)	quiescent current	Output being high T_A = –40°C to +125°C		4.9	7	mA
I_{CC} (TLV3602)	quiescent current per channel	Output being high T_A = –40°C to +125°C		4.9	7	mA
I_{CC} (TLV3603)	quiescent current	Output being high T_A = –40°C to +125°C		5.7	7.8	mA
$V_{POR\ (postive)}$	Power-On Reset Voltage			2.1		V
AC Characteristics						
t_{PD}	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV		2.5	3.5(1)	ns
t_{PD}	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV T_A = –40°C to +125°C			4.5(1)	ns
Δt_{PD} (TLV3602 only)	Channel-to-channel propagation delay skew(2)	V_{CM} = V_{CC}/2, $V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV, 50 MHz Squarewave		24		ps
$t_{CM_DISPERSION}$	Common dispersion	V_{CM} varied from V_{EE} to V_{CC}		80		ps
$t_{OD_DISPERSION}$	Overdrive dispersion	Overdrive varied from 10 mV to 125 mV		600		ps
$t_{UD_DISPERSION}$	Underdrive dispersion	Underdrive varied from 10mV to 125 mV		330		ps
t_R	Rise time	10% to 90%		0.75		ns
t_F	Fall time	90% to 10%		0.75		ns
t_{JITTER}	RMS Jitter	V_{IN} = 100mV_{P-P}, f_{IN} = 100MHz, Jitter BW = 10Hz – 50MHz		4		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mV_{PP} Sine Wave, When output high reaches 90% of V_{CC} - V_{EE} or output low reaches 10% of V_{CC} - V_{EE}		325		MHz
PulseWidth	Minimum allowed input pulse width	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV PW_{OUT} = 90% of PW_{IN}		1.25		ns

6.5 Electrical Characteristics (continued)

V_{CC} = 2.5, 3.3 and 5 V, V_{EE} = 0 V, V_{CM} = V_{EE} + 300 mV, C_L = 5 pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Latching/Adjustable Hysteresis						
V_{HYST}	Input hysteresis voltage	V_{HYST} = Logic High		0		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = Floating		3		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 150 kΩ		30		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 56 kΩ		60		mV
V_{IH_LE}	$\overline{LE}$ pin input high level	T_A = –40°C to +125°C	V_{EE} + 1.5			V
V_{IL_LE}	$\overline{LE}$ pin input low level	T_A = –40°C to +125°C			V_{EE} + 0.35	V
I_{IH_LE}	$\overline{LE}$ pin input leakage current	V_{LE} = V_{CC} T_A = –40°C to +125°C			15	uA
I_{IL_LE}	$\overline{LE}$ pin input leakage current	V_{LE} = V_{EE}, T_A = –40°C to +125°C			40	uA
t_{SETUP}	Latch setup time			–1.4		ns
t_{HOLD}	Latch hold time			7.2		ns
t_{PL}	Latch to OUT delay			7		ns

(1) Ensured by characterization
(2) Differential propagation delay is defined as the larger of the two:
ΔtPDLH = tPDLH(MAX) – tPDLH(MIN)
ΔtPDHL = tPDHL(MAX) – tPDHL(MIN)
where (MAX) and (MIN) denote the maximum and minimum values of a given measurement across the different comparator channels.

6.6 Timing Diagrams

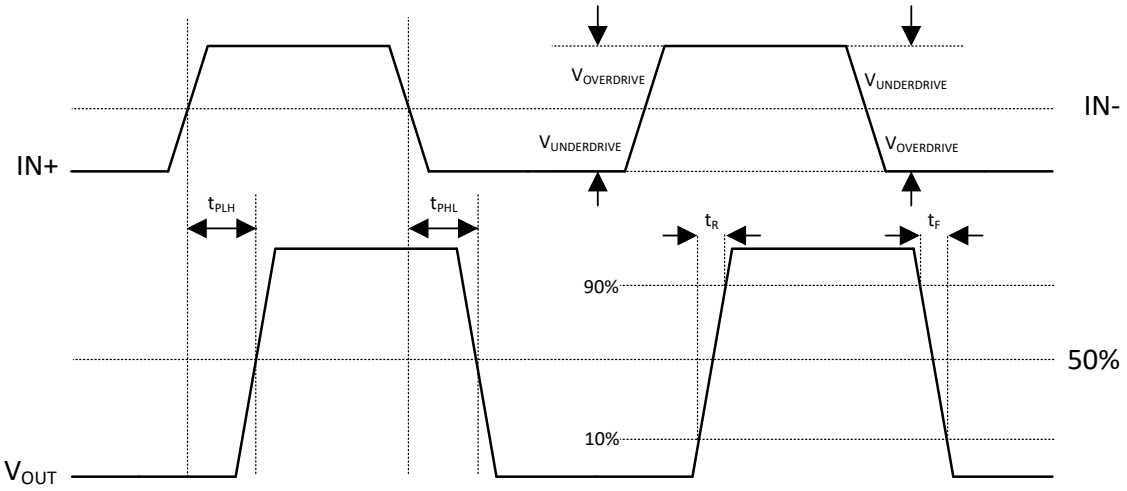


Figure 6-1. General Timing Diagram

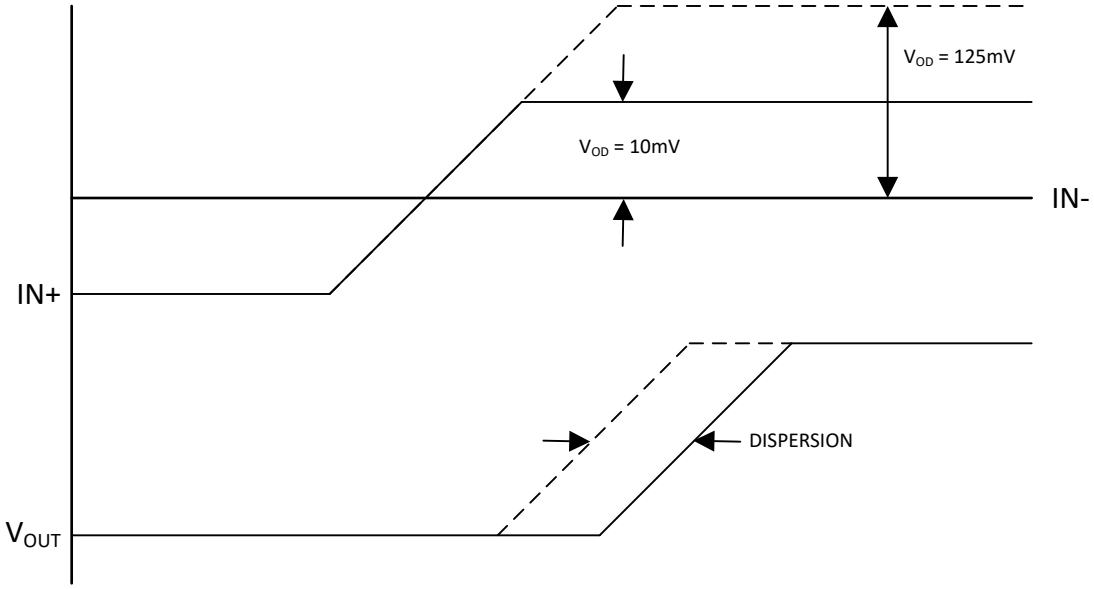


Figure 6-2. Overdrive Dispersion

6.7 Typical Characteristics

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

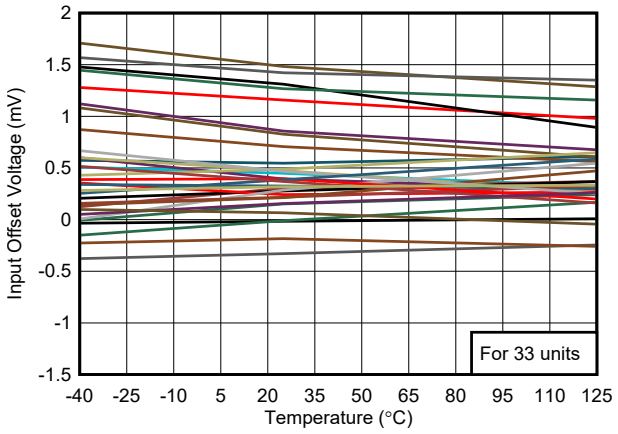


Figure 6-3. TLV3601 Offset vs. Temperature

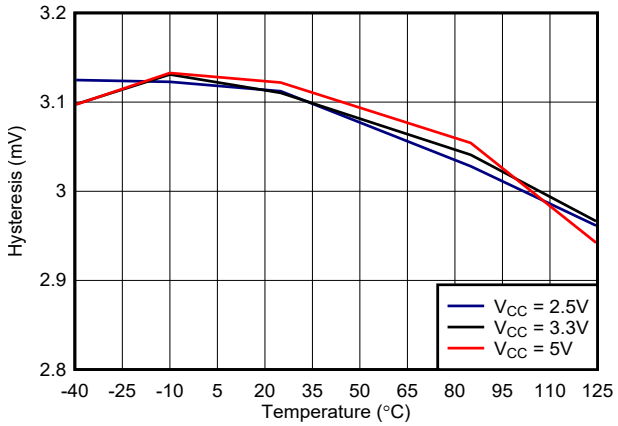


Figure 6-4. TLV3601 Hysteresis vs. Temperature

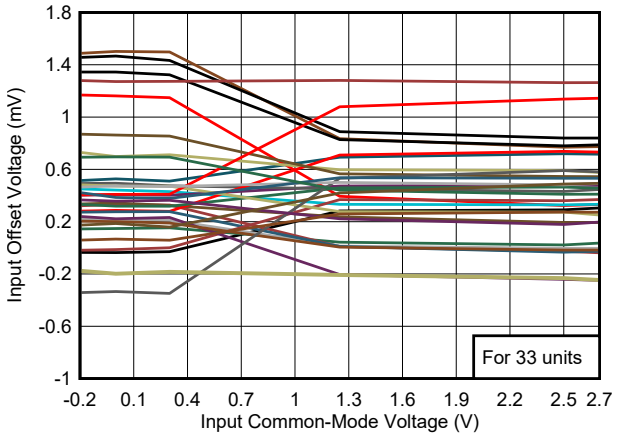


Figure 6-5. TLV3601 Offset vs. Common-Mode, 2.5 V

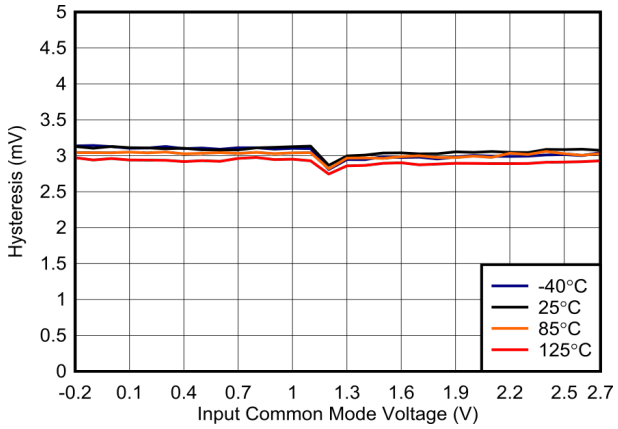


Figure 6-6. TLV3601 Hysteresis vs. Common-Mode, 2.5 V

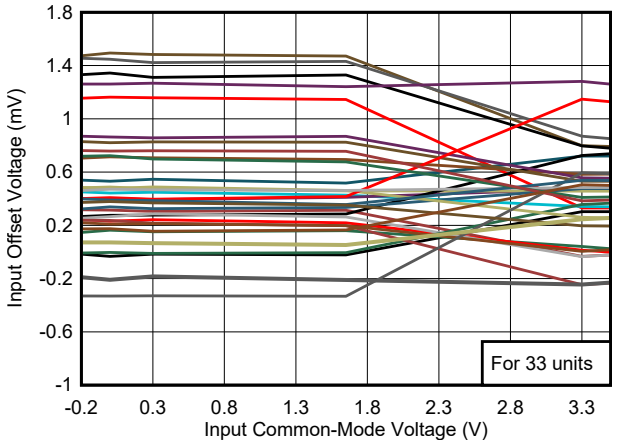


Figure 6-7. TLV3601 Offset vs. Common-Mode, 3.3 V

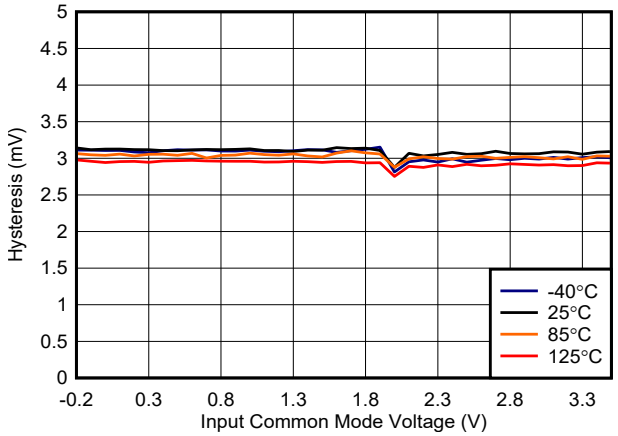


Figure 6-8. TLV3601 Hysteresis vs. Common-Mode, 3.3 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

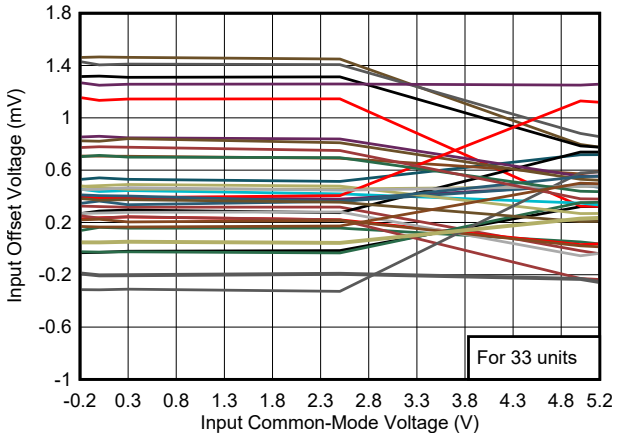


Figure 6-9. TLV3601 Offset vs. Common-Mode, 5 V

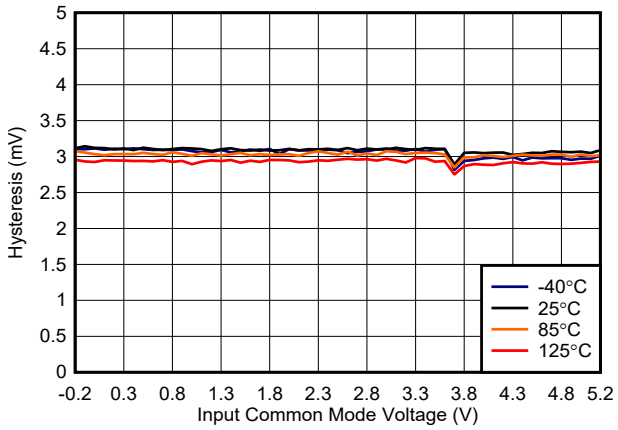


Figure 6-10. TLV3601 Hysteresis vs. Common-Mode, 5 V

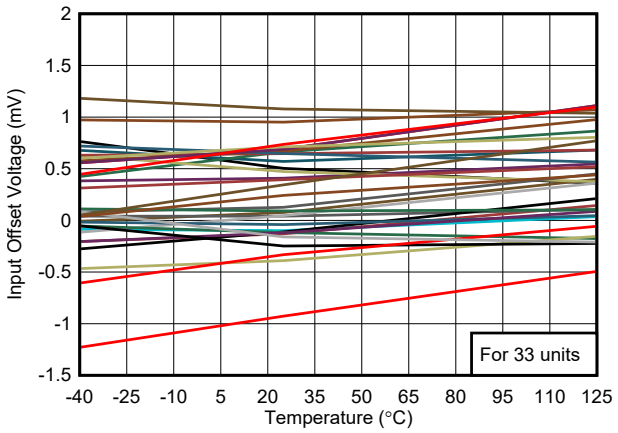


Figure 6-11. TLV3603 Offset vs. Temperature

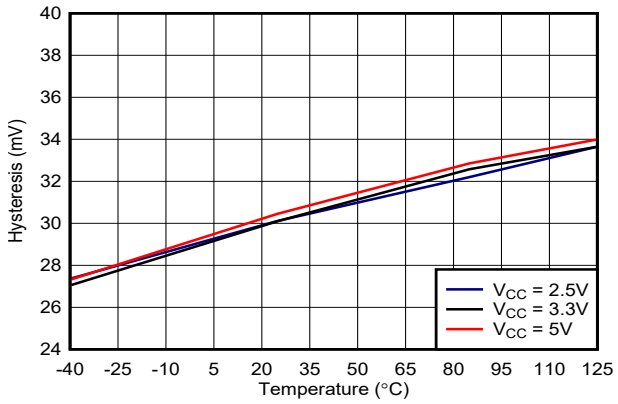


Figure 6-12. TLV3603 Hysteresis vs. Temperature

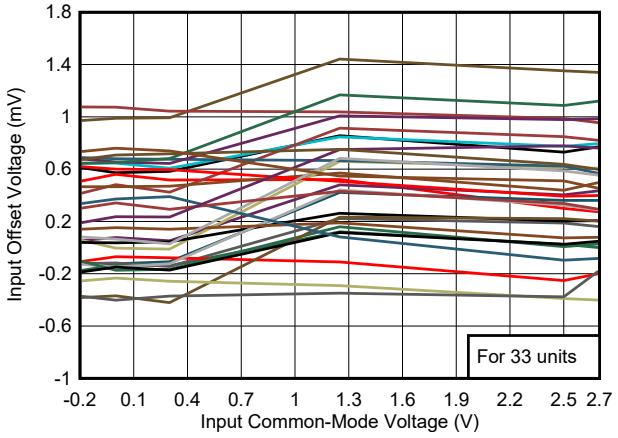


Figure 6-13. TLV3603 Offset vs. Common-Mode, 2.5 V

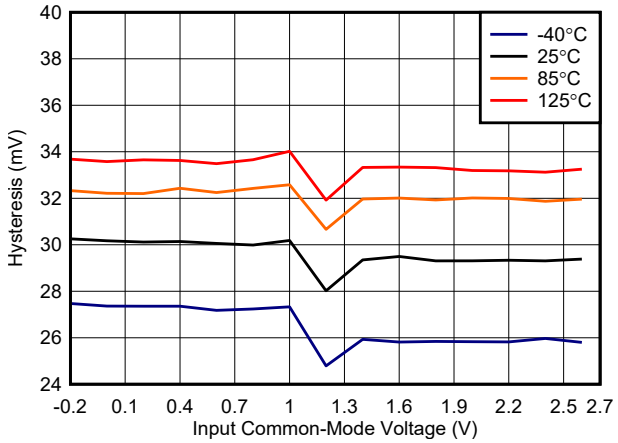


Figure 6-14. TLV3603 Hysteresis vs. Common-Mode, 2.5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

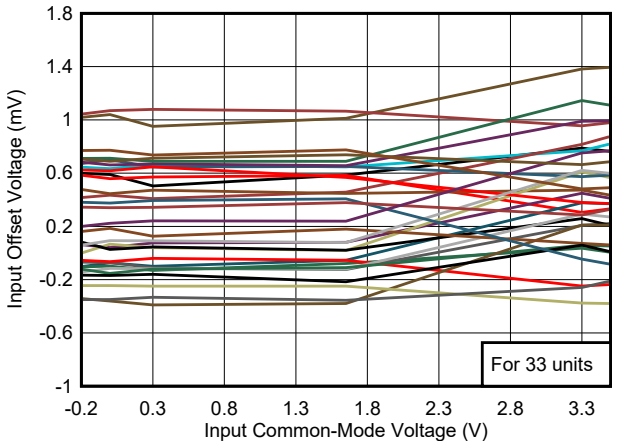


Figure 6-15. TLV3603 Offset vs. Common-Mode, 3.3 V

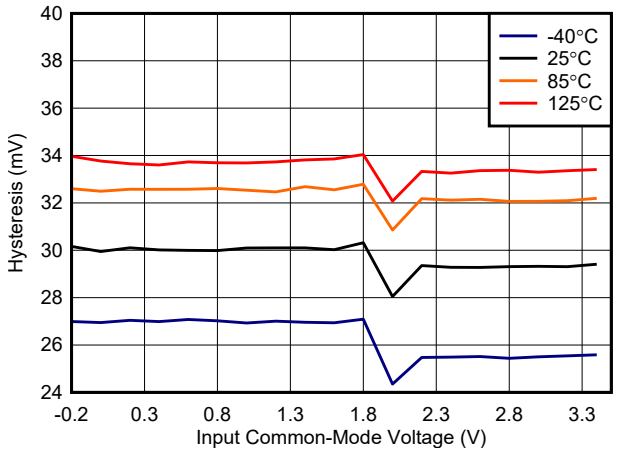


Figure 6-16. TLV3603 Hysteresis vs. Common-Mode, 3.3 V

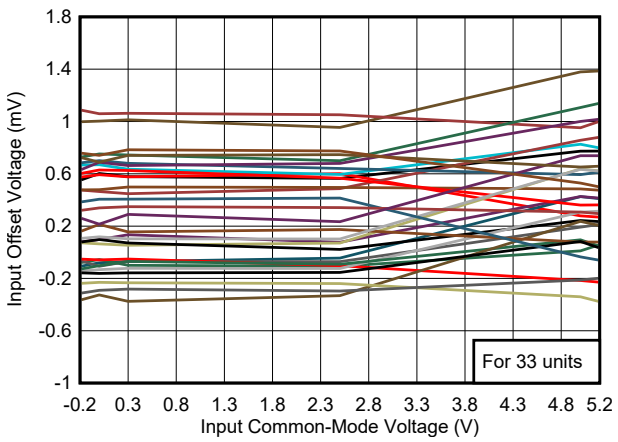


Figure 6-17. TLV3603 Offset vs. Common-Mode, 5 V

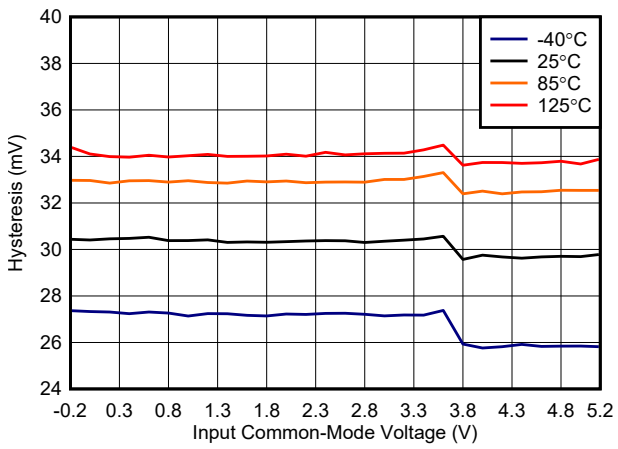


Figure 6-18. TLV3603 Hysteresis vs. Common-Mode, 5 V

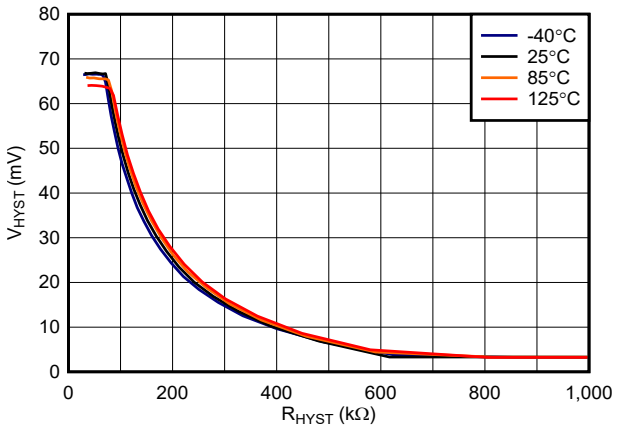


Figure 6-19. TLV3603 Hysteresis vs. Resistance, 2.5 V

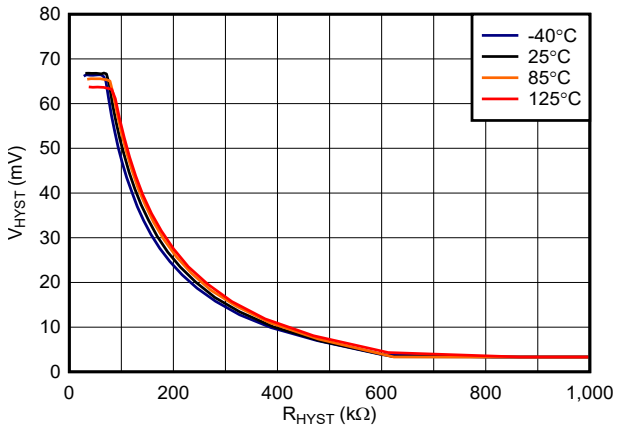


Figure 6-20. TLV3603 Hysteresis vs. Resistance, 3.3 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

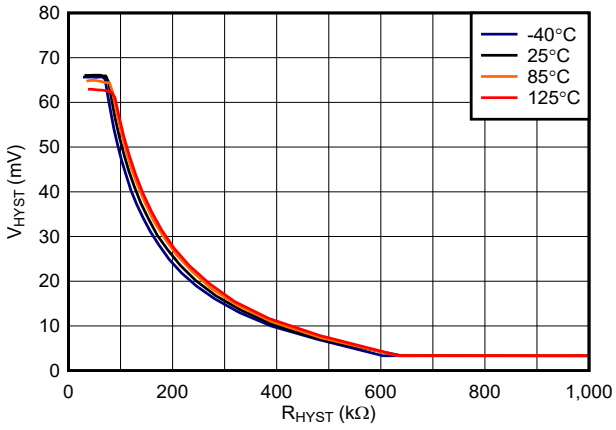


Figure 6-21. TLV3603 Hysteresis vs. Resistance, 5 V

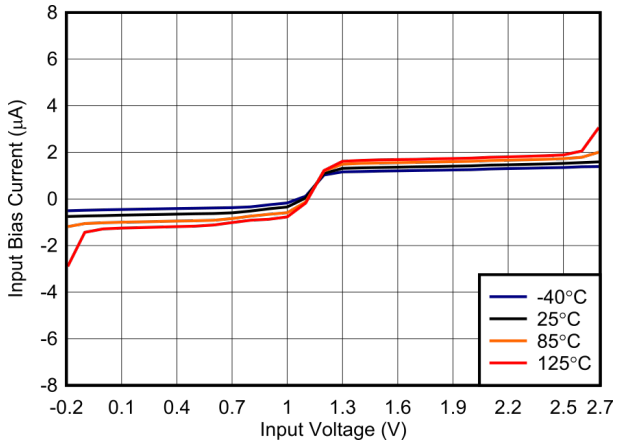


Figure 6-22. Bias Current vs. Input Voltage, 2.5 V

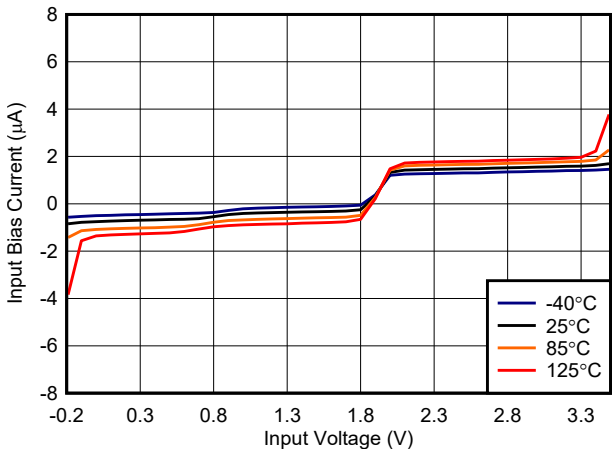


Figure 6-23. Bias Current vs. Input Voltage, 3.3 V

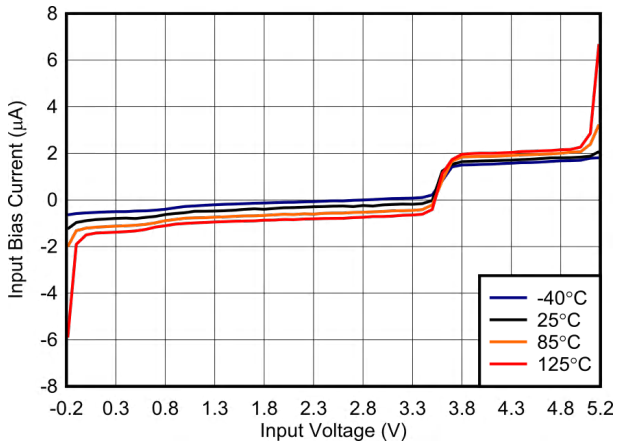


Figure 6-24. Bias Current vs. Input Voltage, 5 V

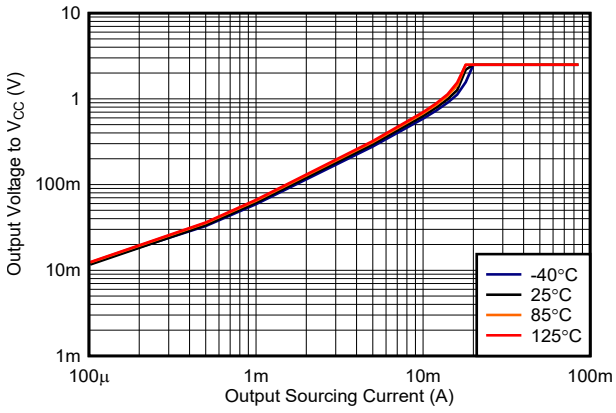


Figure 6-25. Output Voltage vs. Output Sourcing Current, 2.5 V

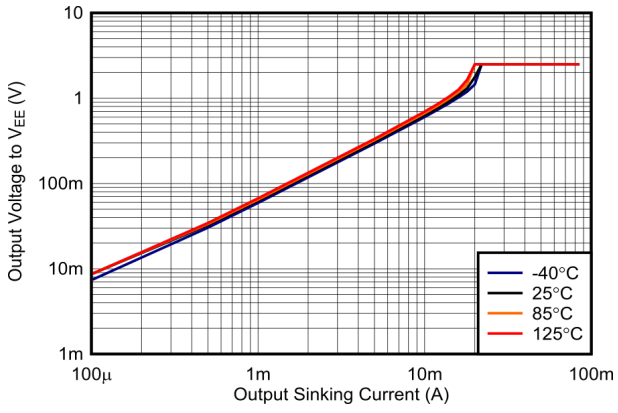


Figure 6-26. Output Voltage vs. Output Sinking Current, 2.5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

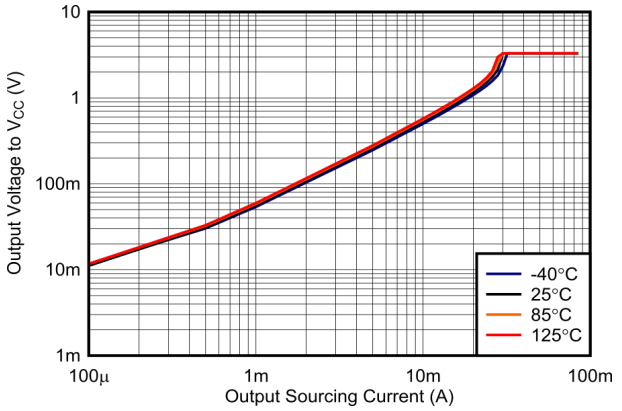


Figure 6-27. Output Voltage vs. Output Sourcing Current, 3.3 V

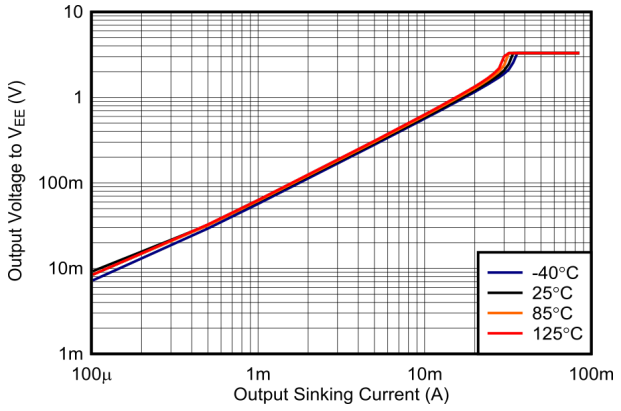


Figure 6-28. Output Voltage vs. Output Sinking Current, 3.3 V

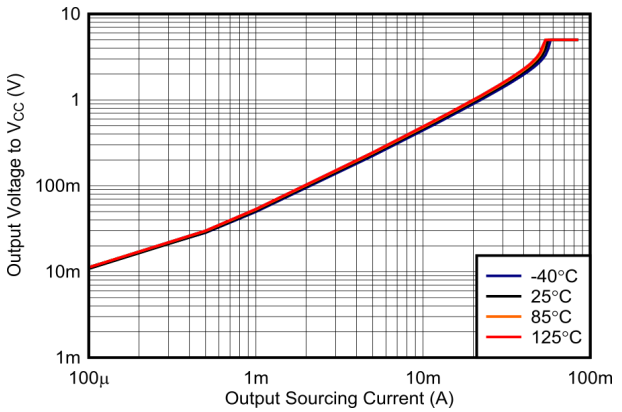


Figure 6-29. Output Voltage vs. Output Sourcing Current, 5 V

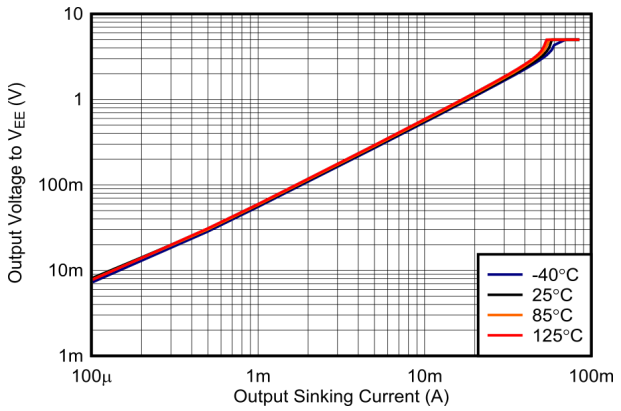


Figure 6-30. Output Voltage vs. Output Sinking Current, 5 V

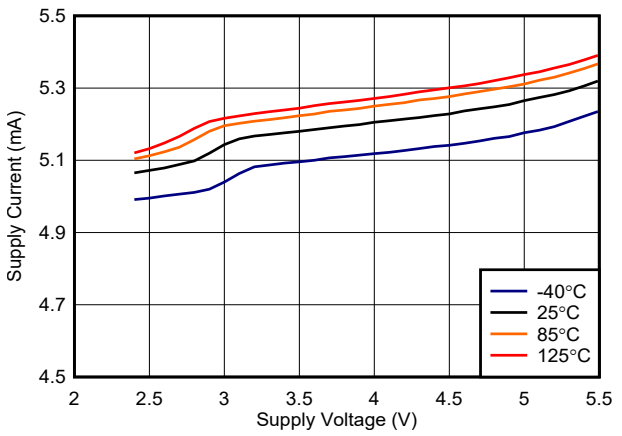


Figure 6-31. TLV3601 Supply Current vs. Voltage (Output Low)

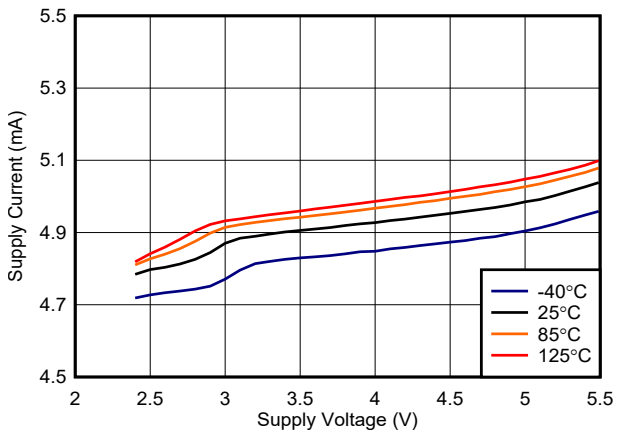


Figure 6-32. TLV3601 Supply Current vs. Voltage (Output High)

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

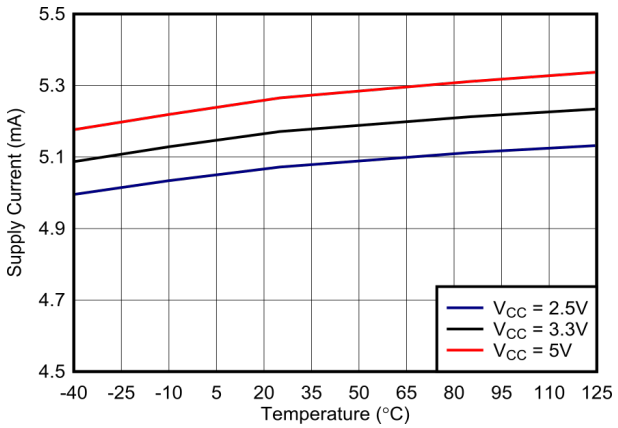


Figure 6-33. TLV3601 Supply Current vs. Temp (Output Low)

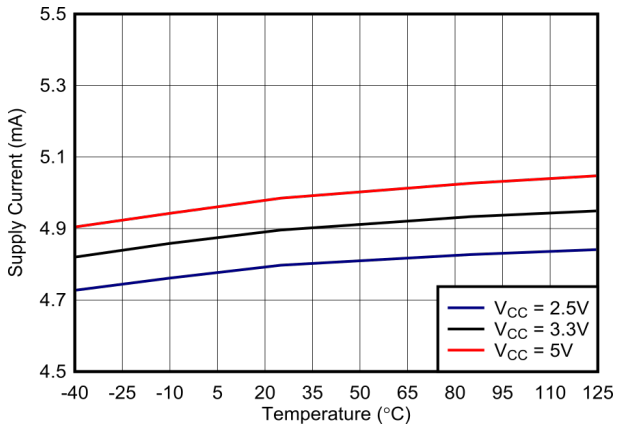


Figure 6-34. TLV3601 Supply Current vs. Temp (Output High)

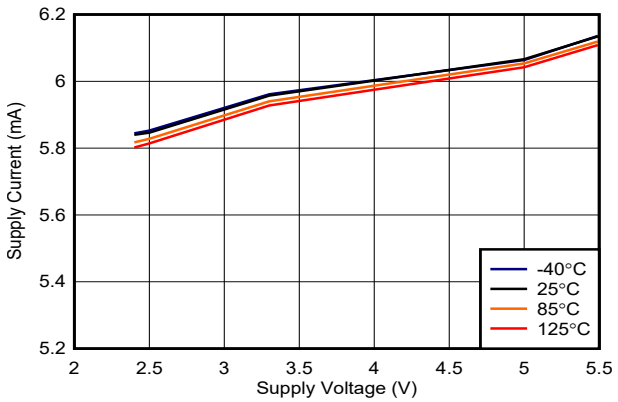


Figure 6-35. TLV3603 Supply Current vs. Voltage (Output Low)

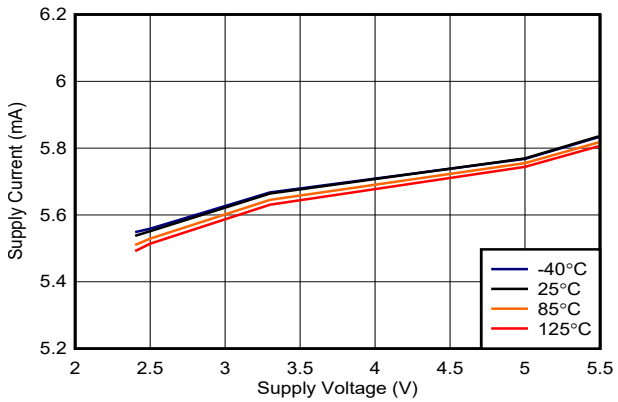


Figure 6-36. TLV3603 Supply Current vs. Voltage (Output High)

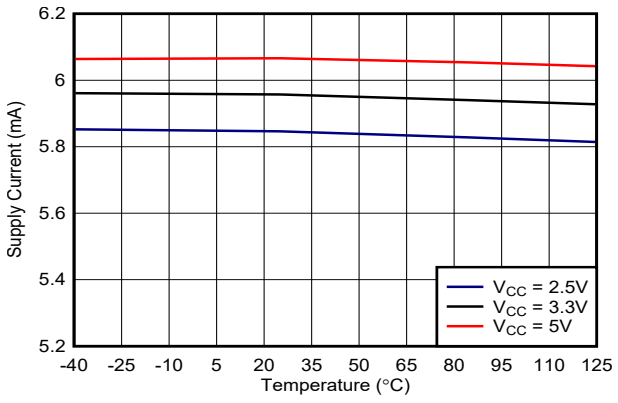


Figure 6-37. TLV3603 Supply Current vs. Temp (Output Low)

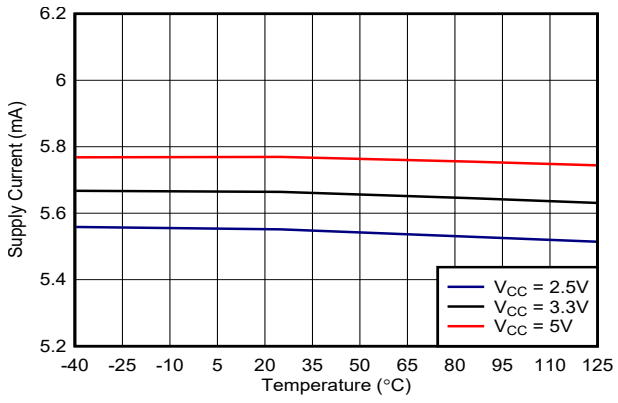


Figure 6-38. TLV3603 Supply Current vs. Temp (Output High)

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

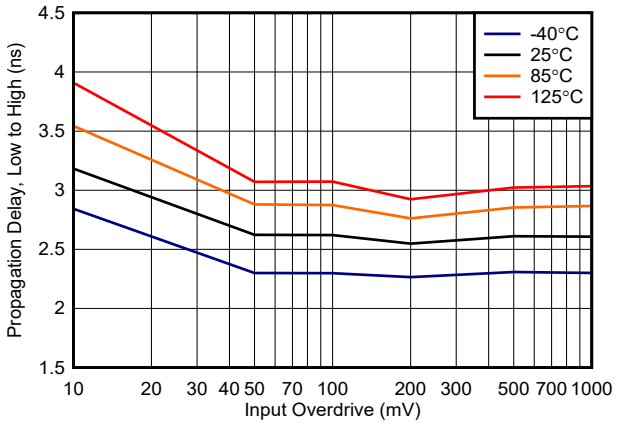


Figure 6-39. Propagation Delay, Low to High, 2.5 V

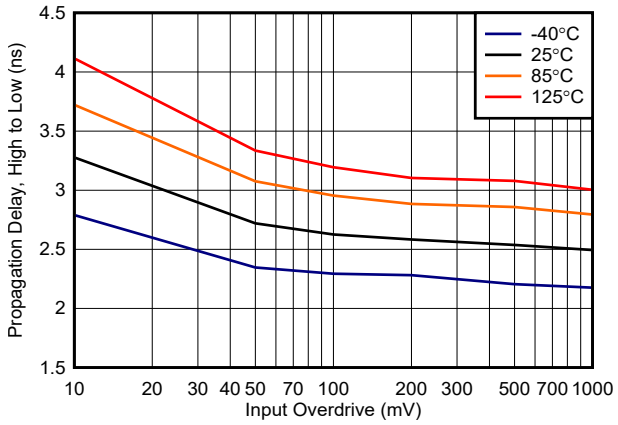


Figure 6-40. Propagation Delay, High to Low, 2.5 V

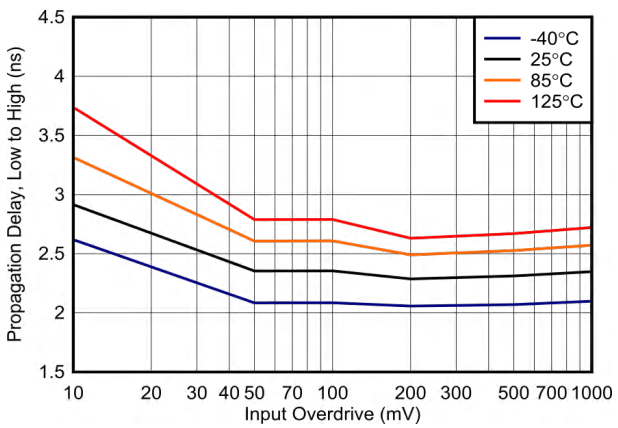


Figure 6-41. Propagation Delay, Low to High, 3.3 V

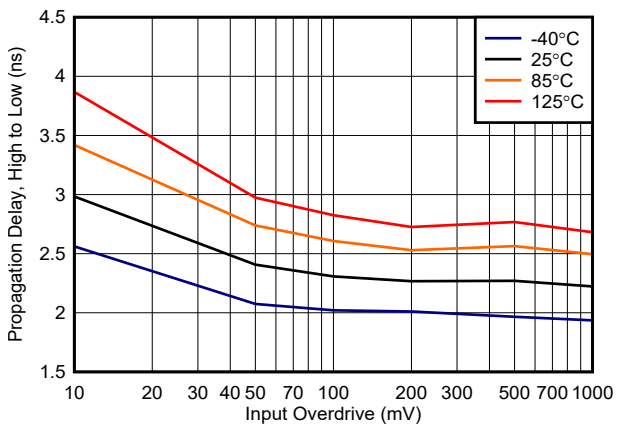


Figure 6-42. Propagation Delay, High to Low, 3.3 V

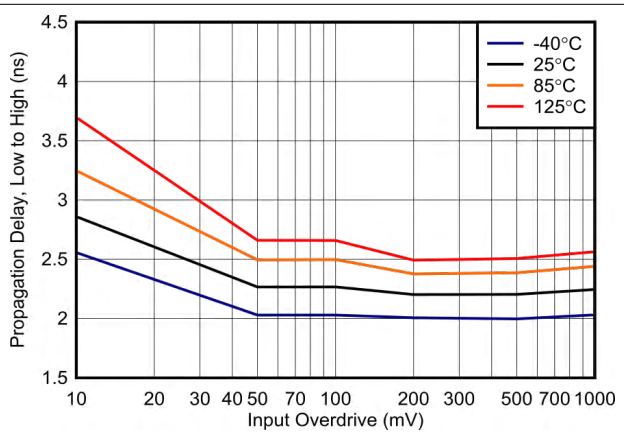


Figure 6-43. Propagation Delay, Low to High, 5 V

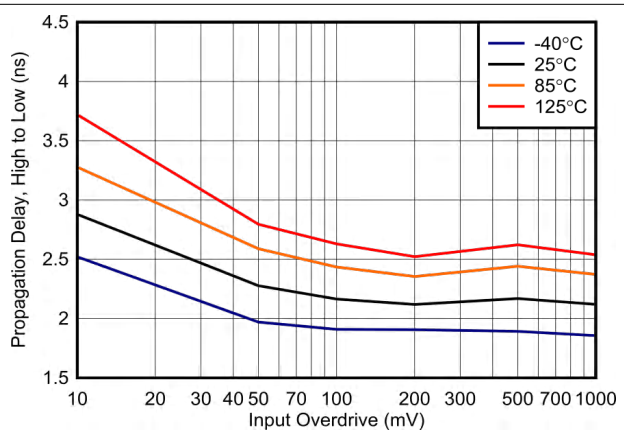


Figure 6-44. Propagation Delay, High to Low, 5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

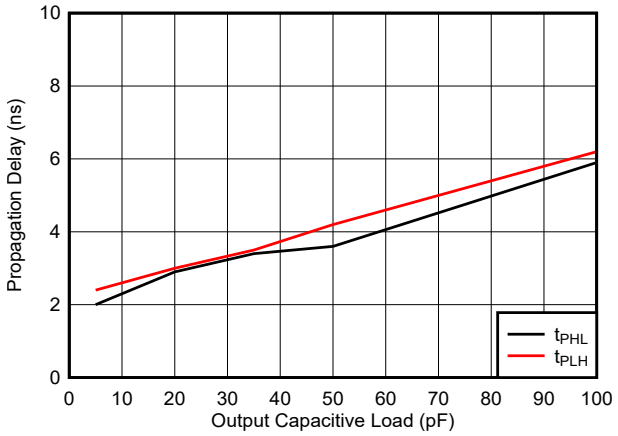


Figure 6-45. Propagation Delay vs. Load Capacitance, 3.3 V

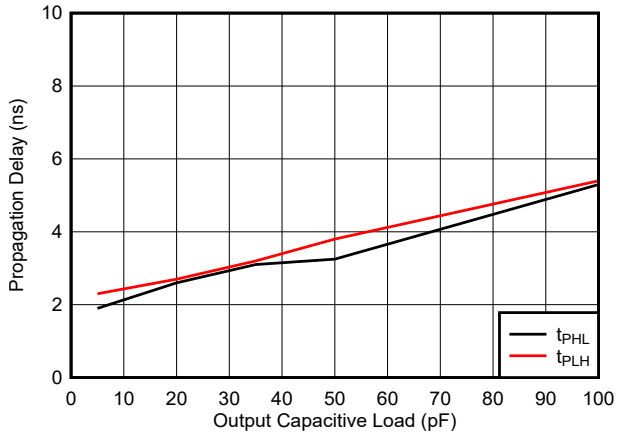


Figure 6-46. Propagation Delay vs. Load Capacitance, 5 V

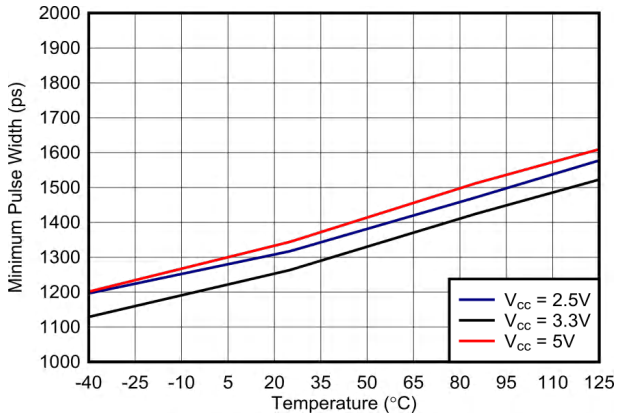


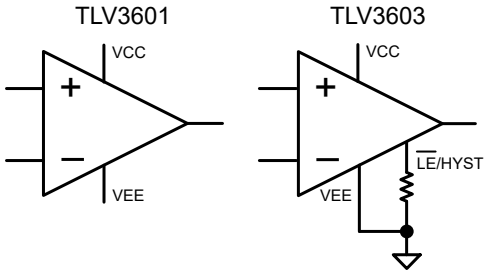
Figure 6-47. Minimum Pulse Width vs. Temperature

7 Detailed Description

7.1 Overview

TheTLV360x family are high-speed comparators with single-ended (push-pull) output stages. The fast response time of these comparators make them well suited for applications that require narrow pulse width detection or high toggle frequencies. The TLV3601-Q1 is available in a 5-pin SC70 and SOT23 package, while the TLV3603-Q1 is packaged in a 6-pin SC70. The TLV3602-Q1 is a dual channel version of the TLV3601-Q1 and is packaged in an 8-pin VSSOP and WSON package.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV3601-Q1,TLV3603-Q1, and TLV3602-Q1 are single and dual channel, high speed comparators with a typical propagation delay of 2.5 ns and push-pull outputs. The minimum pulse width detection capability is 1.25 ns and the typical toggle rate is 325 MHz. These comparators are well-suited for distance measurement applications that utilize a time-of-flight arechitecture as well as systems that suffer from capacitive loading and require data and clock recovery. In addition to their high speed, the TLV360x family offers rail-to-rail input stages capable of operating up to 200 mV beyond each power supply rail combined with a maximum 5 mV input offset. The TLV3603-Q1 also provides adjustable hysteresis via an external resistor for noise suppression or a latching mode to hold the output of the comparators.

7.4 Device Functional Modes

The TLV3601-Q1 has a single functional mode and is active when the power supply voltage is greater than 2.4V. The TLV3603-Q1 has two modes of operation. The first is an active mode where the output reflects the condition at the inputs when an external resistor is connected to ground on the $\overline{LE}$/HYS pin. The second is a latch mode where the output is held at its last active state when the $\overline{LE}$/HYS pin is pulled low. The TLV3603-Q1 returns to active mode after a short delay when the pin is pulled high.

7.4.1 Inputs

The TLV360x family features input stages capable of operating 200 mV below negative power supply (ground) and 200 mV beyond the positive supply voltage, allowing for zero cross detection and maximizing input dynamic range given a certain power supply. The input stages are protected from conditions where the voltage on either pin exceeds this level by internal ESD protection diodes to VCC and VEE. To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor should be used to limit the current.

7.4.2 Push-Pull (Single-Ended) Output

The TLV360x outputs have excellent drive capability and are designed to connect directly to CMOS logic input devices. Likewise, the comparator output stages can drive capacitive loads. Transient performance parameters in the Electrical Characteristics Tables and Typical Characteristics section are for a load of 5pF, corresponding to a standard CMOS load. Device performance for larger capacitive loads can be found in the typical performance curves titled Propagation Delay vs Capacitive Load. For optimal speed and performance, output load capacitance should be reduced as much as possible.

7.4.3 Known Startup Condition

The TLV360x have a Power-on-Reset (POR) circuit which provides system designers a known start-up condition for the output of the comparators. When the power supply (VCC) is ramping up or ramping down, the POR circuit will be active when VCC is below V_{POR}. When active, the POR circuit holds the output low at VEE. When VCC is greater than or equal to V_{POR} as stated in Section 6.5 , the comparator output reflects the state of the input pins.

Figure 7-1 shows how the TLV360x outputs respond for VCC rising. The input is configured with a logic high input to highlight the transition from the POR circuit control (logic low output) to a standard comparator operation where the output reflects the input condition. Note how the output goes high when VCC reaches 2.1V.

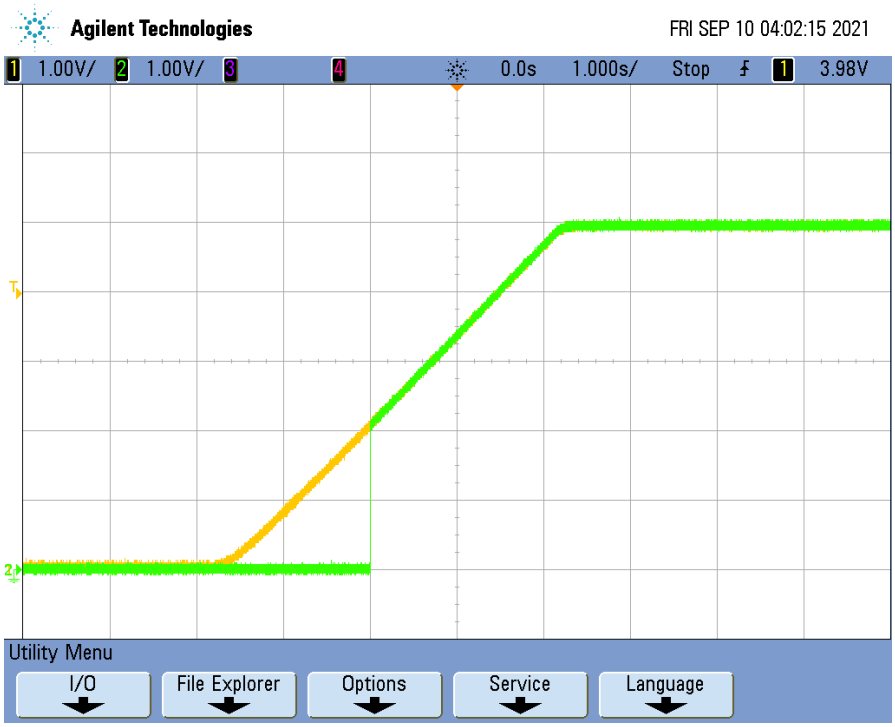


Figure 7-1. TLV3601/TLV3603 Output for VCC Rising

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Hysteresis

As a result of a comparator's high open loop gain, there is a small band of input differential voltage where the output can toggle back and forth between "logic high" and "logic low" states. This can cause design challenges for inputs with slow rise and fall times or systems with excessive noise. These challenges can be overcome by adding hysteresis to the comparator.

Since the TLV3601-Q1 and TLV3602-Q1 only has a minimal amount of internal hysteresis, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on its current output state. See the Implementing Hysteresis section for more details.

The TLV3603-Q1 on the other hand has a $\overline{LE}$/HYS pin that can be used to increase or eliminate the internal hysteresis of the comparator. In order to increase the internal hysteresis of the TLV3603-Q1, connect a single resistor as shown in the adjusting hysteresis figure between the $\overline{LE}$/HYS pin and VEE. A curve of hysteresis versus resistance is provided below to provide guidance in setting the desired amount of hysteresis. Likewise, for applications where no hysteresis is desired, the $\overline{LE}$/HYS pin can be connected to VCC.

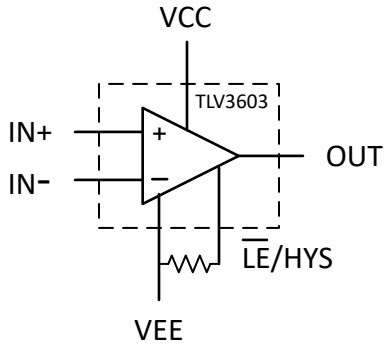


Figure 8-1. Adjustable Hysteresis with an External Resistor

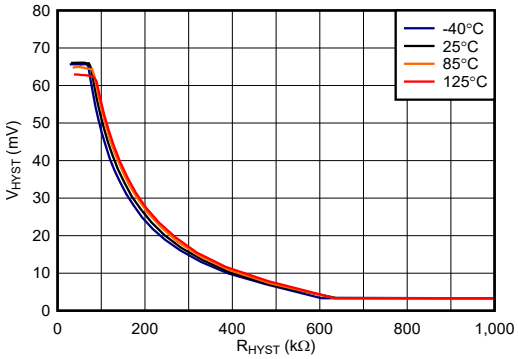


Figure 8-2. V_{HYST} (mV) vs R_{HYST} (kΩ), V_{CC} = 5 V

8.1.2 Capacitive Loads

For capacitive loads under 100 pF, the propagation delay has minimum change (see Propagation Delay vs. Capacitive Load). However, excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

8.1.3 Latch Functionality

The latch pin for the TLV3603-Q1 holds the output state of the device when the voltage at the $\overline{LE}$/HYS pin is a logic low. This is particularly useful when the output state is intended to remain unchanged. An important consideration of the latch functionality is the latch hold and setup times. Latch hold time is the minimum time required (after the latch pin is asserted) for properly latching the comparator output. Likewise, latch setup time is defined as the time that the input must be stable before the latch pin is asserted low. The figure below illustrates when the input can transition for a valid latch. Note that the typical setup time in the EC table is negative; this is due to the internal trace delays of the $\overline{LE}$/HYS pin relative to the input pin trace delays. A small delay (t_{PL}) in the output response is shown below when the TLV3603-Q1 exits a latched output stage.

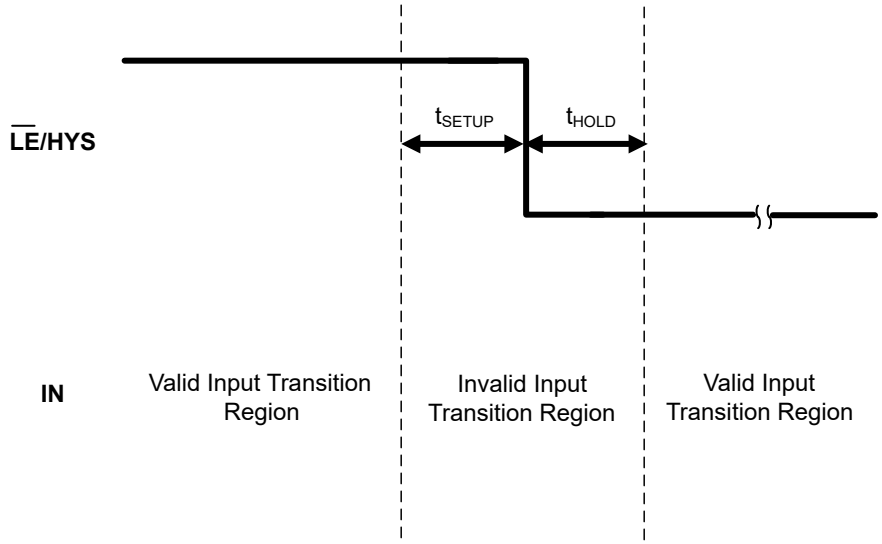


Figure 8-3. Input Change Properly Latched

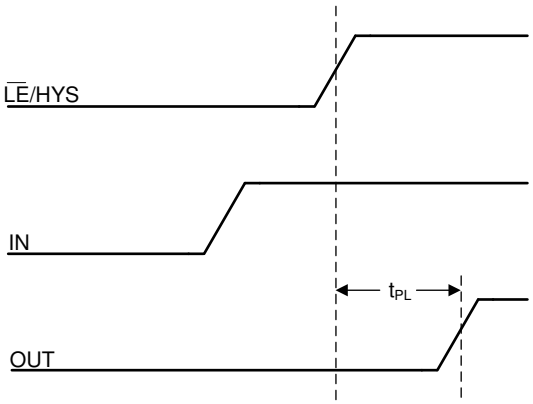


Figure 8-4. Latch Disable with Input Change

8.2 Typical Application

8.2.1 Implementing Hysteresis

A comparator may produce “chatter” (multiple transitions) at the output when there are noise or signal variations around the reference threshold; this causes the output to change states in rapid random successions as the comparator input goes above and below the threshold of the reference. This usually occurs when the input signal

is moving very slowly across the switching threshold of the comparator. This problem can be prevented by using the internal hysteresis feature of the comparator or by the addition of external hysteresis.

The TLV3603-Q1 has a $\overline{LE}$/HYS pin that allows for variable internal hysteresis depending on the resistor value connected between the pin and VEE, where increasing the resistance decreases the hysteresis to a minimum level.

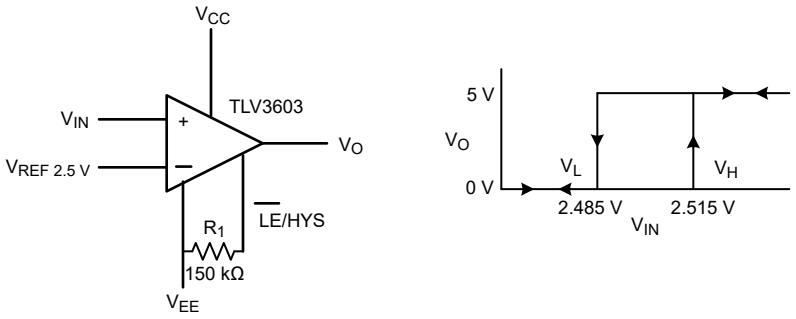


Figure 8-5. Adjustable Hysteresis with a 150kΩ Resistor using TLV3603

Since the TLV3601-Q1 and TLV3602-Q1 only have a minimal amount of internal hysteresis, external hysteresis can be added in the form of a positive feedback loop. A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 8-6.

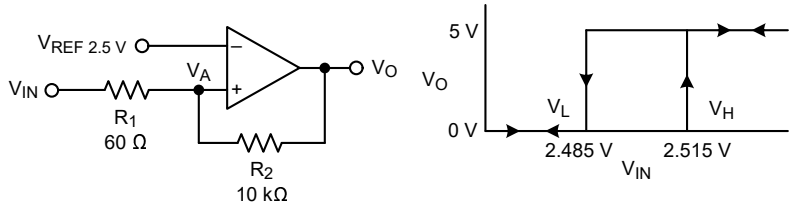


Figure 8-6. Non-Inverting Configuration for Hysteresis using TLV3601

8.2.1.1 Design Requirements

For this design, follow these design requirements.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply Voltage (V_{CC})	5 V
V_{REF}	2.5 V
V_{HYS}	30 mV
Lower Threshold (V_L)	2.485 V
Upper Threshold (V_H)	2.515 V

8.2.1.2 Detailed Design Procedure

For the TLV3603-Q1, the hysteresis vs. resistance curve (Figure 8-2) can be used as a guidance to set the desired amount of hysteresis. Figure 8-2 shows that for a 30-mV hysteresis, a 150 kΩ resistor must be placed from the $\overline{LE}$/HYS pin to VEE.

For the TLV3601-Q1 and TLV3602-Q1, the following procedure can be used to add external hysteresis for a non-inverting configuration. Note that $V_{HYST} << V_{REF}$, so V_{HYST} can be ignored and is not included in the following equations for simpler calculation.

The equivalent resistor networks when the output is high and low are shown in Figure 8-7.

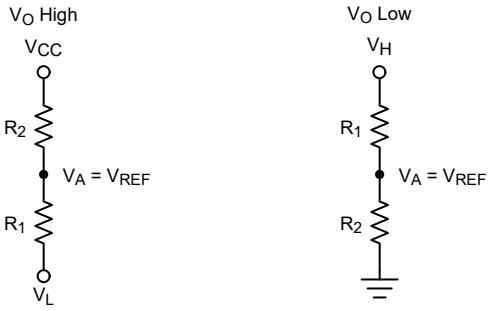


Figure 8-7. Equivalent Resistor Networks for Non-Inverting Configuration with Hysteresis

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_H threshold. Use Equation 1 to calculate V_H.

$$V_H = (R1 \times V_{REF}/R2) + V_{REF} \quad (1)$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below the V_L threshold. Use Equation 2 to calculate V_L.

$$V_L = [V_{REF} (R1 + R2) - V_{CC} \times R1] / R2 \quad (2)$$

The hysteresis of this circuit is the difference between V_H and V_L, as shown in Equation 3.

$$\Delta V_{IN} = V_{HYS} = (V_{CC} \times R1/R2) \quad (3)$$

Select a value for R2. Plug in given values for V_{CC}, V_{REF}, V_H, and V_L **.** For the given example, R2 = 10 kΩ, and R1 is solved as 60 Ω.

For more information, please see Application Notes SNOA997 "Inverting Comparator with Hysteresis Circuit", SBOA313 "Non-Inverting Comparator With Hysteresis Circuit", SBOA219 "Comparator with and without hysteresis circuit".

8.2.1.3 Application Curve

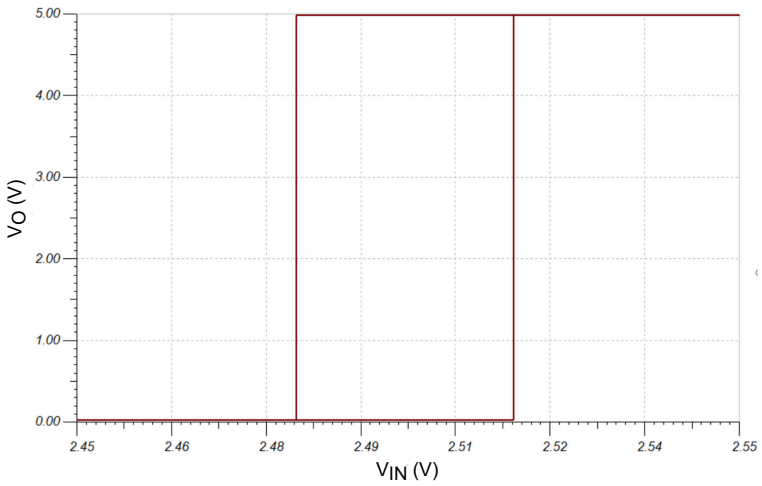


Figure 8-8. Hysteresis Transfer Curve using TLV3601/TLV3603

8.2.2 Optical Receiver

The TLV360x can be used in conjunction with a high speed amplifier such as the OPA858 to create an optical receiver as shown in the figure below. The photodiode is connected to a bias voltage and is being driven with a pulsed laser. The OPA858 takes the current conducting through the diode and translates it into a voltage for a high speed comparator to detect. The comparators will then output the proper output signal according to the threshold set (V_{REF}).

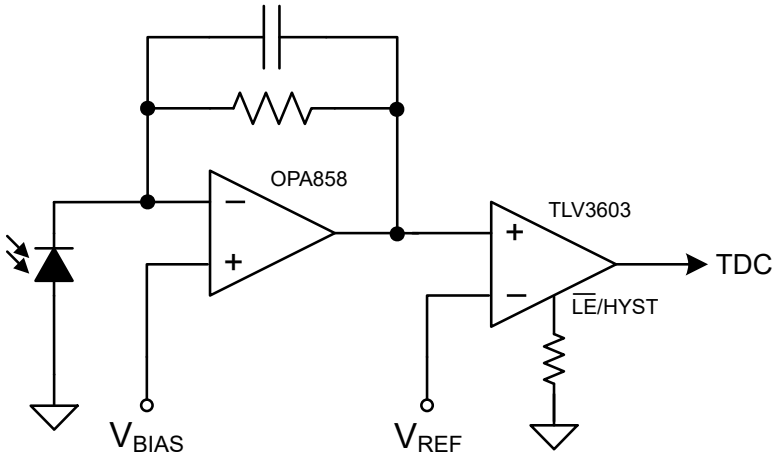


Figure 8-9. Optical Receiver

8.2.3 Over-Current Latch Condition

When it is important for a system to detect a brief over-current condition, it is advisable to utilize the latching feature of the TLV3603-Q1. By latching the comparator output, the MCU is reassured not to miss the over-current occurrence. The circuit below shows one way to implement the latching function.

When an over-current condition is detected by the TLV3603-Q1, the output will go high. The occurrence of the output going high coupled with a logic high from the $\overline{\text{RESET}}$ signal from the MCU will create a logic low signal at the output of the 2-channel NAND gate. This will cause the output of the TLV3603-Q1 to be held in a logic high state (latched), thus allowing the MCU to detect the fault condition regardless of how narrow the over-current condition persists. The addition of the NAND gate also provides a means of clearing the latch state of the comparator once the MCU is done processing the event. This is accomplished by the MCU passing a logic low state to the NAND input causing the $\overline{\text{LE}}$/HYS pin of the comparator to be returned to a logic high state. The TLV3603-Q1 latched status is cleared and the TLV3603-Q1 output can continue to track the status of the input pins.

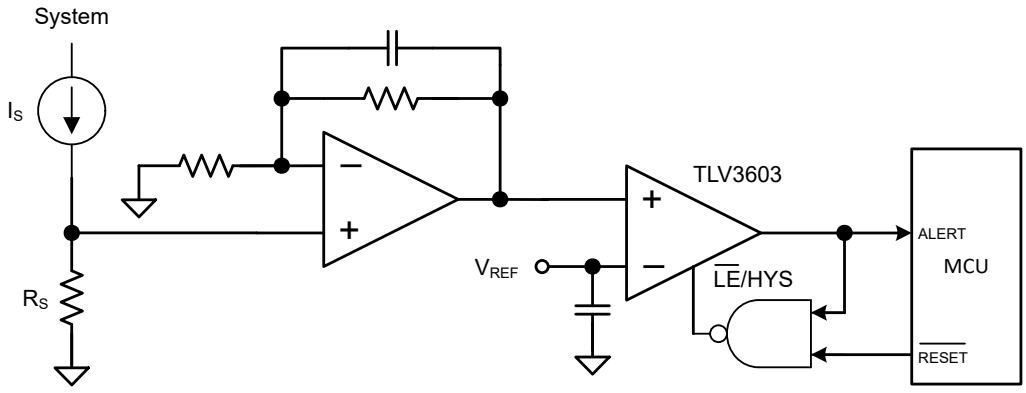


Figure 8-10. Over-Current Latched Output Circuit

8.2.4 External Trigger Function for Oscilloscopes

Below is a typical configuration for creating an external trigger on oscilliscopes. The user adjusts the trigger level by programming a DAC that the TLV360x can use as a reference. The input from an oscilloscope channel is then compared to the trigger reference voltage, and the comparator sends a signal to a downstream FPGA to begin a capture.

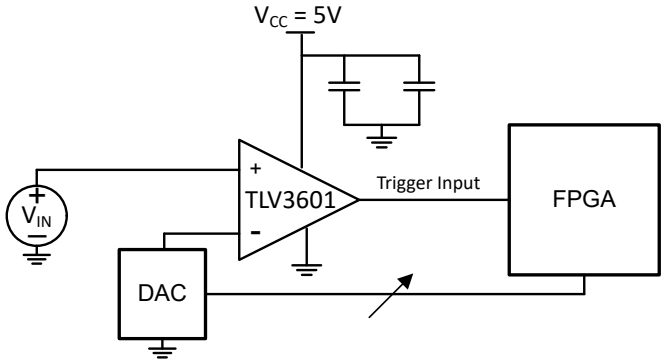


Figure 8-11. External Trigger Function

9 Power Supply Recommendations

The TLV360x are specified for operation from 2.4 V to 5.5 V. While most applications will require single supply operation where VEE is connected to the ground plane and VCC is connected to the intended power supply level, the comparators can also be operated with split supplies. One caution when using split supplies is that the output logic levels are determined by the VCC and VEE levels. For example, if split supplies of +/- 2.5V are used, the output levels will be 2.5V and -2.5V accordingly. In addition, the logic level of the $\overline{LE}$/HYS pin will also be referenced to VEE. This means that the external hysteresis resistor on the TLV3603-Q1 needs to be connected between the $\overline{LE}$/HYS pin and VEE (not to ground) for proper operation.

Regardless of single supply or split supply operation, proper decoupling capacitors are required. It is recommended to use a scheme of multiple, low-ESR ceramic capacitors from the supply pins to the ground plane for optimum performance. A good combination would be 100 pF, 10 nF, and 1 uF with the lowest value capacitor closest to the comparator.

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, adhere to the following layout guidelines.

1. Use a printed-circuit-board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance.

   Likewise, high performance board materials such as Rogers or high speed FR4 is also recommended.
2. Place a decoupling capacitor (100-pF ceramic, surface-mount capacitor) between V_{CC} and

   V_{EE} as close to the device as possible. Using multiple bypass capacitors in different decade ranges such as 100-pF, 100-nF, and 1-µF provides the best noise reduction across frequency ranges.
3. On the inputs and the output, keep lead lengths as short and minimize capacitive coupling to the traces by having a keepout area around the traces that is 3x the width of the traces. It is also recommended to keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.

10.2 Layout Example

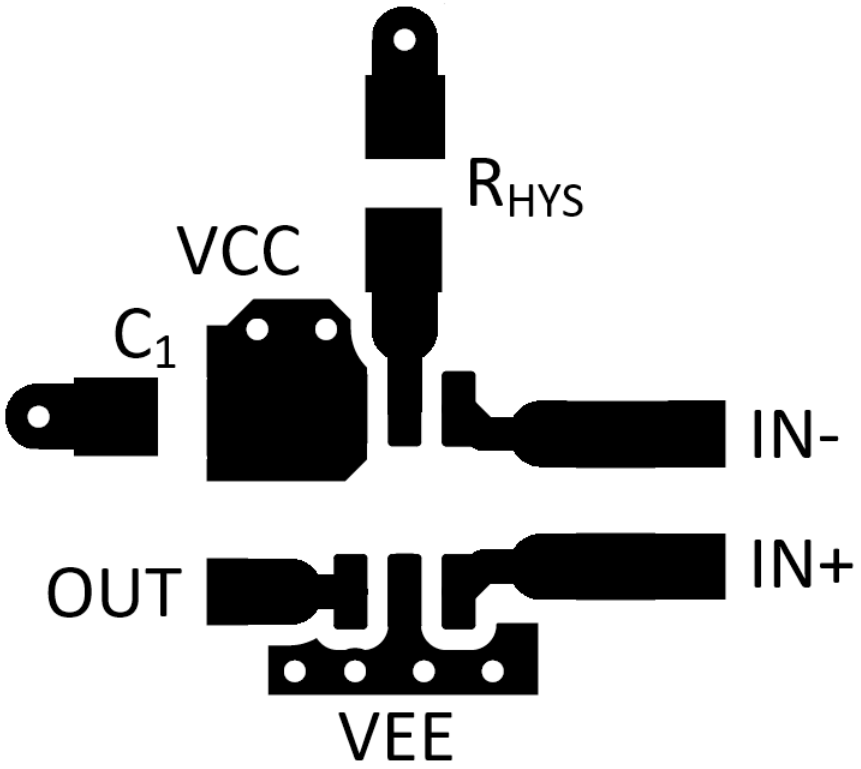


Figure 10-1. TLV3603 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LIDAR Pulsed Time of Flight Reference Design

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3601QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	601Q	Samples
TLV3601QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1JG	Samples
TLV3602QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	602Q	Samples
TLV3603QDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1JH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3601-Q1, TLV3602-Q1, TLV3603-Q1 :

- Catalog : TLV3601, TLV3602, TLV3603

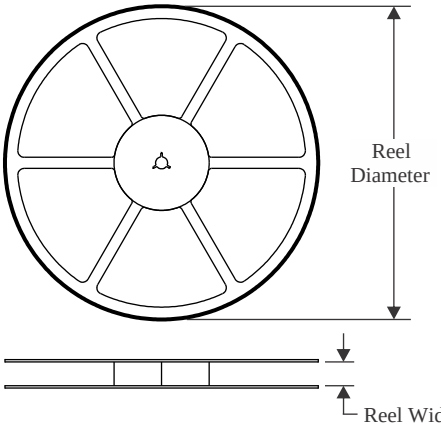
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

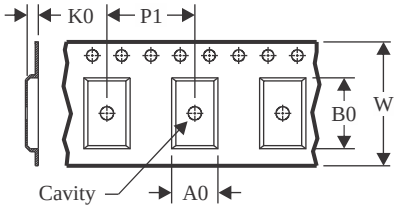
27-Mar-2024

TAPE AND REEL INFORMATION

REEL DIMENSIONS

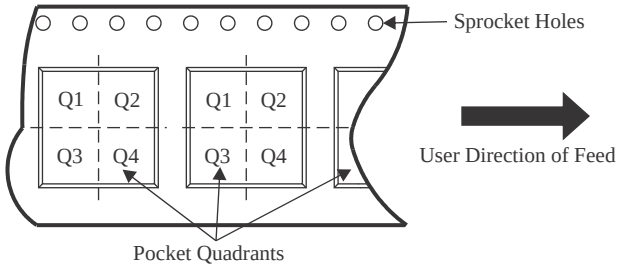


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



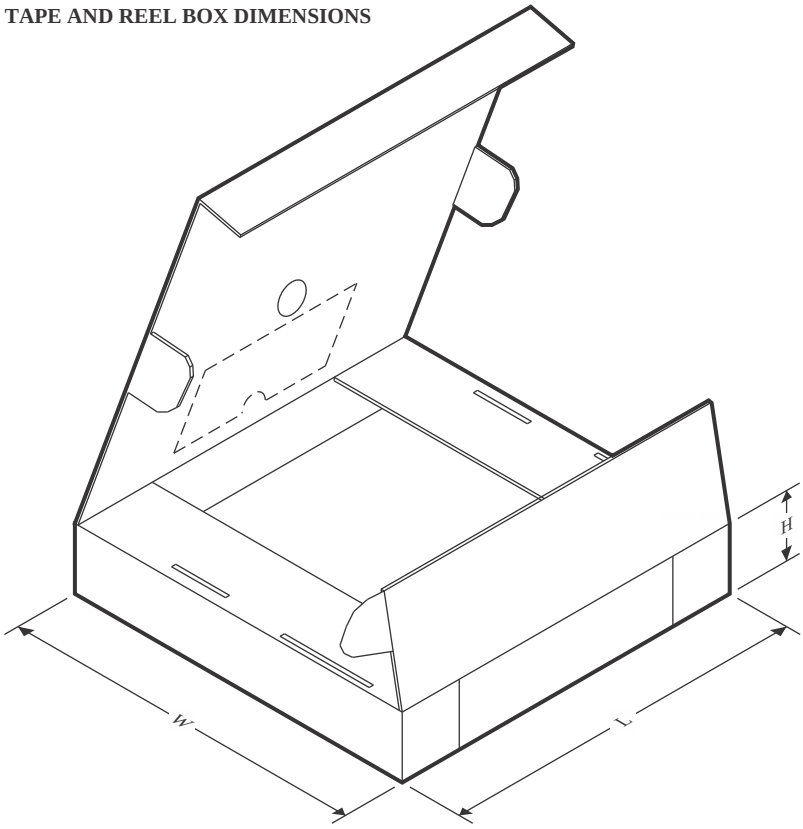
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3601QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3601QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TLV3602QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3603QDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

27-Mar-2024

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

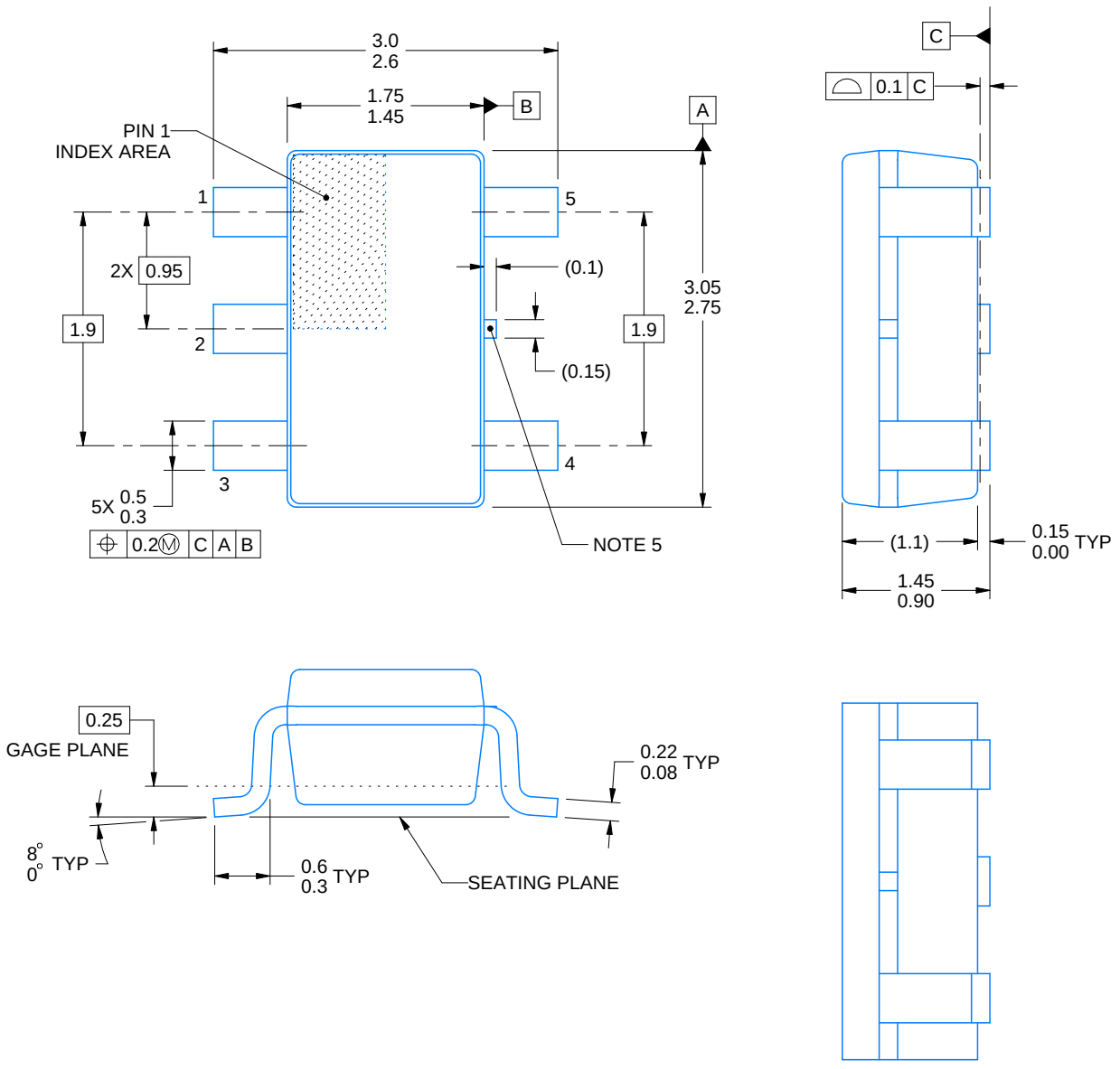
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3601QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV3601QDCKRQ1	SC70	DCK	5	3000	183.0	183.0	20.0
TLV3602QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV3603QDCKRQ1	SC70	DCK	6	3000	183.0	183.0	20.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214839/J 02/2024

NOTES:

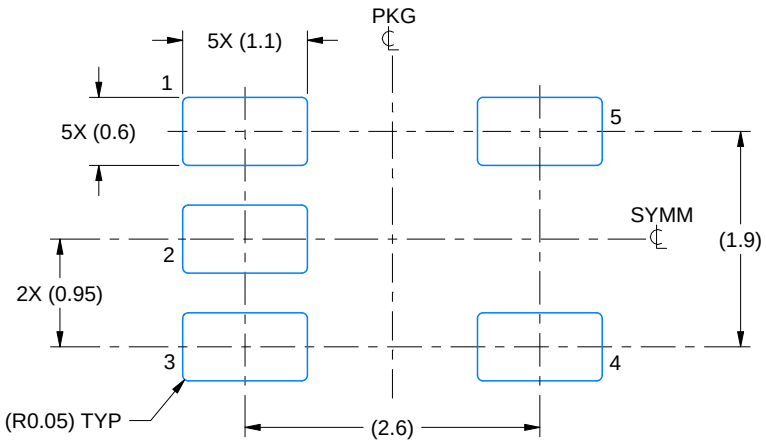
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

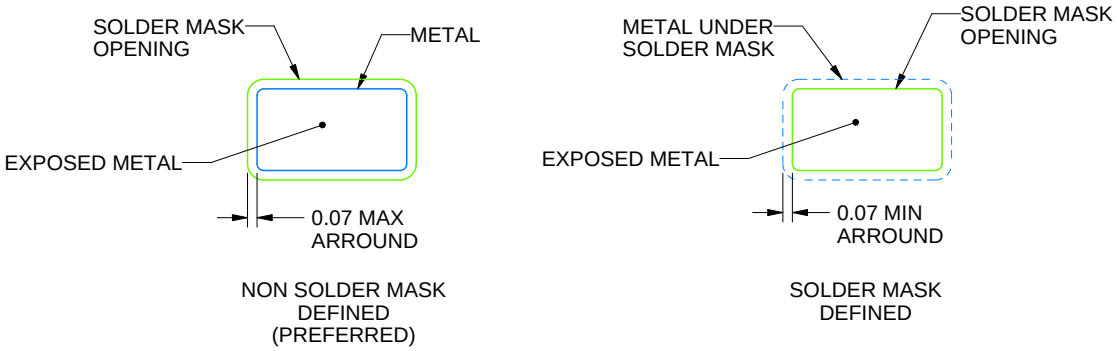
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

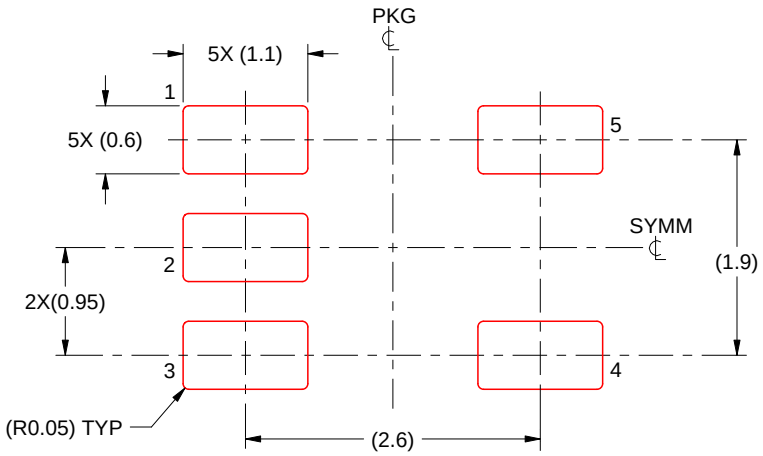
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

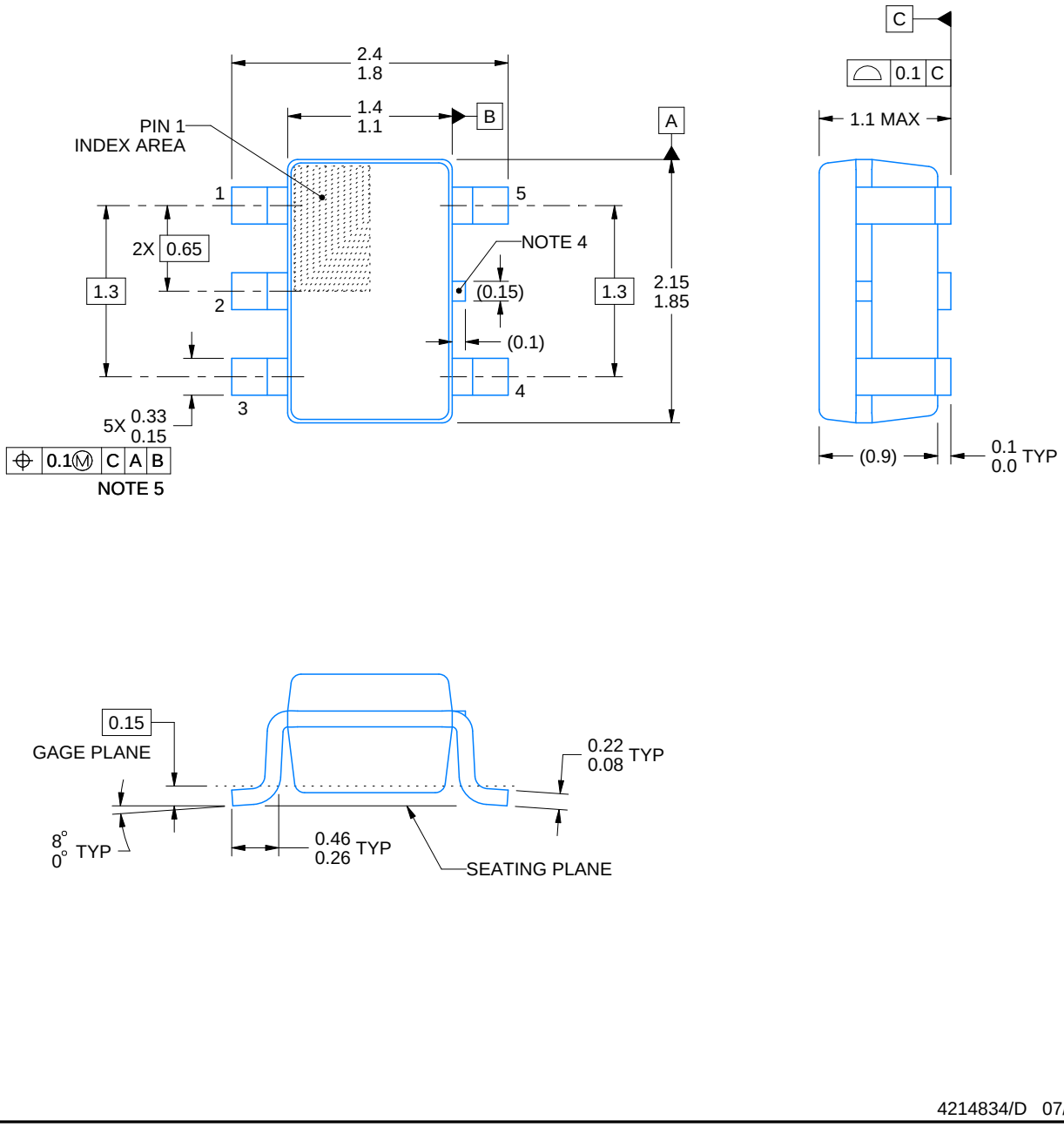
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/D 07/2023

NOTES:

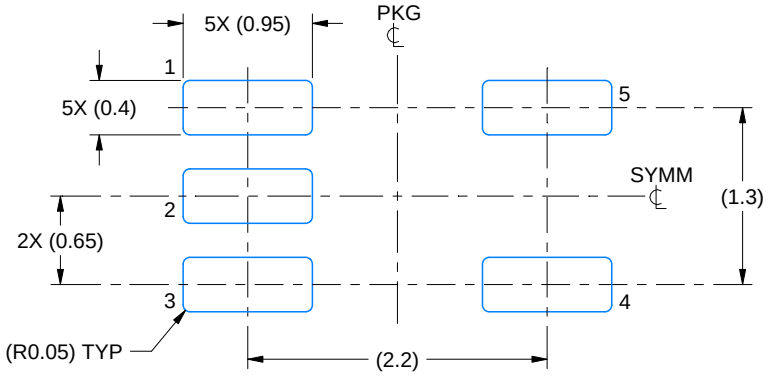
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.

EXAMPLE BOARD LAYOUT

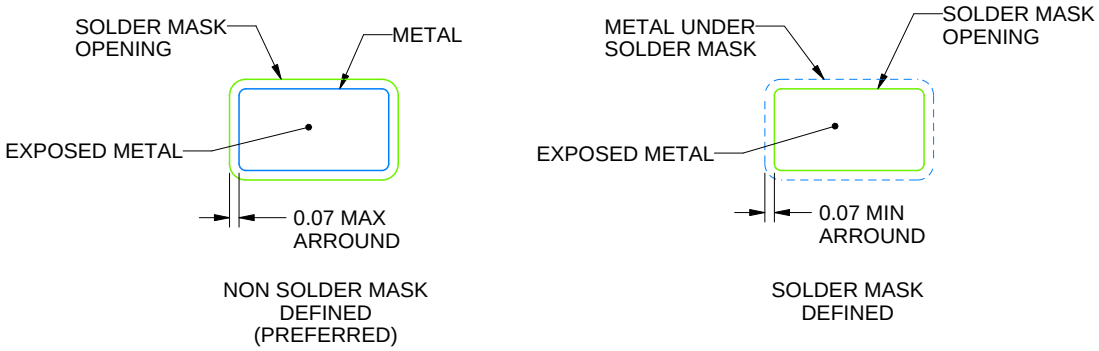
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

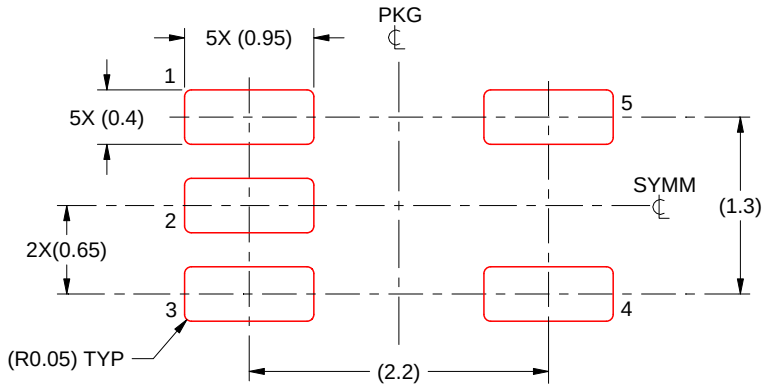
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

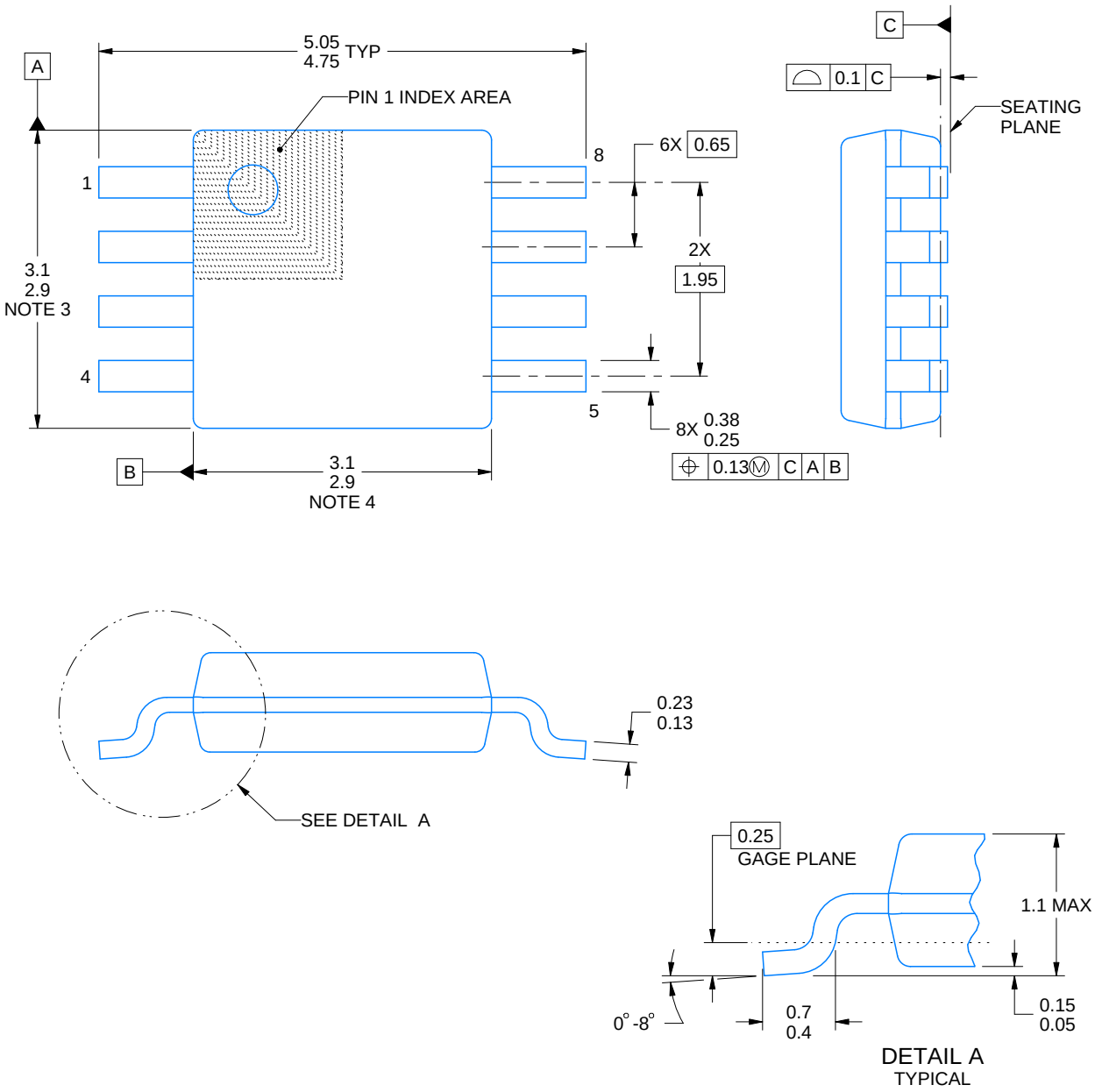
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

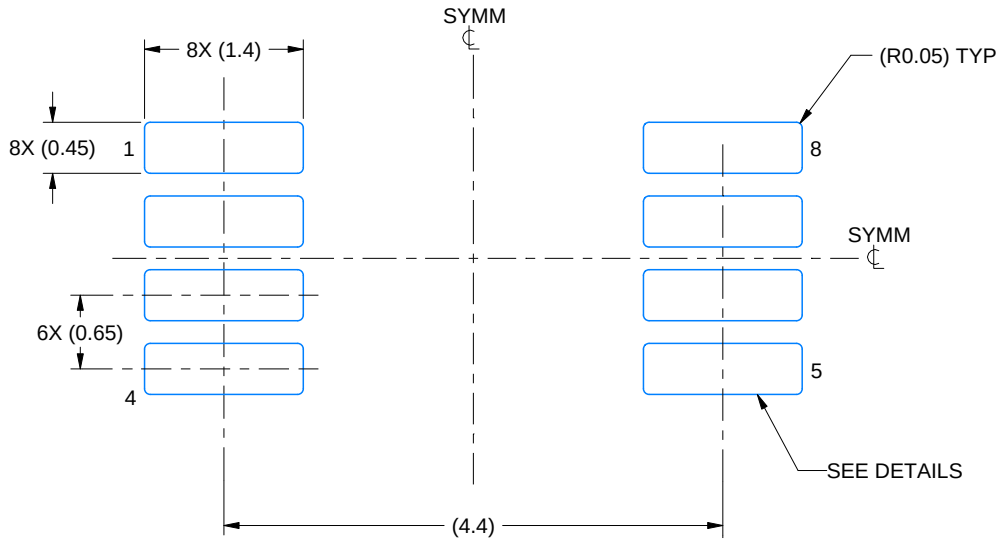


4214862/A 04/2023

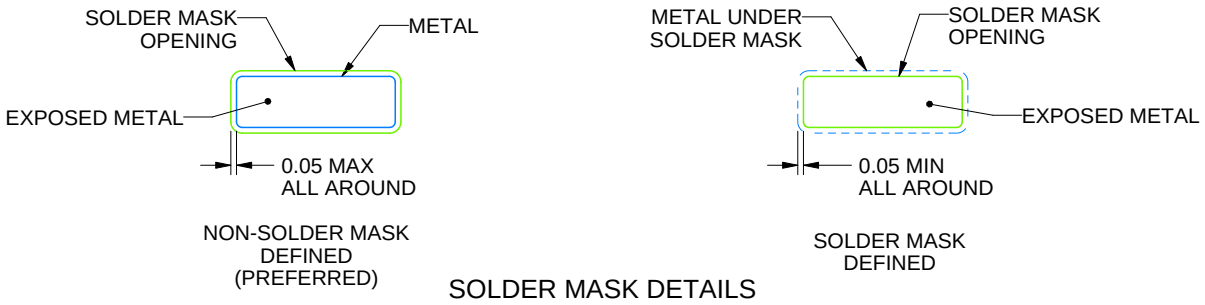
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

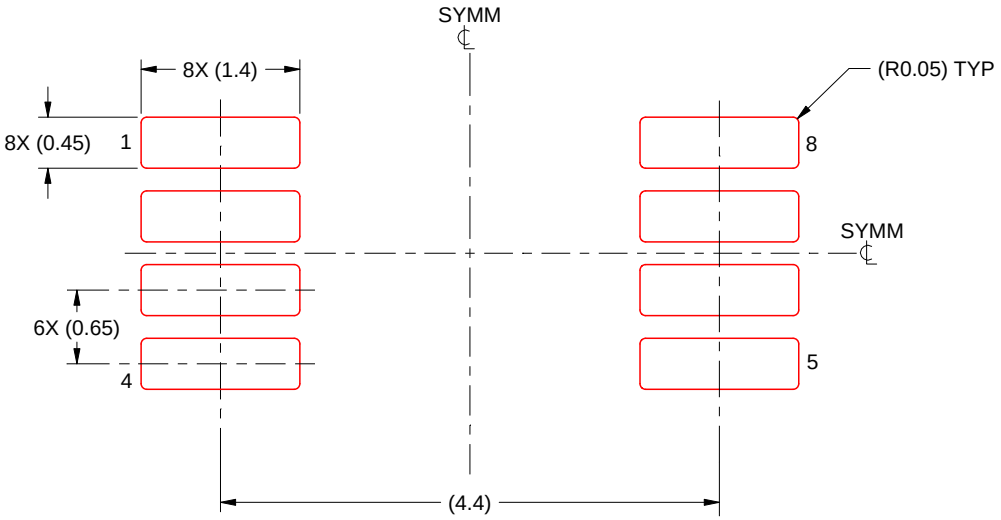
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

VSSOP™ - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

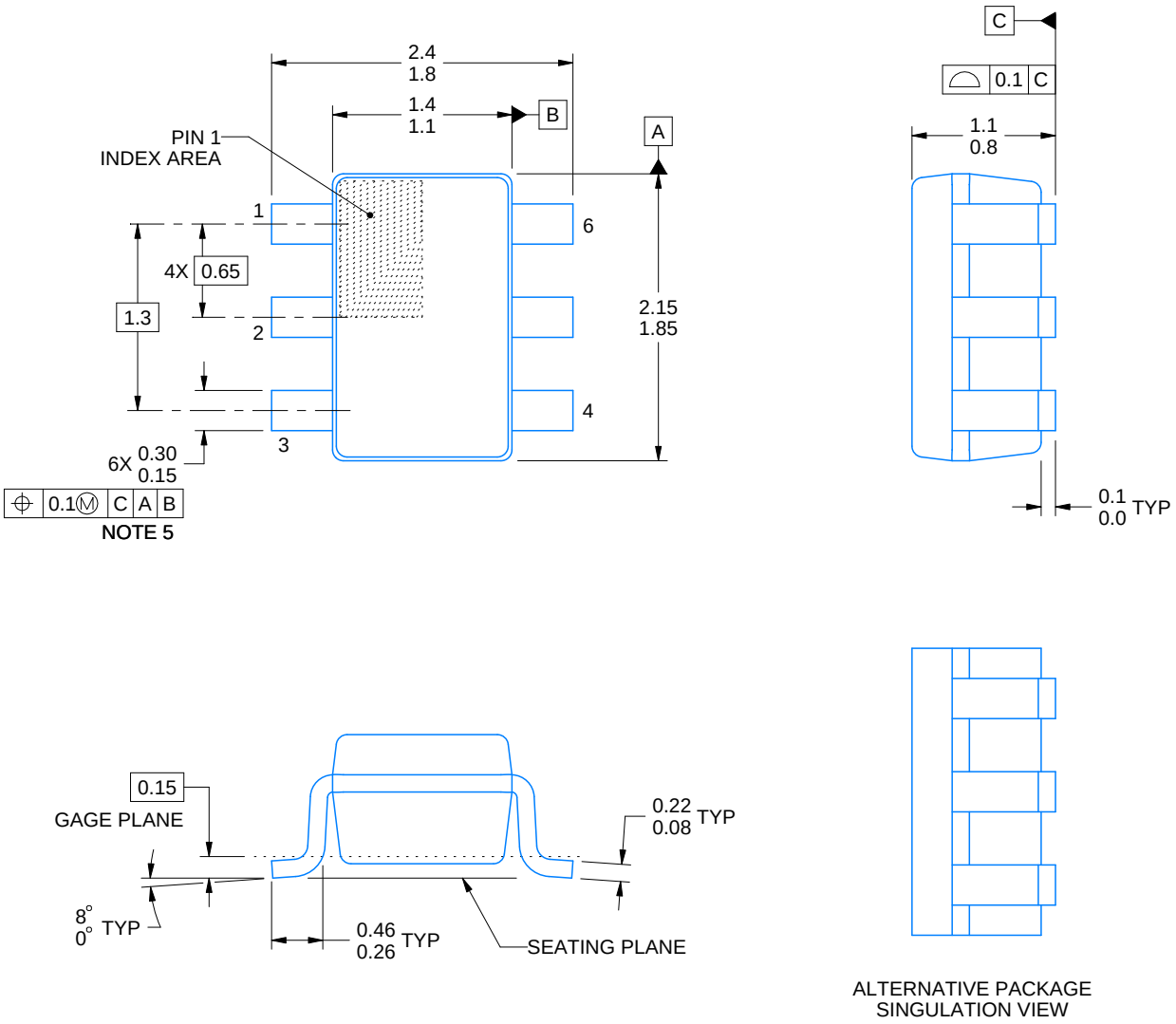
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DCK0006A

PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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NOTES:

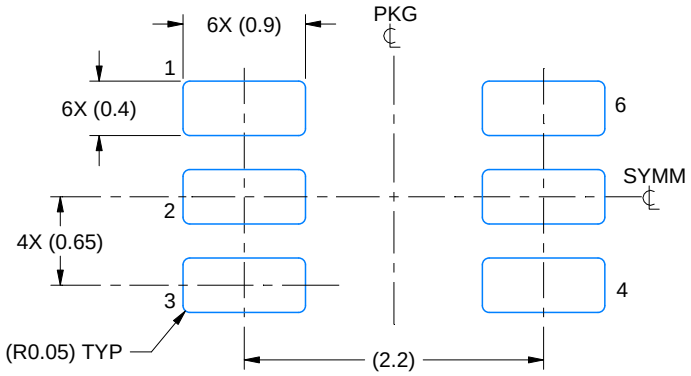
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.

EXAMPLE BOARD LAYOUT

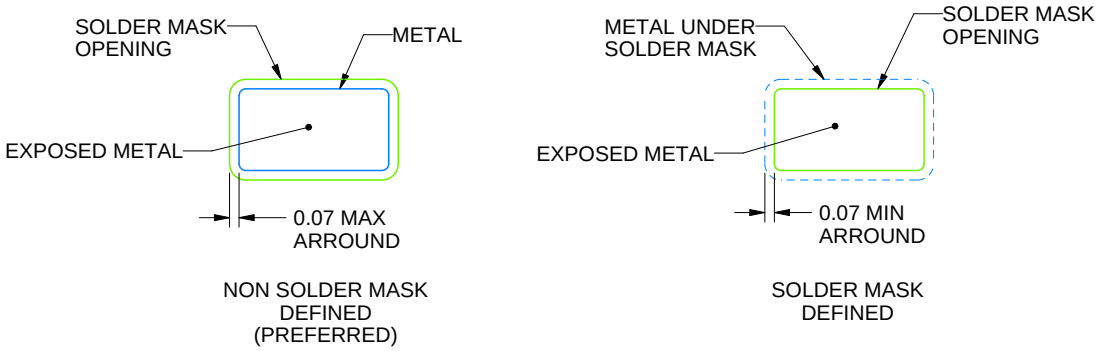
DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

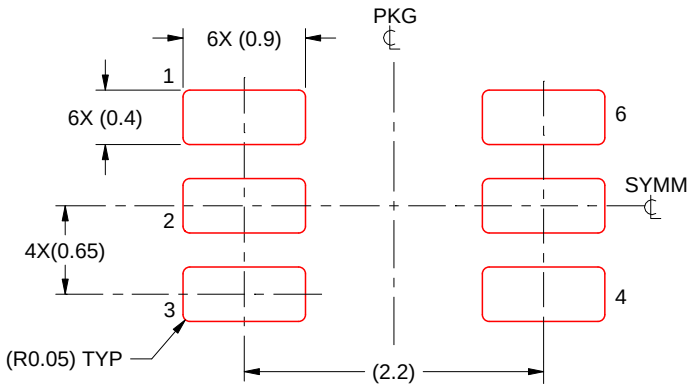
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.