74HC595Q/74HCT595Q Automotive, 8-Bit Serial-In/Serial-Out or Parallel-Out Shift Registers with 3-State Controlled Outputs

GENERAL DESCRIPTION

The 74HC595Q and 74HCT595Q are 8-bit serial-in/serial-out or parallel-out shift registers with 3-state controlled outputs designed for power supply voltage ranges of 2.0V to 5.5V and 4.5V to 5.5V respectively.

These devices integrate an 8-bit shift register, an 8-bit storage register, and parallel 3-state outputs respectively. The shift register provides a master reset input ($\overline{MR}$), a serial input (DS) and a serial output (Q7S) for cascading. All of the 8 shift register stages have the asynchronous reset function when $\overline{MR}$ is low.

Both the shift register and storage register have separate clocks. The shift register clock (SHCP) is positive-edge triggered. Data is shifted on the positive-going transition of the SHCP. The storage register clock (STCP) is also positive-edge triggered. The data in each shift register is transferred to the storage register on the positive-going transition of the STCP. If the SHCP and STCP are connected together, the shift register always leads one clock pulse than the storage register all the time. The output enable $\overline{OE}$ input is active-low. When $\overline{OE}$ is held low, the data in storage register appears at the outputs. When $\overline{OE}$ is held high, all parallel outputs are in high-impedance state. $\overline{OE}$ has no influence on the inner working of the registers. The clamp diodes of inputs allow the use of current limiting resistors to connect inputs to the voltage exceeding supply voltage.

These devices are AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and they are suitable for automotive applications.

The 74HC595Q and 74HCT595Q are available in Green TSSOP-16 and SOIC-16 packages. They operate over a temperature range of -40℃ to +125℃.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Supply Voltage Range**
  - **74HC595Q: 2.0V to 5.5V**
  - **74HCT595Q: 4.5V to 5.5V**
- **8-Bit Serial-In/Serial or Parallel-Out Shift Registers**
- **Storage Registers Have 3-State Outputs**
- **Direct Clear Inputs of Shift Registers**
- **Input Levels**
  - **74HC595Q: CMOS Input Level**
  - **74HCT595Q: TTL Input Level**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TSSOP-16 and SOIC-16 Packages**

APPLICATIONS

Automotive Applications
Medical Equipment

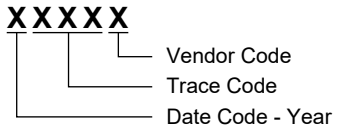
代理商 威尔逊 www.viswie.com 联系电话 138 2526 5270

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
74HC595Q	TSSOP-16	-40℃ to +125℃	74HC595QTS16G/TR	1B2TS16 XXXXX	Tape and Reel, 4000
	SOIC-16	-40℃ to +125℃	74HC595QS16G/TR	1B3S16 XXXXX	Tape and Reel, 2500
74HCT595Q	TSSOP-16	-40℃ to +125℃	74HCT595QTS16G/TR	117TS16 XXXXX	Tape and Reel, 4000
	SOIC-16	-40℃ to +125℃	74HCT595QS16G/TR	14CS16 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CC} ..... -0.5V to 7.0V
Input Voltage Range, V_I [(1)] .... -0.5V to MIN(7.0V, V_{CC} + 0.5V)
Output Voltage Range, V_O [(1)] -0.5V to MIN(7.0V, V_{CC} + 0.5V)
Input Clamp Current, I_{IK} (V_I < -0.5V or V_I > V_{CC} + 0.5V)
..... ±20mA
Output Clamp Current, I_{OK} (V_O < -0.5V or V_O > V_{CC} + 0.5V)
..... ±20mA
Output Current, I_O (V_O = -0.5V to V_{CC} + 0.5V)
Pin Q7S..... ±25mA
Pins Qn ..... ±35mA
Supply Current, I_{CC} 70mA
Ground Current, I_{GND}..... -70mA
Junction Temperature [(2)] ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility [(3)] [(4)]
HBM..... ±8000V
CDM ..... ±1000V

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

3. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

4. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC}
For 74HC595Q ..... 2.0V to 5.5V
For 74HCT595Q ..... 4.5V to 5.5V
Input Voltage Range, V_I..... 0V to V_{CC}
Output Voltage Range, V_O..... 0V to V_{CC}
Input Transition Rise or Fall Rate, Δt/ΔV
For 74HC595Q
V_{CC} = 2.0V ..... 625ns/V (MAX)
V_{CC} = 4.5V ..... 1.67ns/V (TYP), 139ns/V (MAX)
V_{CC} = 5.5V ..... 83ns/V (MAX)
For 74HCT595Q
V_{CC} = 4.5V ..... 1.67ns/V (TYP), 139ns/V (MAX)
Operating Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

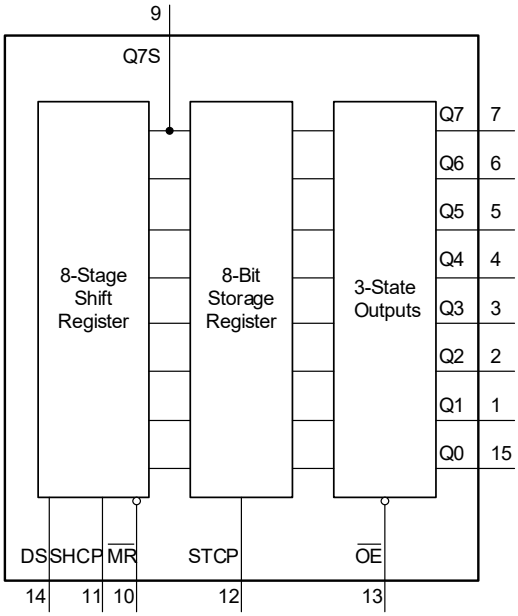
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

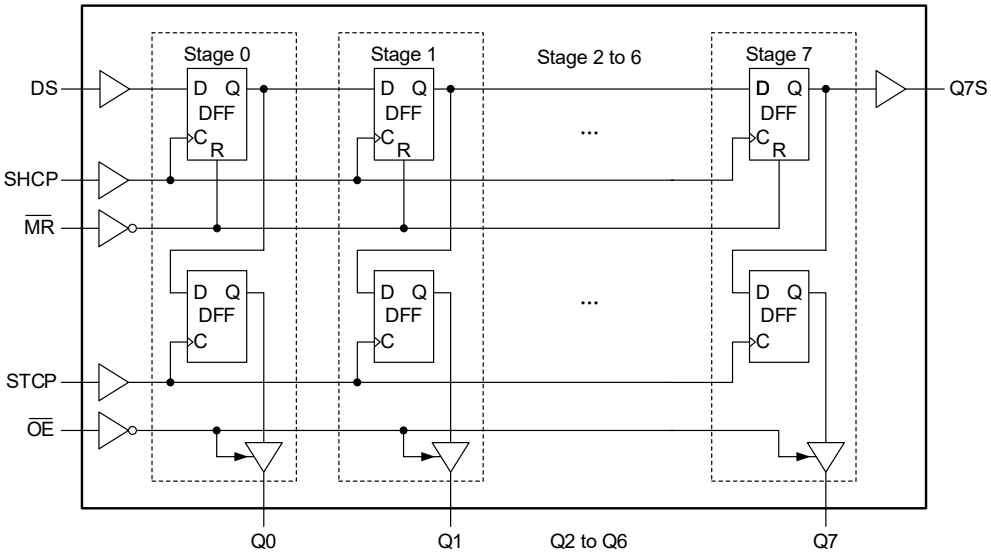
DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

CONTROL INPUTS				INPUT	OUTPUTS		FUNCTION
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	*X*	L	L	*X*	L	NC	When $\overline{MR}$ is low, it only affects the shift register.
X	↑	L	L	*X*	L	L	Load the empty shift register into the storage register.
X	*X*	H	L	*X*	L	Z	Shift register is reset and all parallel outputs are in high-impedance state.
↑	*X*	L	H	H	Q6S	NC	When shift register stage 0 goes high, data of all shift register stages shifted through, e.g. the serial output (Q7S) presents the previous state of stage 6 (internal Q6S).
X	↑	L	H	*X*	NC	QnS	Data of shift register (internal QnS) is transferred to the storage register and parallel output stages.
↑	↑	L	H	*X*	Q6S	QnS	Data of shift register shifted through, previous data of the shift register is transferred to the storage register and parallel output stages.

H = High Voltage Level

L = Low Voltage Level

↑ = Low-to-High Clock Transition

Z = High-Impedance State

NC = No Change

X = Don't Care

TIMING DIAGRAM

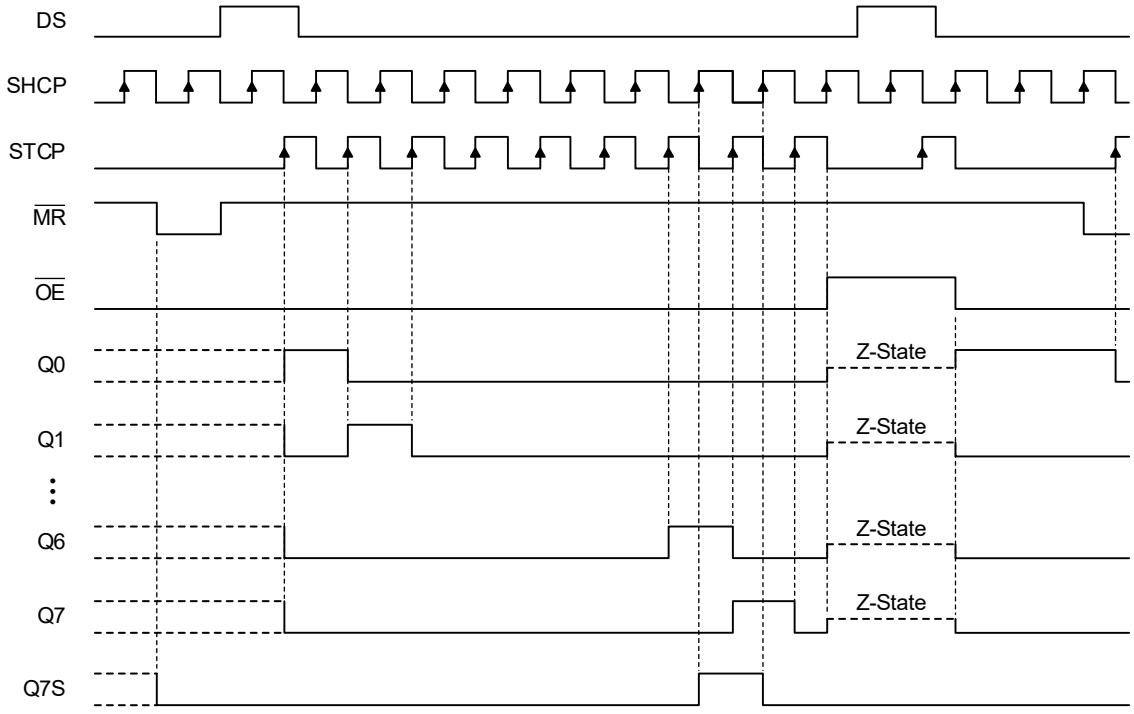
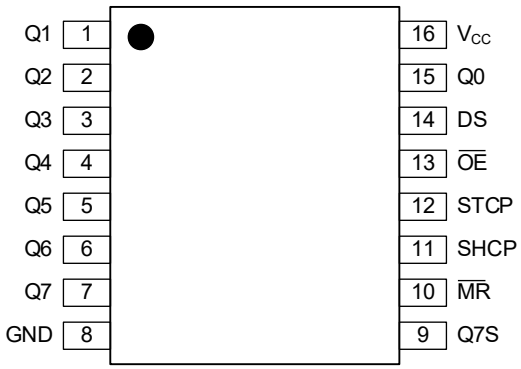


Figure 1. Timing Diagram

PIN CONFIGURATIONS

(TOP VIEW)



TSSOP-16/SOIC-16

PIN DESCRIPTION

PIN	NAME	FUNCTION
15, 1, 2, 3, 4, 5, 6, 7	Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	Parallel Data Outputs.
8	GND	Ground.
9	Q7S	Serial Data Output.
10	$\overline{MR}$	Master Reset Input (Active-Low).
11	SHCP	Shift Register Clock Input (Rising Edge Triggered).
12	STCP	Storage Register Clock Input (Rising Edge Triggered).
13	$\overline{OE}$	Output Enable Input (Active-Low).
14	DS	Serial Data Input.
16	V_{CC}	Power Supply.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
74HC595Q								
High-Level Input Voltage	V_{IH}	V_{CC} = 2.0V		Full	1.50			V
		V_{CC} = 4.5V		Full	3.15			
		V_{CC} = 5.5V		Full	3.85			
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.0V		Full			0.50	V
		V_{CC} = 4.5V		Full			1.35	
		V_{CC} = 5.5V		Full			1.65	
High-Level Output Voltage	V_{OH}	All outputs	V_{CC} = 2.0V, I_{OH} = -20μA	Full	1.9	1.998		V
			V_{CC} = 4.5V, I_{OH} = -20μA	Full	4.4	4.499		
			V_{CC} = 5.5V, I_{OH} = -20μA	Full	5.4	5.499		
		Q7S output	V_{CC} = 4.5V, I_{OH} = -4mA	Full	3.7	4.35		
			V_{CC} = 5.5V I_{OH} = -5.2mA	Full	4.77	5.33		
		Qn bus driver outputs	V_{CC} = 4.5V, I_{OH} = -6mA	Full	3.7	4.30		
			V_{CC} = 5.5V, I_{OH} = -7.8mA	Full	4.77	5.27		
Low-Level Output Voltage	V_{OL}	All outputs	V_{CC} = 2.0V, I_{OL} = 20μA	Full		0.002	0.1	V
			V_{CC} = 4.5V, I_{OL} = 20μA	Full		0.001	0.1	
			V_{CC} = 5.5V, I_{OL} = 20μA	Full		0.001	0.1	
		Q7S output	V_{CC} = 4.5V, I_{OL} = 4mA	Full		0.16	0.4	
			V_{CC} = 5.5V I_{OL} = 5.2mA	Full		0.19	0.4	
		Qn bus driver outputs	V_{CC} = 4.5V, I_{OL} = 6mA	Full		0.18	0.4	
			V_{CC} = 5.5V, I_{OL} = 7.8mA	Full		0.22	0.4	
Input Leakage Current	I_I	V_{CC} = 5.5V, V_I = V_{CC} or GND		Full		±0.01	±1	μA
Off-State Output Current	I_{OZ}	V_{CC} = 5.5V, V_I = V_{IH} or V_{IL}, V_O = V_{CC} or GND		Full		±0.01	±5	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, V_I = V_{CC} or GND, I_O = 0A		Full		0.02	5	μA
Input Capacitance	C_I			+25℃		7		pF
74HCT595Q								
High-Level Input Voltage	V_{IH}	V_{CC} = 4.5V to 5.5V		Full	2			V
Low-Level Input Voltage	V_{IL}	V_{CC} = 4.5V to 5.5V		Full			0.8	V
High-Level Output Voltage	V_{OH}	All outputs	V_{CC} = 4.5V, I_{OH} = -20μA	Full	4.4	4.499		V
		Q7S output	V_{CC} = 4.5V, I_{OH} = -4mA	Full	3.84	4.35		
		Qn bus driver outputs	V_{CC} = 4.5V, I_{OH} = -6mA	Full	3.84	4.30		
Low-Level Output Voltage	V_{OL}	All outputs	V_{CC} = 4.5V, I_{OL} = 20μA	Full		0.001	0.1	V
		Q7S output	V_{CC} = 4.5V, I_{OL} = 4mA	Full		0.15	0.33	
		Qn bus driver outputs	V_{CC} = 4.5V, I_{OL} = 6mA	Full		0.18	0.33	
Input Leakage Current	I_I	V_{CC} = 5.5V, V_I = V_{CC} or GND		Full		±0.01	±1	μA
Off-State Output Current	I_{OZ}	V_{CC} = 5.5V, V_I = V_{IH} or V_{IL}, V_O = V_{CC} or GND		Full		±0.01	±5	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, V_I = V_{CC} or GND, I_O = 0A		Full		0.05	5	μA
Additional Supply Current	ΔI_{CC}	$\overline{MR}$, SHCP, STCP and $\overline{OE}$ pins	Per input pin, other inputs at V_{CC} or GND, V_{CC} = 4.5V to 5.5V, V_I = V_{CC} - 2.1V, I_O = 0A	Full		65	120	μA
		DS pin		Full		65	120	
Input Capacitance	C_I			+25℃		3.5		pF

DYNAMIC CHARACTERISTICS

(See Figure 2 for test circuit. Full = -40℃ to +125℃, C_L = 50pF, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
74HC595Q								
Propagation Delay (2)	t_{PD}	SHCP to Q7S, see Figure 3	V_{CC} = 2.0V	Full	5	55.0	112.8	ns
			V_{CC} = 4.5V	Full	5	21.0	38.3	
			V_{CC} = 5.5V	Full	5	18.0	32.7	
		STCP to Qn, see Figure 4	V_{CC} = 2.0V	Full	5	55.0	108.8	
			V_{CC} = 4.5V	Full	5	21.0	36.0	
			V_{CC} = 5.5V	Full	5	20.0	30.7	
High-to-Low Propagation Delay	t_{PHL}	$\overline{MR}$ to Q7S, see Figure 6	V_{CC} = 2.0V	Full	5	40.0	83.4	ns
			V_{CC} = 4.5V	Full	3	15.0	27.5	
			V_{CC} = 5.5V	Full	3	13.0	23.7	
Enable Time (2)	t_{EN}	$\overline{OE}$ to Qn, see Figure 7	V_{CC} = 2.0V	Full	1	20.0	35.3	ns
			V_{CC} = 4.5V	Full	1	8.0	12.4	
			V_{CC} = 5.5V	Full	1	8.0	11.2	
Disable Time (2)	t_{DIS}	$\overline{OE}$ to Qn, see Figure 7	V_{CC} = 2.0V	Full	1	15.0	20.7	ns
			V_{CC} = 4.5V	Full	0.5	10.0	14.8	
			V_{CC} = 5.5V	Full	0.5	10.0	14.3	
Maximum Frequency	f_{MAX}	SHCP or STCP, see Figure 3 and Figure 4	V_{CC} = 2.0V	Full	5	30		MHz
			V_{CC} = 4.5V	Full	50	100		
			V_{CC} = 5.5V	Full	60	105		
Pulse Width	t_W	SHCP high or low, see Figure 3	V_{CC} = 2.0V	Full	38			ns
			V_{CC} = 4.5V	Full	16			
			V_{CC} = 5.5V	Full	13			
		STCP high or low, see Figure 4	V_{CC} = 2.0V	Full	38			
			V_{CC} = 4.5V	Full	16			
			V_{CC} = 5.5V	Full	13			
		$\overline{MR}$ low, see Figure 6	V_{CC} = 2.0V	Full	55			
			V_{CC} = 4.5V	Full	16			
			V_{CC} = 5.5V	Full	16			
Setup Time	t_{SU}	DS to SHCP, see Figure 5	V_{CC} = 2.0V	Full	30			ns
			V_{CC} = 4.5V	Full	10			
			V_{CC} = 5.5V	Full	9			
		SHCP to STCP (3), see Figure 4	V_{CC} = 2.0V	Full	60			
			V_{CC} = 4.5V	Full	20			
			V_{CC} = 5.5V	Full	16			
Hold Time	t_H	DS to SHCP, see Figure 5	V_{CC} = 2.0V	Full	0.5			ns
			V_{CC} = 4.5V	Full	0.5			
			V_{CC} = 5.5V	Full	0.5			
Recovery Time	t_{REC}	$\overline{MR}$ to SHCP, see Figure 6	V_{CC} = 2.0V	Full	0.5			ns
			V_{CC} = 4.5V	Full	0.5			
			V_{CC} = 5.5V	Full	0.5			
Power Dissipation Capacitance (4) (5)	C_{PD}	f_i = 1MHz, V_I = GND to V_{CC}		+25℃		35		pF

DYNAMIC CHARACTERISTICS (continued)

(See Figure 2 for test circuit. Full = -40℃ to +125℃, C_L = 50pF, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN (1)	TYP	MAX (1)	UNITS
74HCT595Q (V_{CC} = 4.5V to 5.5V)							
Propagation Delay (2)	t_{PD}	SHCP to Q7S, see Figure 3	Full	5	21.0	38.9	ns
		STCP to Qn, see Figure 4	Full	5	21.0	36.2	
High-to-Low Propagation Delay	t_{PHL}	$\overline{MR}$ to Q7S, see Figure 6	Full	2	16.0	31.9	ns
Enable Time (2)	t_{EN}	$\overline{OE}$ to Qn, see Figure 7	Full	0.5	9.0	17.4	ns
Disable Time (2)	t_{DIS}	$\overline{OE}$ to Qn, see Figure 7	Full	2	10.0	14.0	ns
Maximum Frequency	f_{MAX}	SHCP or STCP, see Figure 3 and Figure 4	Full	25	50		MHz
Pulse Width	t_W	SHCP high or low, see Figure 3	Full	15			ns
		STCP high or low, see Figure 4	Full	15			
		$\overline{MR}$ low, see Figure 6	Full	25			
Setup Time	t_{SU}	DS to SHCP, see Figure 5	Full	18			ns
		SHCP to STCP (3), see Figure 4	Full	20			
Hold Time	t_H	DS to SHCP, see Figure 5	Full	0.5			ns
Recovery Time	t_{REC}	$\overline{MR}$ to SHCP, see Figure 6	Full	0.5			ns
Power Dissipation Capacitance (4) (5)	C_{PD}	f_i = 1MHz, V_I = GND to V_{CC} - 1.5V	+25℃		40		pF

NOTES:

1. Specified by design and characterization, not production tested.

2. t_{PD} is the same as t_{PHL} and t_{PLH}. t_{EN} is the same as t_{PZL} and t_{PZH}. t_{DIS} is the same as t_{PLZ} and t_{PHZ}.

3. The setup time enables the storage register to get stable data from the shift register. In this case where clocks can be tied together, the shift register is a clock pulse in front of the storage register.

4. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

where:

f_i = Input frequency in MHz.

f_o = Output frequency in MHz.

C_L = Output load capacitance in pF.

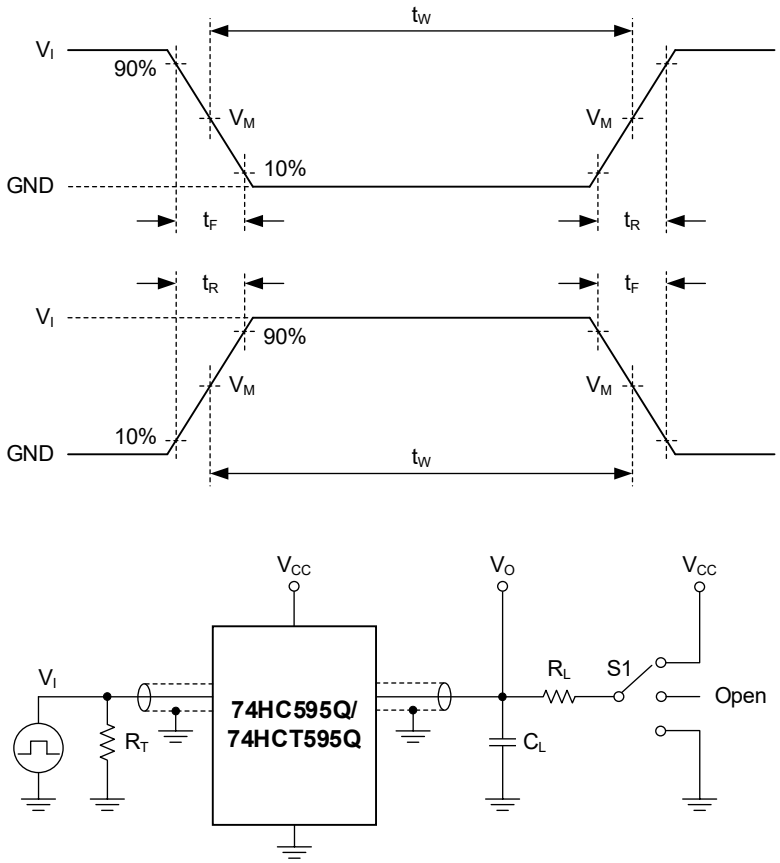
V_{CC} = Supply voltage in Volts.

N = Number of inputs switching.

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

5. All 9 outputs switching.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

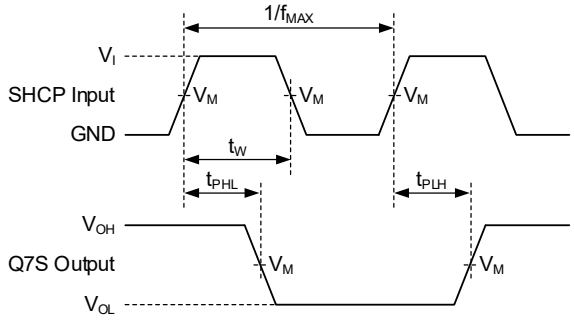
S1: Test selection switch.

Figure 2. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

MODEL	INPUT		LOAD		S1 POSITION		
	V_I	t_R, t_F	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC595Q	V_{CC}	≤ 6ns	50pF	1kΩ	Open	GND	V_{CC}
74HCT595Q	3V	≤ 6ns	50pF	1kΩ	Open	GND	V_{CC}

WAVEFORMS

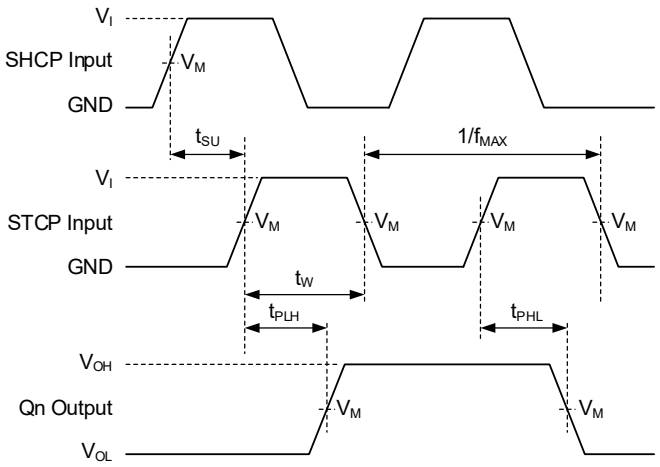


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Shift Register Clock Input to Output Propagation Delay Times, Pulse Width and Maximum Frequency

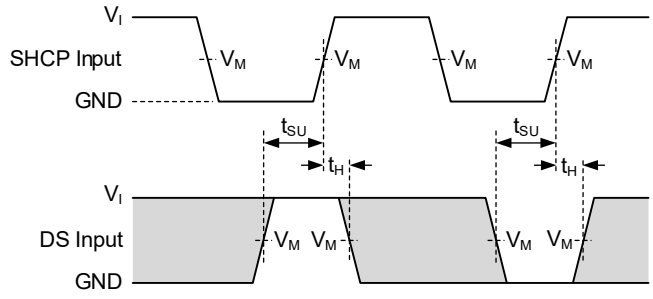


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Storage Register Clock Input to Output Propagation Delay Times, Shift Register Clock to Storage Register Clock Setup time, Pulse Width and Maximum Frequency



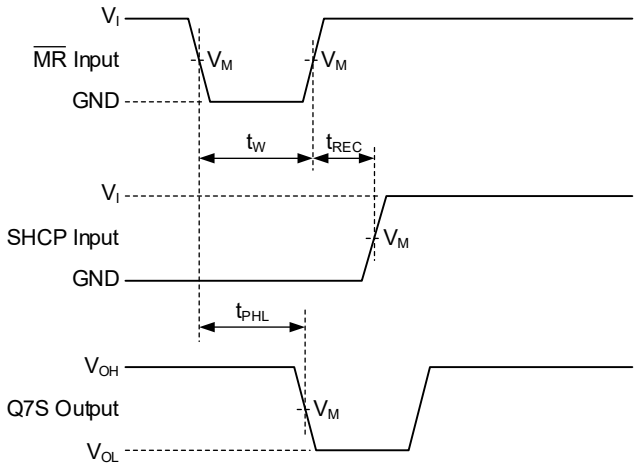
Test conditions are given in Table 1.

Measurement points are given in Table 2.

The shaded areas refer to when the input is allowed to change for predictable output performance.

Figure 5. Data Setup and Hold Times

WAVEFORMS (continued)

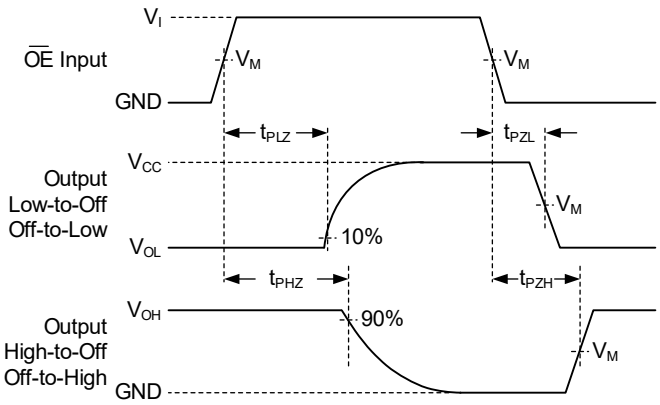


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. Master Reset Input to Output Propagation Delay Times, Pulse Width and Recovery Time



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. Enable and Disable Times

Table 2. Measurement Points

MODEL	INPUT		OUTPUT
	V_I	V_M (1)	V_M
74HC595Q	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
74HCT595Q	3V	1.3V	1.3V

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 6ns.

REVISION HISTORY

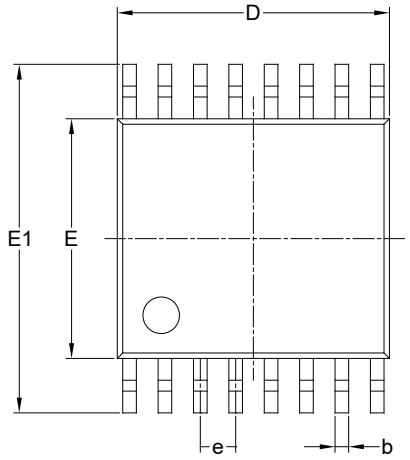
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

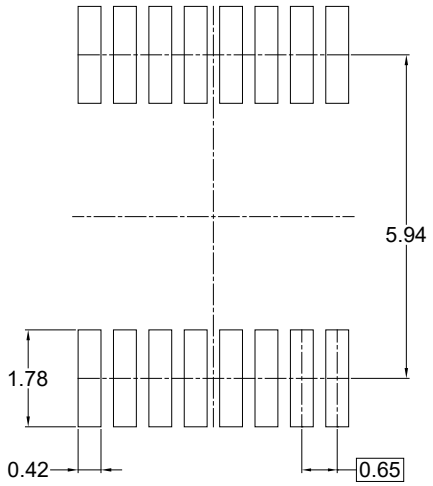
OCTOBER 2025 – REV.A to REV.A.1	**Page**
Updated Timing Diagram section	4

Changes from Original (FEBRUARY 2025) to REV.A	**Page**
Changed from product preview to production data	All

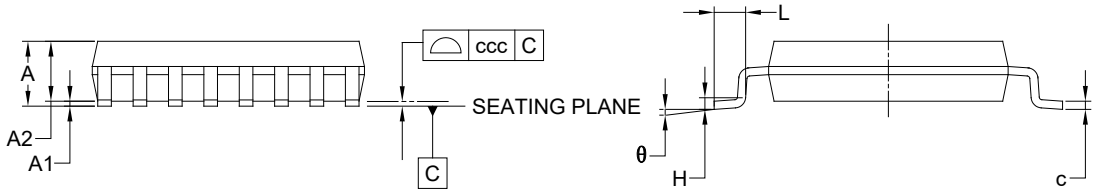
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

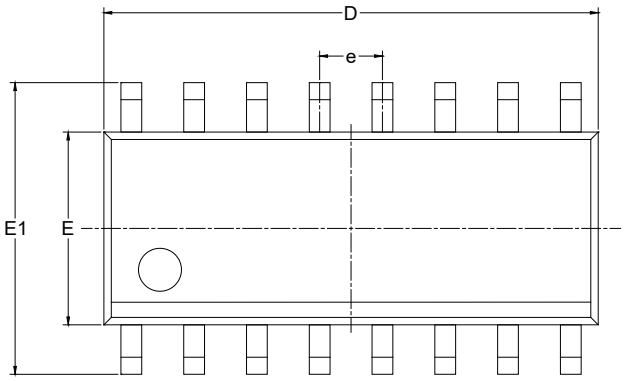


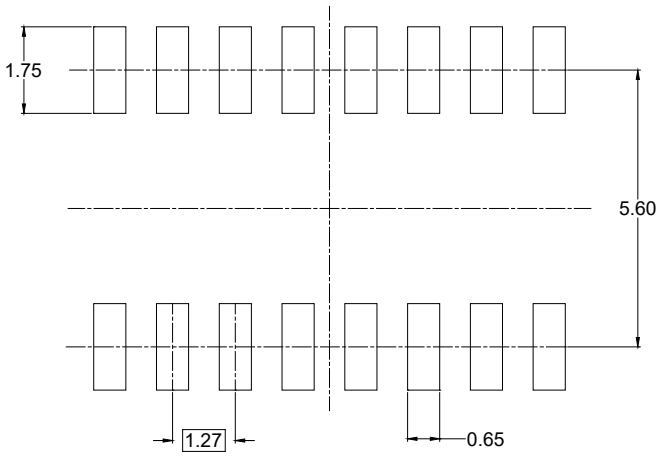
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

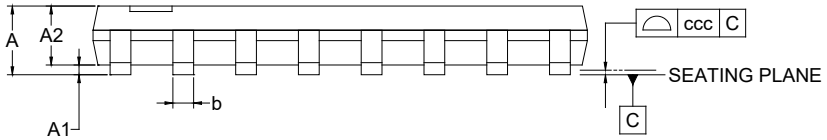
PACKAGE OUTLINE DIMENSIONS

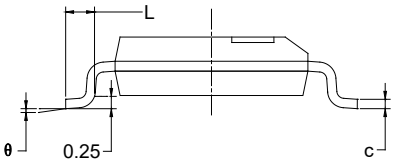
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)



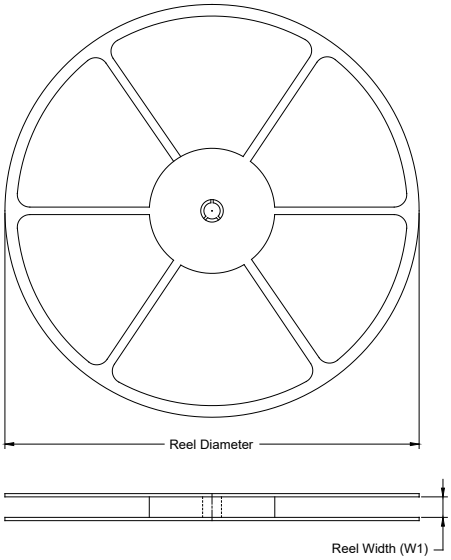


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	1.550
b	0.310	-	0.510
c	0.100	-	0.250
D	9.800	-	10.200
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

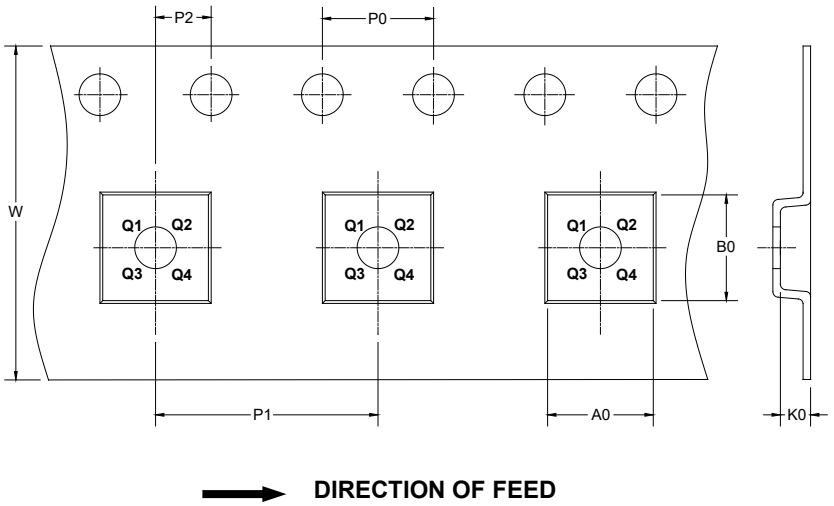
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

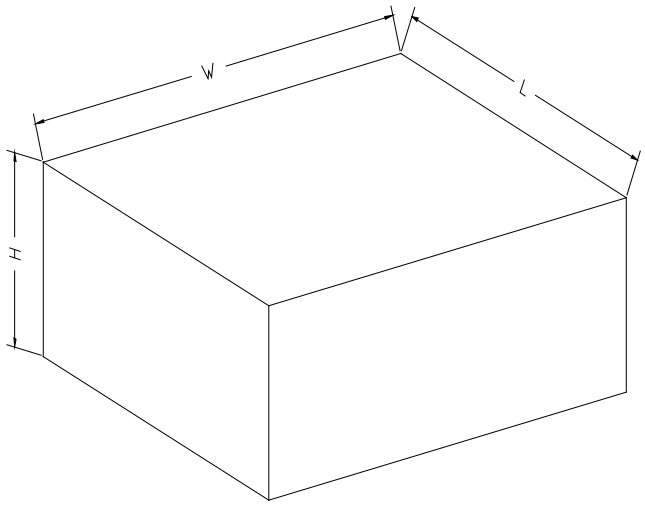
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
SOIC-16	13"	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002