LSF0102-Q1 汽车类 2 通道自动双向多电压电平转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C ≤ T_A ≤ 125°C
  - 器件 HBM ESD 分类等级 2
  - CDM ESD 分类等级 C6
- 在无方向引脚的情况下提供双向电压转换
- 支持开漏和推挽应用，如 I^2C、SPI、UART、MDIO、SDIO 和 GPIO
- 在不超过 30pF 的容性负载条件下支持最高达 100MHz 的上行转换和超过 100MHz 的下行转换，在 50pF 的容性负载条件下支持高达 40MHz 的上行/下行转换
- 可实现以下电压之间的双向电压电平转换
  - 0.95V ↔ 1.8/2.5/3.3/5 V
  - 1.2V ↔ 1.8/2.5/3.3/5V
  - 1.8V ↔ 2.5/3.3/5V
  - 2.5V ↔ 3.3/5V
  - 3.3V ↔ 5V
- 低待机电流
- 5V 耐受 I/O 端口，可支持 TTL 电压电平
- 低导通电阻，可减少信号失真
- EN = 低电平时为高阻抗 I/O 引脚
- 采用直通引脚排列以简化 PCB 布线
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范

2 应用

- 信息娱乐系统音响主机
- 图形群集
- ADAS 融合
- ADAS 前置摄像头
- HEV 电池管理系统

3 说明

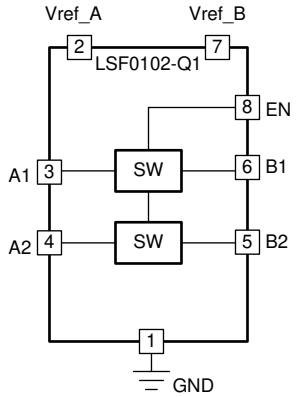
LSF0102-Q1 器件是一款自动双向电压转换器，无需方向引脚即可在广泛的电源范围内进行转换。当容性负载 ≤ 30pF 时，LSF0102-Q1 支持最高 100MHz 的升压转换和高于 100MHz 的降压转换。此外，当容性负载为 50pF 时，LSF0102-Q1 支持最高 40MHz 的上行和下行转换，因此，LSF0102-Q1 器件可支持汽车中各种常见的标准接口，如 I^2C、SPI、GPIO、SDIO、UART 和 MDIO。

LSF0102-Q1 器件具有 5V 耐受数据输入。因此该器件可兼容 TTL 电压电平。此外，LSF0102-Q1 还支持混合模式电压转换，可在各个通道上升压和降压转换至不同的电源电平。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
LSF0102-Q1	DCU（VSSOP，8）	2.30mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (April 2021) to Revision B (May 2023)	Page
• Updated the *Recommended Operating Conditions* table to reflect maximum of 5.5 V	4
• Updated the *Thermal Information* table	4
• Changed all *Switching Characteristic* Test Conditions	6
• Added the *Output Enable* section	9
• Added the *Up and Down Translation* sections	11
• Changed *pull up resistor* to *bias resistor* in *Enable, Disable, and Reference Voltage Guidelines* section	12
• Added the *Bias Circuitry* section	13
• Updated the current values in the table titled *Pull-up Resistor Values*	13
• Added image to the *Mixed-Mode Voltage Translation* section	14
• Added the *Single Supply Translation* section	15
• Added section *Voltage Translation for Vref_B < Vref_A + 0.8 V*	17

Changes from Revision * (May 2018) to Revision A (April 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated the *Bidirectional Translation* section to include inclusive terminology	13

5 Pin Configuration and Functions

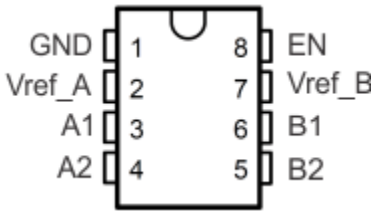


图 5-1. LSF0102-Q1 DCU Package, 8-Pin VSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A1	3	I/O	Input/Output A port for Channel 1
A2	4	I/O	Input/Output A port for Channel 2
B1	6	I/O	Input/Output B port for Channel 1
B2	5	I/O	Input/Output B port for Channel 2
EN	8	I	I/O enable input; see 图 9-1 for typical setup. Should be tied directly to V_{ref_B} to be enabled or pulled LOW to disable all I/O pins.
GND	1	—	Ground
Vref_A	2	—	A side reference supply voltage; see *节 9* for setup and supply voltage range.
Vref_B	7	—	B side reference supply voltage. Must be connected to supply through 200 kΩ; see *节 9* for setup and supply voltage range.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage(2), V_I		–0.5	7	V
Input/output voltage(2), $V_{I/O}$		–0.5	7	V
Continuous channel current			128	mA
Input clamp current, I_{IK}	$V_I < 0$		–50	mA
Storage temperature range, T_{stg}		–65	150	°C
Operating junction temperature, T_J			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage		5.5	V
$V_{ref_A/B/EN}$	Reference voltage		5.5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LSF0102-Q1 DCU (US8) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	279.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	129.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	191.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	66.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	190.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = – 18 mA, V_{EN} = 0				– 1.2	V
I_{IH}	I/O input high leakage	V_I = 5 V, V_{EN} = 0				5.0	µA
I_{CCBA}	V_{ref_B} to V_{ref_A} leakage	V_{ref_B} = V_{EN} = 5.5 V, V_{ref_A} = 4.5 V, I_O = 0, V_I = V_{CC} or GND			1		µA
$C_{I(ref_A/B/EN)}$	Input capacitance	V_I = 3 V or 0			11		pF
$C_{io(off)}$	I/O pin off-state capacitance	V_O = 3 V or 0, V_{EN} = 0			4.0	6.0	pF
$C_{io(on)}$	I/O Pin on-state capacitance	V_O = 3 V or 0, V_{EN} = 3 V			10.5	12.5	pF
r_{on} (2)	On-state resistance	V_I = 0, I_O = 64 mA	V_{ref_A} = 3.3 V; V_{ref_B} = V_{EN} = 5 V		8.0		Ω
			V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 5 V		9.0		
			V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 5 V		10		
		V_I = 0, I_O = 32 mA	V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 5 V		10		Ω
			V_{ref_A} = 2.5 V; V_{ref_B} = V_{EN} = 5 V		15		
		V_I = 1.8 V, I_O = 15 mA	V_{ref_A} = 3.3 V; V_{ref_B} = V_{EN} = 5 V		9.0		Ω
		V_I = 1.0 V, I_O = 10 mA	V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 3.3 V		18		Ω
		V_I = 0 V, I_O = 10 mA	V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 3.3 V		20		Ω
		V_I = 0 V, I_O = 10 mA	V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 1.8 V		30		Ω

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

6.6 Switching Characteristics (Translating Down): V_{CCB} = 3.3 V

over recommended operating free-air temperature range, V_{CCB} = 3.3 V, V_{CCB} = V_{IH} = V_{ref_A} + 1, V_{IL} = 0, and V_M = 0.5V_{ref_A} (unless otherwise noted) (see *Parameter Measurement Information*)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1.1			0.7			0.3		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1.2			0.8			0.4		

6.7 Switching Characteristics (Translating Down): V_{CCB} = 2.5 V

over recommended operating free-air temperature range, V_{CCB} = 2.5 V, V_{CCB} = V_{IH} = V_{ref_A} + 1, V_{IL} = 0, and V_M = 0.5V_{ref_A} (unless otherwise noted) (see *Parameter Measurement Information*)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1.2			0.8			0.35		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1.3			1			0.5		

6.8 Switching Characteristics Translating Up): V_{CCB} = 3.3 V

over recommended operating free-air temperature range, V_{CCB} = 3.3 V, V_{CCB} = V_T = V_{ref_A} + 1, V_{ref_A} = V_{IH}, V_{IL} = 0, V_M = 0.5V_{ref_A} and R_L = 300 (unless otherwise noted) (see *Parameter Measurement Information*)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1			0.8			0.4		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1			0.9			0.4		

6.9 Switching Characteristics (Translating Up): V_{CCB} = 2.5 V

over recommended operating free-air temperature range, V_{CCB} = 2.5 V, V_{CCB} = V_T = V_{ref_A} + 1, V_{ref_A} = V_{IH}, V_{IL} = 0, V_M = 0.5V_{ref_A} and R_L = 300 (unless otherwise noted) (see *Parameter Measurement Information*)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1.1			0.9			0.45		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1.3			1.1			0.6		

6.10 Typical Characteristics

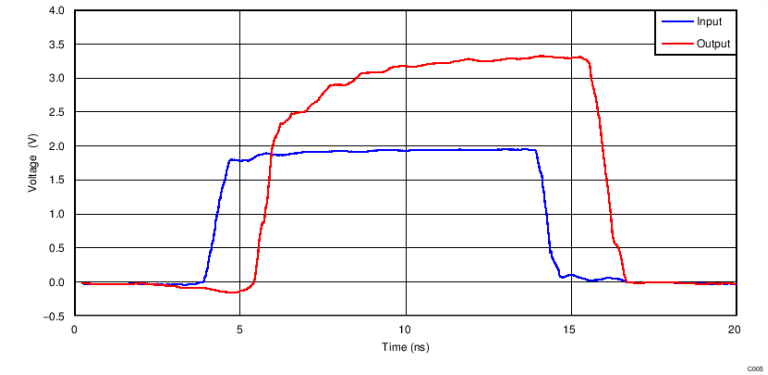
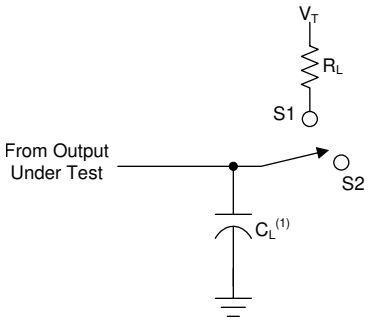


图 6-1. Signal Integrity (1.8 to 3.3 V Translation Up at 50 MHz)

7 Parameter Measurement Information

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

- PRR ⩽ 10 MHz
- Z_O = 50 Ω
- t_r ⩽ 2 ns
- t_f ⩽ 2 ns



A. C_L includes probe and jig capacitance.

图 7-1. Load Circuit

USAGE	SWITCH
Translating Up Translating Down	S1 S2

图 7-2. Translating Up and Down Table

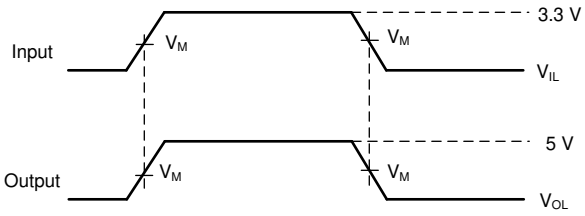


图 7-3. Translating Up

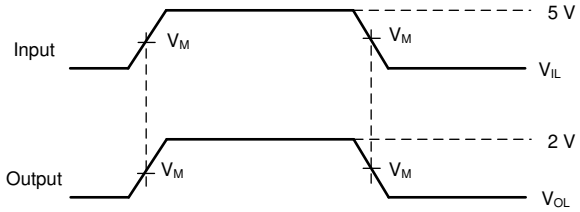


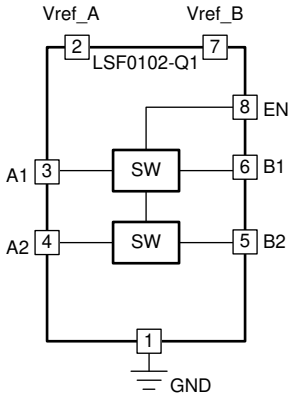
图 7-4. Translating Down

8 Detailed Description

8.1 Overview

The LSF0102-Q1 device can be used in level translation applications for interfacing devices or systems operating at different interface voltages. The LSF0102-Q1 device is ideal for use in applications where an open-drain driver is connected to the data I/Os. With appropriate pull-up resistors and layout, the LSF0102-Q1 device can achieve 100 MHz. The LSF0102-Q1 can also be used in applications where a push-pull driver is connected to the data I/Os.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Auto Bidirectional Voltage Translation

The LSF0102-Q1 device is an auto bidirectional voltage level translator that operates from 0.95 to 5.5 V on V_{ref_A} and 1.8 to 5.5 V on V_{ref_B}. This allows bidirectional voltage translation between 0.95 V and 5.5 V without the need for a direction pin in open-drain or push-pull applications. The LSF0102-Q1 device supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 250-Ω pull-up resistor with a 30-pF capacitive load.

8.3.2 Output Enable

To enable the I/O pins, the EN input should be tied directly to V_{ref_B} during operation and both pins must be pulled up to the HIGH side (V_{CCB}) through a bias resistor (typically 200 kΩ). To ensure the high impedance state during power-up, power-down, or during operation, the EN pin must be LOW. The EN pin should always be tied directly to the V_{ref_B} pin and is recommended to be disabled by an open-drain driver without a pullup resistor. This allows V_{ref_B} to regulate the EN input and bias the channels for proper translation. A filter capacitor on V_{ref_B} is recommended for a stable supply at the device.

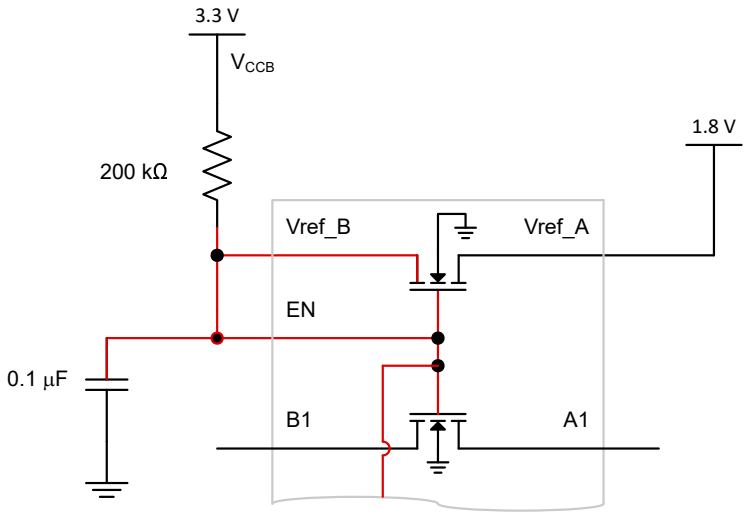


图 8-1. EN Pin Tied to V_{ref_B} Directly and to V_{CCB} Through a Pull-Up Resistor

The supply voltage of open drain I/O devices can be completely different from the supplies used for the LSF and has no impact on the operation. For additional details on how to use the enable pin, see the *Using the Enable Pin with the LSF Family video.*

表 8-1. EN Pin Function Table

INPUT EN(1) PIN	Data Port State
Tied directly to V_{ref_B}	An = Bn
L	Hi-Z

(1) EN is controlled by V_{ref_B} logic levels.

8.3.3 Device Functional Modes

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low R_{ON} of the switch allows connections to be made with minimal propagation delay and signal distortion.

表 8-1 provides a summary of device operation. For additional details on the functional operation of the LSF family of devices, see the *Down Translation with the LSF Family* and *Up Translation with the LSF Family* videos.

表 8-2. Device Functionality

Signal Direction(1)	Input State	Switch State	Functionality
B to A (Down Translation)	B = LOW	ON (Low Impedance)	A-side voltage is pulled low through the switch to the B-side voltage
	B = HIGH	OFF (High Impedance)	A-side voltage is clamped at V_{ref_A} (2)
A to B (Up Translation)	A = LOW	ON (Low Impedance)	B-side voltage is pulled low through the switch to the A-side voltage
	A = HIGH	OFF (High Impedance)	B-side voltage is clamped at V_{ref_A} and then pulled up to the V_{PU} supply voltage

(1) The downstream channel should not be actively driven through a low impedance driver, or else bus contention may occur.
(2) The A-side can have a pullup to V_{ref_A} for additional current drive capability or may also be pulled above V_{ref_A} with a pullup resistor. Specifications in the *Recommended Operating Conditions* section should always be followed.

8.3.3.1 Up and Down Translation

8.3.3.1.1 Up Translation

When the signal is being driven from A to B and the An port is HIGH, the switch will be OFF and the Bn port will then be driven to a voltage higher than V_{ref_A} by the pull-up resistor that is connected to the pull-up supply voltage (V_{PU}). This functionality allows seamless translation between higher and lower voltages selected by the user, without the need for directional control. Pull-up resistors are always required on the high side, and pull-ups are only required on the low side, if the low side of the device's output is open drain or its input has a leakage greater than 1 µA.

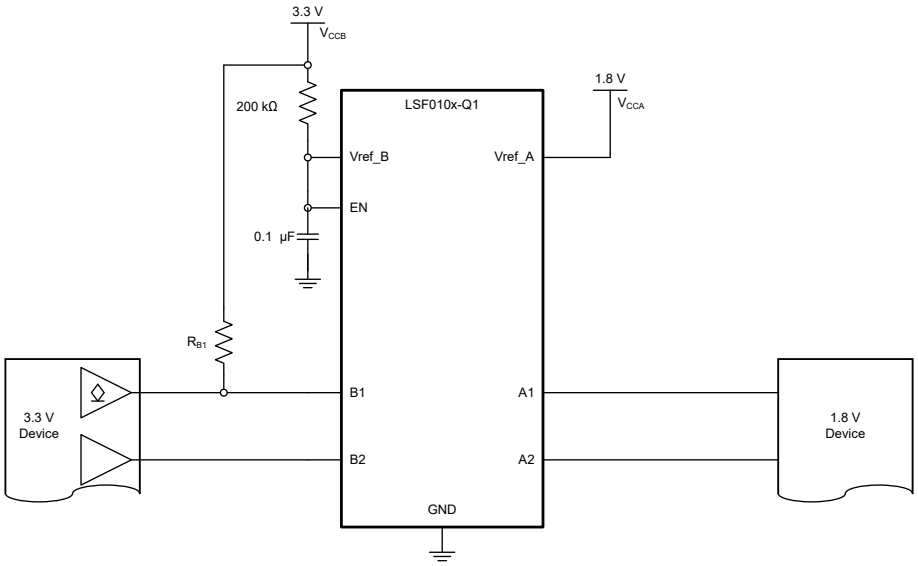


图 8-2. Up Translation Example Schematic with Push-Pull and Open Drain Configuration

Up translation with the LSF requires attention to two important factors: maximum data rate and sink current. Maximum data rate is directly related to the rising edge of the output signal. Sink current depends on supply values and the chosen pull-up resistor values. 方程式 1 shows the maximum data rate formula and 方程式 2 shows the maximum sink current formula, both of which are estimations. A low RC value is needed to reach high speeds, which also require strong drivers. Please see the *Up Translation with the LSF Family* video for estimated data rate and sink current calculations based on circuit components.

$$\frac{1}{3 \times 2R_{B1}C_{B1}} = \frac{1}{6R_{B1}C_{B1}}\left(\frac{bits}{second}\right) \quad (1)$$

$$I_{OL} \cong \frac{V_{CCA}}{R_{A1}} + \frac{V_{CCB}}{R_{B1}}\left(A\right) \quad (2)$$

8.3.3.1.2 Down Translation

When the signal is being driven HIGH from the Bn port to An port, the switch will be OFF, clamping the voltage on the An port to the voltage set by V_{ref_A}. A pull-up resistor can be added on either side of the device. There are special circumstances that allow the removal of one or both of the pull-up resistors. If the signal is always going to be down translated from a push-pull transmitter, then the resistor on the B-side can be removed. If the leakage current into the receiver on the A-side is less than 1 µA, then the resistor on the A-side can also be removed. This arrangement with no external pull-up resistors can be used when down translating from a push-pull output to a low-leakage input. For an open drain transmitter, the pull-up resistor on the B-side is necessary because an open drain output can't drive high by itself. For a summary of device operation, refer to 节 8.3.3. For additional details on the functional operation of the LSF family of devices, see the *Up Translation with the LSF Family* and *Down Translation with the LSF Family* videos.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The LSF0102-Q1 device is able to perform voltage translation for open-drain or push-pull interfaces such as I^2C, SPI, UART, MDIO, SDIO, and GPIO.

9.2 Typical Application

9.2.1 Bidirectional Translation

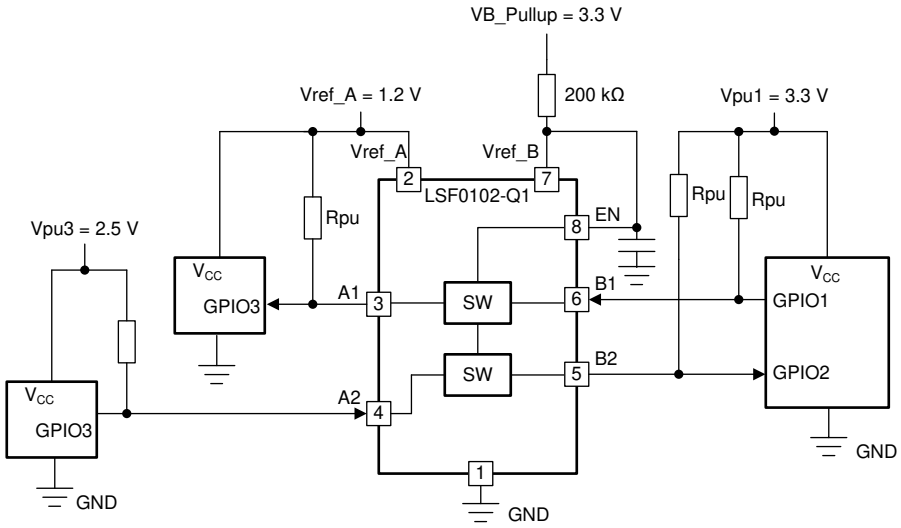


图 9-1. Bidirectional Translation to Multiple Voltage Levels

9.2.1.1 Design Requirements

9.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

The LSF0102-Q1 device has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. Since LSF family is switch-type voltage translator, the power consumption is very low. It is recommended to always enable LSF0102-Q1 device for bidirectional applications by connecting the EN pin to the V_{ref_B} pin, as shown in 图 9-1. For additional details on setting up the V_{ref_A}, V_{ref_B}, and EN pins, see the *Understanding the Bias Circuit for the LSF Family* video.

表 9-1. Application Operating Condition

PARAMETER		MIN	TYP	MAX	UNIT
V_{ref_A} (1)	reference voltage (A)	0.95		5.5	V
V_{ref_B}	reference voltage (B)	V_{ref_A} + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	V_{ref_A} + 0.8	V_{ref_B}	5.5	V
V_{PU}	pull-up supply voltage	0		V_{ref_B}	V

(1) V_{ref_A} is required to be the lowest voltage level across all inputs and outputs.

The 200 kΩ, bias resistor is required to allow V_{ref_B} to regulate the EN input. A filter capacitor on V_{ref_B} is recommended. Also V_{ref_B} and $V_{I(EN)}$ are recommended to be 1.0 V higher than V_{ref_A} for best signal integrity.

9.2.1.1.2 Bias Circuitry

For proper operation, V_{CCA} must always be at least 0.8 V less than V_{CCB} (V_{CCA} + 0.8 ≦ V_{CCB}). The 200 kΩ bias resistor is required to allow V_{ref_B} to regulate the EN input and properly bias the device for translation. A 0.1 µF capacitor is recommended for providing a path from V_{ref_B} to ground for high frequency noise. V_{ref_B} and $V_{I(EN)}$ are recommended to be 1.0 V higher than V_{ref_A} for best signal integrity.

Attempting to drive the EN pin directly with a push-pull output device is a very common design error with the LSF0102-Q1 series of devices. It is also very important to note that current does flow into the A-side voltage supply during normal operation. Not all voltage sources can sink current, so be sure that applicable designs can handle this current. For more design details, see the *Understanding the Bias Circuit for the LSF Family* video.

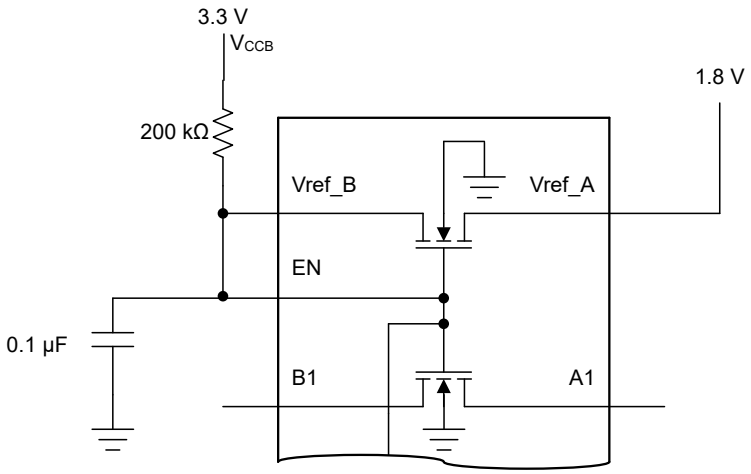


图 9-2. Bias Circuitry Inside the LSF010x-Q1 Device

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{ref_B} and both pins pulled to HIGH side V_{CCB} through a bias resistor (typically 200 kΩ), as shown in 图 9-1. This allows V_{ref_B} to regulate the EN input. A filter capacitor on V_{ref_B} is recommended. The controller output driver can be push-pull or open-drain (pull-up resistors may be required) and the peripheral device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to Vpu).

If either output is push-pull, data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contention in either direction. If both outputs are open-drain, no direction control is needed.

In 图 9-1, the reference supply voltage V_{ref_A} is connected to the processor core power supply voltage. V_{ref_B} is connected through a 200 kΩ resistor to a 3.3 V V_{B_Pullup} power supply and V_{ref_A} is set to 1.2 V. The output of A1 has a maximum output voltage equal to Vref_A, and the bidirectional interface on channel 2 has a maximum output voltage equal to V_{PU1}.

9.2.1.2.2 Pull-Up Resistor Sizing

To maintain an appropriate output low voltage, the pull-up resistor value should limit the current through the pass transistor when it is in the ON state to less than 15 mA. This ensures a pass voltage of 260 mV to 350 mV. To set the current through each pass transistor at 15 mA, the pull-up resistor value can be calculated using the following equation:

$$R_{pu} = \frac{\left(V_{pu} - 0.35\,V\right)}{0.015\,A} \quad (3)$$

The appropriate pull up resistor will depend on the current requirements of the application. 表 9-2 provides resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF0102-Q1 device at 0.175 V, although the 15 mA applies only to current flowing through the LSF0102-Q1.

表 9-2. Pull-up Resistor Values

V_{PU}	8 mA		5 mA		3 mA	
	NOMINAL (Ω)	+10%(1) (Ω)	NOMINAL (Ω)	+10%(1) (Ω)	NOMINAL (Ω)	+10%(1) (Ω)
5 V	581	639	930	1023	1550	1705
3.3 V	369	406	590	649	983	1082
2.5 V	269	296	430	473	717	788
1.8 V	181	199	290	319	483	532
1.5 V	144	158	230	253	383	422
1.2 V	106	117	170	187	283	312

(1) +10% to compensate for V_{DD} range and resistor tolerance

9.2.1.2.3 Application Curve

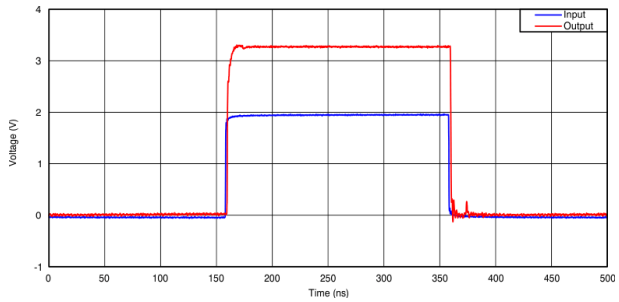


图 9-3. Captured Waveform From Above I^2C Set-Up (1.8 V to 3.3 V at 2.5 MHz)

9.2.1.2.4 Mixed-Mode Voltage Translation

The supply voltage (V_{PU}) for each channel can be individually set with a pull-up resistor. 图 9-4 shows an example of this mixed-mode multi-voltage translation. For additional details on multi-voltage translation, see the *Multi-voltage Translation with the LSF Family* video.

With the V_{ref_B} pulled up to 5 V and V_{ref_A} connected to 1.8 V, all channels will be clamped to 1.8 V at which point a pullup can be used to define the high level voltage for a given channel.

- **Push-Pull Down Translation (5 V to 1.8 V):** Channel 1 is an example of this setup. When B1 is 5 V, A1 is clamped to 1.8 V, and when B1 is LOW, A1 is driven LOW through the switch.
- **Push-Pull Up Translation (1.8 V to 5 V)**: Channel 2 is an example of this setup. When A2 is 1.8 V, the switch is high impedance and the B2 channel is pulled up to 5 V. When A2 is LOW, B2 is driven LOW through the switch.
- **Push-Pull Down Translation (3.3 V to 1.8 V):** Channels 3 and 4 are examples of this setup. When either B3 or B4 are driven to 3.3 V, A3 or A4 are clamped to 1.8 V, and when either B3 or B4 are LOW, A3 or A4 are driven LOW through the switch.
- **Open-Drain Bidirectional Translation (3.3 V ↔ 1.8 V):** Channels 5 through 8 are examples of this setup. These channels are for bidirectional operation for I^2C and MDIO to translate between 1.8 V and 3.3 V with open-drain drivers.

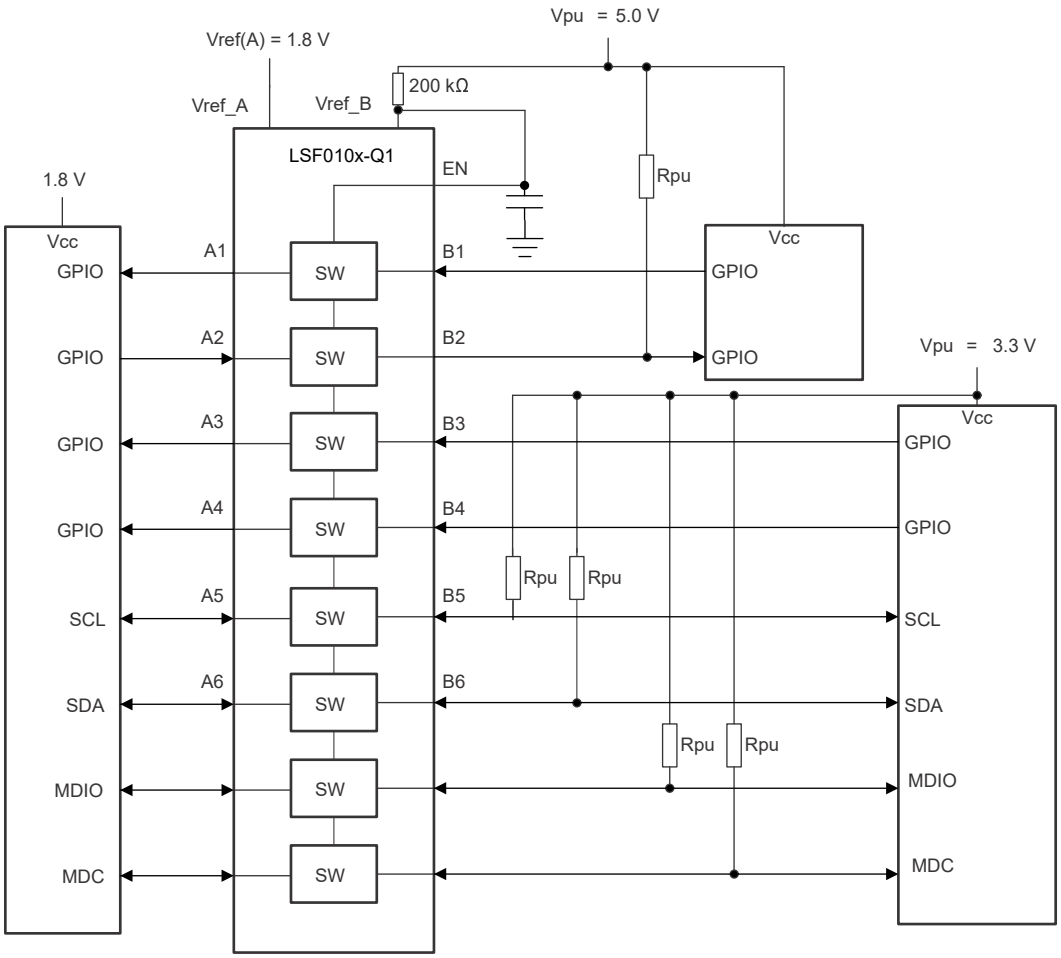


图 9-4. Multi-Voltage Translation with the LSF010x-Q1

9.2.1.2.5 Single Supply Translation

Sometimes, an external device will have an unknown voltage that could be above or below the desired translation voltage, preventing a normal connection of the LSF. Resistors are added on the A side in place of the second supply in this case – this is an example of when LSF single supply operation is utilized, shown in Figure 9-5. In the following figure, a single 3.3 V supply is used to translate between a 3.3 V device and a device that can change between 1.8 V and 5.0 V. R1 and R2 are added in place of the second supply. Note that due to some current coming out of the V_{ref_A} pin, this cannot be treated as a simple voltage divider.

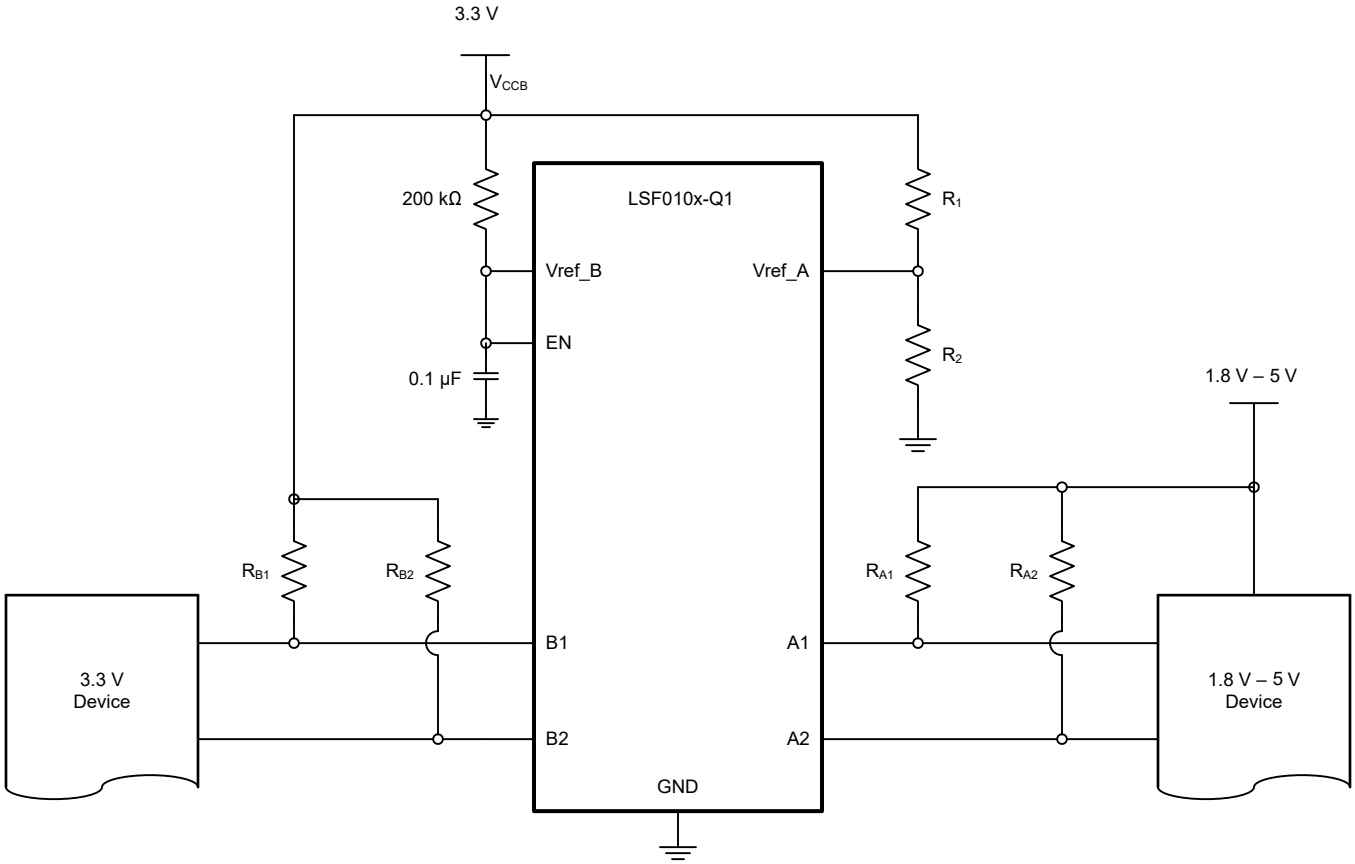


图 9-5. Single Supply Translation with 3.3 V Supply

The steps to select the resistor values for R1 and R2 are as follows:

1. Select a value for R1. Typically, 1 MΩ is used to reduce current consumption.
2. Plug in values for your system into the following equation. Note that V_{ref_A} is the lowest voltage in the system. V_{CCB} is the primary supply and R1 is the selected value from step 1.

$$R_2 = \frac{200\left(10^3\right) \times R_1 \times V_{REFA}}{\left(200\left(10^3\right) + R_1\right)\left(V_{CCB} - V_{REFA}\right) - 0.85 \times R_1} \quad (4)$$

The single supply used must be at least 0.8 V larger than the lowest desired translation voltage. The voltage at V_{ref_A} must be selected as the lowest voltage to be used in the system. The LSF evaluation module (LSF-EVM) contains unpopulated pads to place R1 and R2 for single supply operation testing. For an example single supply translation schematic and details, see the *Single Supply Translation with the LSF Family* video.

9.2.1.2.6 Voltage Translation for $V_{ref_B} < V_{ref_A}$ + 0.8 V

As described in the *Enable, Disable, and Reference Voltage Guidelines* section, it is generally recommended that $V_{ref_B} > V_{ref_A}$ + 0.8 V; however, the device can still operate in the condition where $V_{ref_B} < V_{ref_A}$ + 0.8 V as long as additional considerations are made for the design.

Typical Operation ($V_{ref_B} > V_{ref_A}$ + 0.8 V): in this scenario, pullup resistors are not required on the A-side for proper down-translation as is shown for channels 1 and 2 of 图 9-4. The typical operating mode of the device ensures that when down translating from B to A, the A-side I/O ports will clamp at V_{ref_A} to provide proper voltage translation. For further explanation of device operation, see the *Down Translation with the LSF Family* video.

Requirements for $V_{ref_B} < V_{ref_A}$ + 0.8 V Operation: in this scenario, there is not a large enough voltage difference between V_{ref_A} and V_{ref_B} to ensure that the A side I/O ports will be clamped at V_{ref_A}, but rather at a voltage approximately equal to V_{ref_B} – 0.8 V. For example, if V_{ref_B} = 1.8 V and V_{ref_A} = 1.2 V, the A-side I/Os will clamp to a voltage around 1.0 V. Therefore, to operate in such a condition, the following additional design considerations must be met:

- V_{ref_B} must be greater than V_{Ref_A} during operation ($V_{ref_B} > V_{ref_A}$)
- Pullup resistors should be populated on A-side I/O ports to ensure the line will be fully pulled up to the desired voltage.

图 9-6 shows an example of this setup, where 1.2 V ↔ 1.8 V translation is achieved with the LSF0102-Q1. This type of setup also applies for other voltage nodes such as 1.8 V ↔ 2.5 V, 1.05 V ↔ 1.5 V, and others as long as the *Recommended Operating Conditions* table is followed.

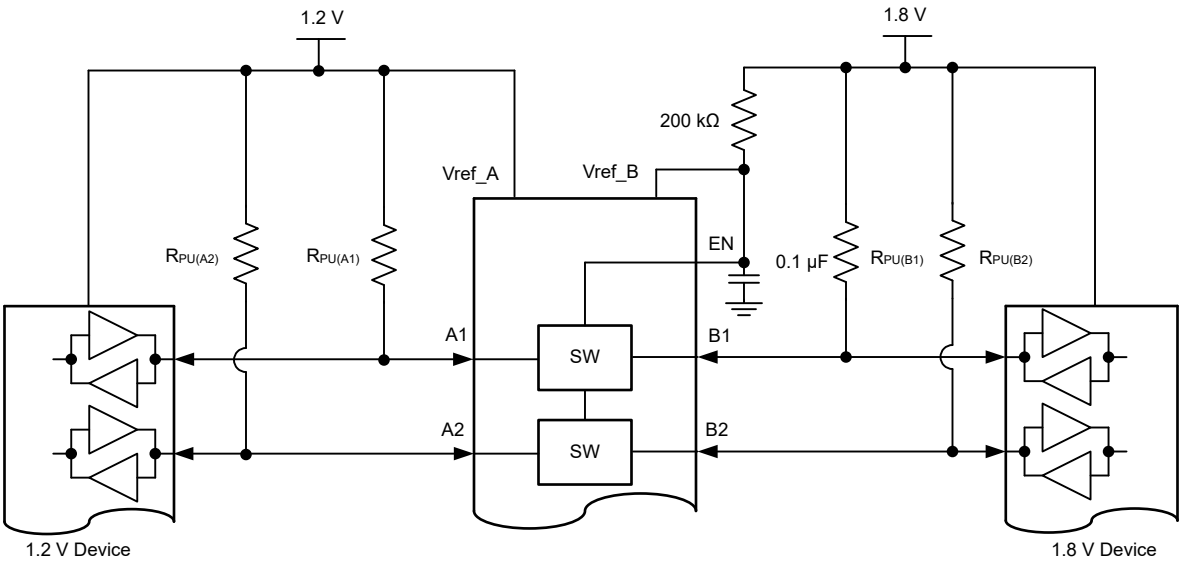


图 9-6. 1.2 V to 1.8 V Level Translation with LSF010x

9.3 Power Supply Recommendations

There are no power sequence requirements for the LSF family. 表 9-3 provides the recommended operating voltages for all supply and input pins.

表 9-3. Recommended Operating Voltages

PARAMETER		MIN	TYP	MAX	UNIT
V_{ref_A} (1)	reference voltage (A)	0.95		5.5	V
V_{ref_B}	reference voltage (B)	V_{ref_A} + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	V_{ref_A} + 0.8		5.5	V

表 9-3. Recommended Operating Voltages (continued)

PARAMETER		MIN	TYP	MAX	UNIT
V_{PU}	pull-up supply voltage	0		V_{ref_B}	V

9.4 Layout

9.4.1 Layout Guidelines

Because the LSF0102-Q1 device is a switch-type level translator, the signal integrity is dependent upon the pull-up resistor value and PCB board parasitics. Consider the following recommendations when designing with the LSF0102-Q1.

- Minimize the signal trace length to reduce capacitance
- Avoid using stubs in the signal path to reduce parasitics.
- Place the LSF0102-Q1 device near the high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of transmitter.

9.4.2 Layout Example

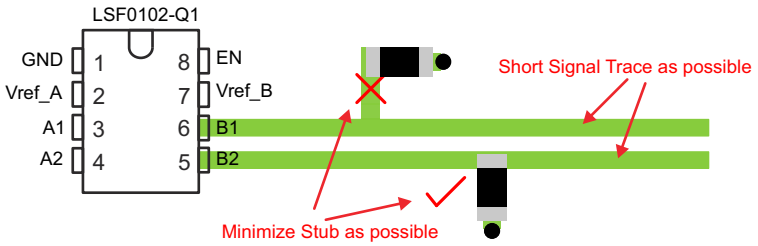


图 9-7. Short Trace Layout

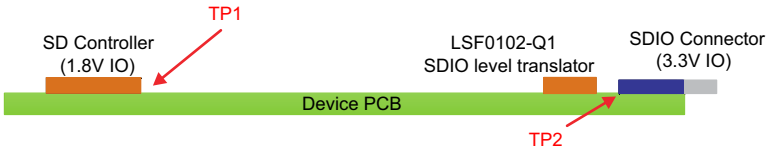


图 9-8. Device Placement

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, TI Logic Minute: *Introduction – Voltage Level Translation with the LSF Family* video
- Texas Instruments, *Voltage-Level Translation with the LSF Family* application report

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LSF0102QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	NG2SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LSF0102-Q1 :

- Catalog : LSF0102

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

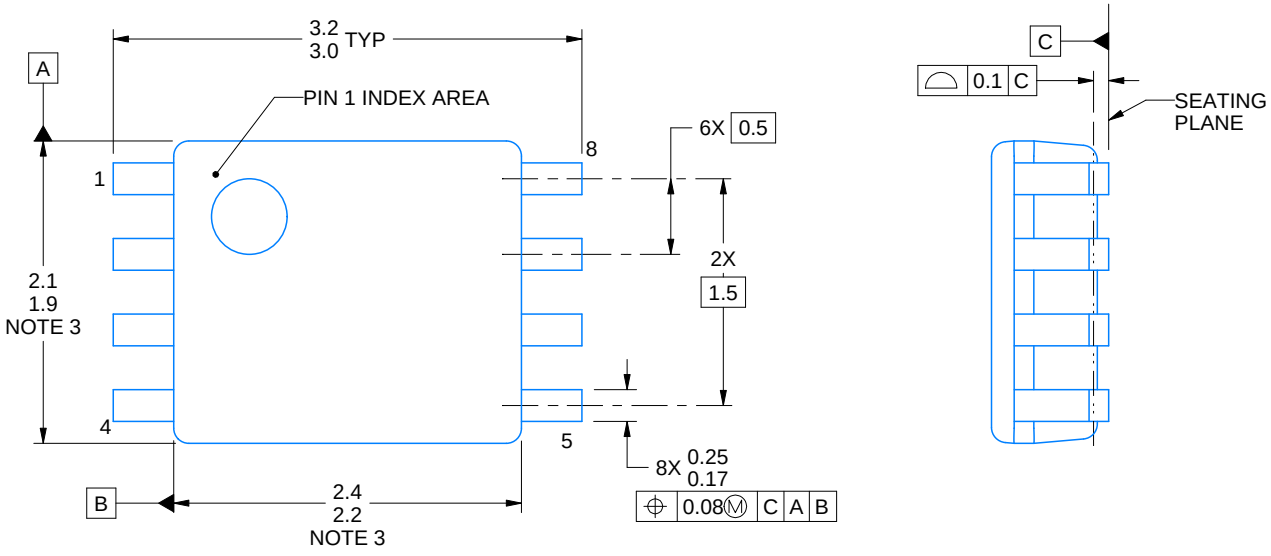
DCU0008A

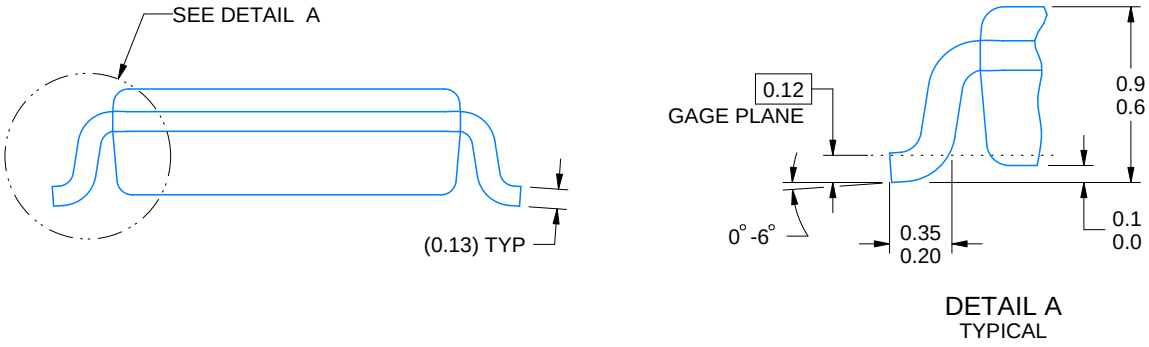


PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE





DETAIL A
TYPICAL

4225266/A 09/2014

NOTES:

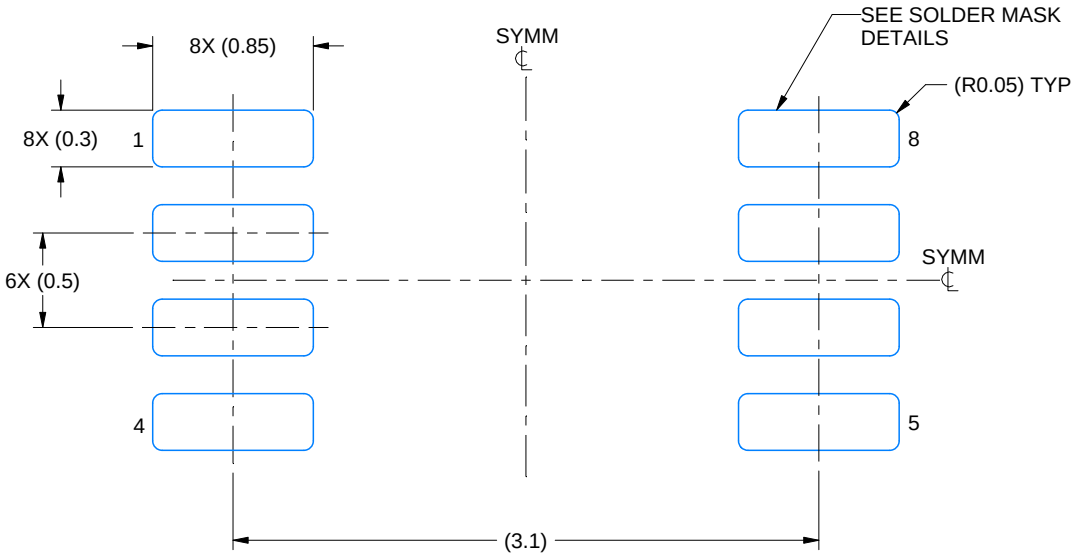
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

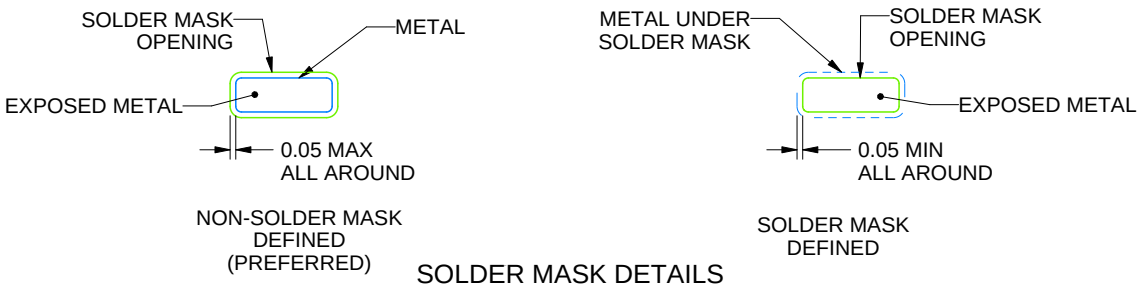
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

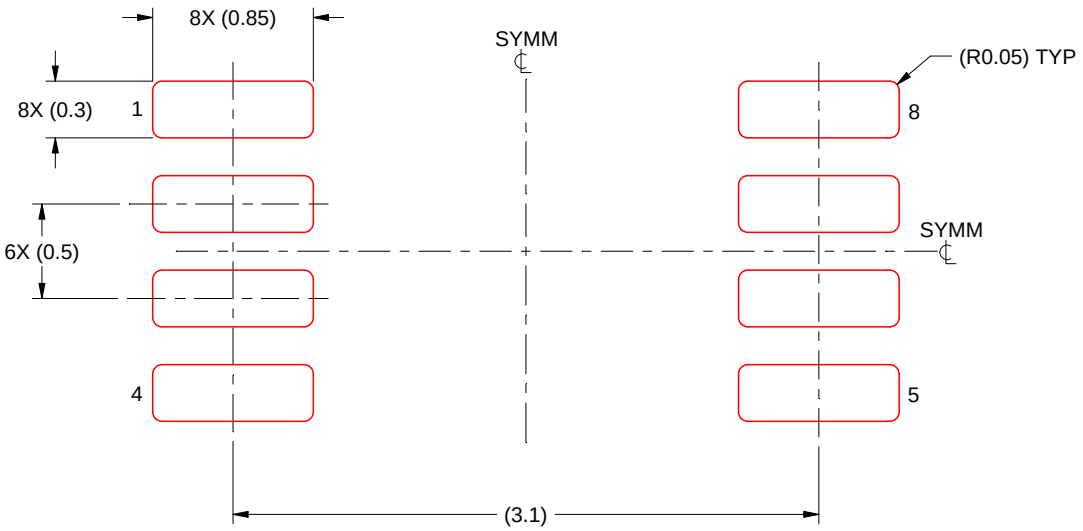
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.