SGM48536BQ
Automotive Single High-Speed, Low-Side Gate Driver with Negative Input Voltage Capability

GENERAL DESCRIPTION

The SGM48536BQ is a single high-speed low-side gate driver for MOSFET and IGBT power switches. The device can provide rail-to-rail driving capability and very small propagation delays (18.5ns, TYP). It also provides 4A peak source current and 8A peak sink current (asymmetrical drive) when V_{DD} = 12V. The input can withstand a maximum negative voltage of -10V.

The operating voltage range is 9V to 25V. The device features under-voltage lockout (UVLO) function. After UVLO is triggered, the output remains low.

The SGM48536BQ adopts separate output architecture. The separate output structure with asymmetric drive improves the immunity of the device to the parasitic Miller conduction effect and reduces ground bounce.

The input threshold of the device is compatible with low voltage TTL and CMOS logic, which will not be affected by V_{DD} changes. A Schmitt trigger is used at the input, and a wide range of hysteresis voltage is designed to enhance the immunity.

The SGM48536BQ is available in a Green SOT-23-6 package.

This device is AEC-Q100 qualified (Automotive Electronics Council Standard Q100 Grade 1) and the use of this device is suitable for automotive applications.

APPLICATIONS

Power MOSFETs
IGBT Driving for Power Supplies
DC/DC Converters
Solar Power, Motor Drivers

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Asymmetrical Drive**
  - **4A Peak Source Current**
  - **8A Peak Sink Current**
- **TTL and CMOS Compatible Logic Threshold**
- **Logic Levels Independent of Supply Voltage**
- **Hysteretic Input Logic for High Noise Immunity**
- **Outputs are Logic Low when Input is Floating**
- **Negative Voltage Handling Capability:**
  - **-10V DC at Input**
  - **-2V, 200ns Pulse for Outputs**
- **Glitch-Free Operation at Power-Up and Power-Down: Outputs are Pulled Low during Supply UVLO**
- **Fast Propagation Delay: 18.5ns (TYP)**
- **Fast Rise Time: 9.5ns (TYP)**
- **Fast Fall Time: 8ns (TYP)**
- **Separate Output Options Allow for Tuning of Turn-on and Turn-off Currents**
- **Input Pin Absolute Maximum Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage**
- **Available in a Green SOT-23-6 Package**

TYPICAL APPLICATION

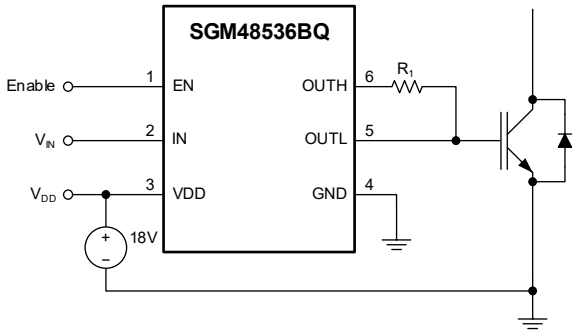


Figure 1. SGM48536BQ Driving IGBT

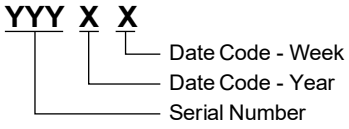
代理商 威尔芯 www.visvie.com 联系电话 138 2526 5270

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48536BQ	SOT-23-6	-40℃ to +125℃	SGM48536BQN6G/TR	0FBXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{DD} ..... -0.3V to 28V
EN, IN Voltage Range ..... -10V to 28V
OUTH, OUTL Voltage Range
DC ..... -0.3V to V_{DD} + 0.3V
Repetitive Pulse < 200ns (1) ..... -2V to V_{DD} + 0.3V
Maximum Output Pulsed Source/Sink Current (0.5μs), I_{OUT_PULSED} 4A/8A
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 147.4℃/W
SOT-23-6, θ_{JB} ..... 39.8℃/W
SOT-23-6, θ_{JC} ..... 60.8℃/W
Maximum Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 3000V
CDM 1000V

NOTE:
1. Verified by characterization on bench.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{DD} ..... 9V to 25V
EN, IN Voltage Range ..... -10V to 25V
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

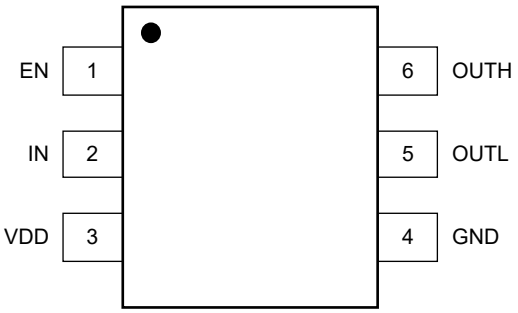
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM48536BQ (TOP VIEW)



SOT-23-6

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	EN	I	Enable Input. Pull EN high or leave it floating to enable output. Pull EN low to disable output, ignoring input state.
2	IN	I	Non-Inverting Input. OUT is logic low if IN is unbiased or left floating.
3	VDD	I	Power Supply Input.
4	GND	—	Ground. Reference pin for all signals.
5	OUTL	O	Driver Sink Current Output.
6	OUTH	O	Driver Source Current Output.

NOTE: I: input, O: output.

FUNCTION TABLE

IN	EN	OUTH	OUTL	OUT (OUTH and OUTL Pins Tied Together)
L	L	High-Impedance	L	L
L	H	High-Impedance	L	L
H	L	High-Impedance	L	L
H	H	H	High-Impedance	H
H	Floating	H	High-Impedance	H
Floating	H	High-Impedance	L	L

ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V, C_{IN} = 1μF, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, OUTH and OUTL are tied together for SGM48536BQ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supplies						
VDD Supply Voltage	V_{DD}		9		25	V
VDD Start-Up Current	I_{DD_OFF}	V_{DD} = 6V, V_{IN} = V_{EN} = 0V	45	83	135	μA
		V_{DD} = 6V, V_{IN} = V_{EN} = V_{DD}	20	48	85	
Supply Start Threshold	V_{ON}		7.4	8	8.6	V
Minimum Operating Voltage after Supply Start	V_{OFF}		6.5	7	7.5	V
Supply Voltage Hysteresis	V_{DD_HYS}			1		V
Input and Enable (IN, EN)						
Non-Inverting Input Signal High Threshold	V_{IN_H}			2.05	2.4	V
Non-Inverting Input Signal Low Threshold	V_{IN_L}		1	1.23		V
Non-Inverting Input Hysteresis	V_{IN_HYS}			0.82		V
Enable Signal High Threshold	V_{EN_H}			2	2.4	V
Enable Signal Low Threshold	V_{EN_L}		1	1.2		V
Enable Signal Hysteresis	V_{EN_HYS}			0.8		V
Outputs (OUTH, OUTL)						
High Level Output Voltage	V_{OH}	V_{DD} = 12V, V_{OH} = V_{DD} - V_{OUT}, I_{OUT} = -10mA		53	130	mV
		V_{DD} = 9V, V_{OH} = V_{DD} - V_{OUT}, I_{OUT} = -10mA		53	130	
Low Level Output Voltage	V_{OL}	V_{DD} = 12V, I_{OUT} = 10mA		4.3	10	mV
		V_{DD} = 9V, I_{OUT} = 10mA		4.3	10	
Output Pull-Up Resistance (1)	R_{OH}	V_{DD} = 12V, I_{OUT} = -50mA		5.3	11	Ω
		V_{DD} = 9V, I_{OUT} = -50mA		5.3	11	
Output Pull-Down Resistance	R_{OL}	V_{DD} = 12V, I_{OUT} = 50mA		0.43	0.72	Ω
		V_{DD} = 9V, I_{OUT} = 50mA		0.43	0.72	
Peak Output Current (2)	I_{PK_SOURCE}	C_L = 0.22μF, f_{SW} = 1kHz		4		A
	I_{PK_SINK}			8		A
Protection Circuits						
Thermal Shutdown Temperature	T_{TSD}			170		℃
Thermal Shutdown Temperature Hysteresis	T_{HYS}			15		℃

NOTES:
1. R_{OH} represents constant pull-up resistance only.
2. Verified by characterization on bench.

SWITCHING CHARACTERISTICS

(V_{DD} = 12V, C_{IN} = 1μF, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, OUTH and OUTL are tied together for SGM48536BQ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN (2)	TYP	MAX (2)	UNITS
Rise Time (1)	t_R	V_{DD} = 12V, C_L = 1.8nF		9.5	13	ns
		V_{DD} = 9V, C_L = 1.8nF		10	13	
Fall Time (1)	t_F	V_{DD} = 12V, C_L = 1.8nF		8	12	ns
		V_{DD} = 9V, C_L = 1.8nF		7	12	
Minimum Input Pulse Width	t_{PW}			16		ns
IN to Output Propagation Delay (1)	t_{D1}	V_{DD} = 12V, 5V IN pulse, C_L = 1.8nF	6	12.5	22	ns
		V_{DD} = 9V, 5V IN pulse, C_L = 1.8nF	6	12.5	22	
	t_{D2}	V_{DD} = 12V, 5V IN pulse, C_L = 1.8nF	10	18.5	30	ns
		V_{DD} = 9V, 5V IN pulse, C_L = 1.8nF	10	19	30	
EN to Output Propagation Delay (1)	t_{D3}	V_{DD} = 12V, 5V enable pulse, C_L = 1.8nF	6	13	22	ns
		V_{DD} = 9V, 5V enable pulse, C_L = 1.8nF	6	13	22	
	t_{D4}	V_{DD} = 12V, 5V enable pulse, C_L = 1.8nF	10	20	30	ns
		V_{DD} = 9V, 5V enable pulse, C_L = 1.8nF	10	21	30	

NOTES:
1. See timing diagrams from Figure 2 to Figure 3.
2. Specified by design and characterization, not production tested.

TIMING DIAGRAMS

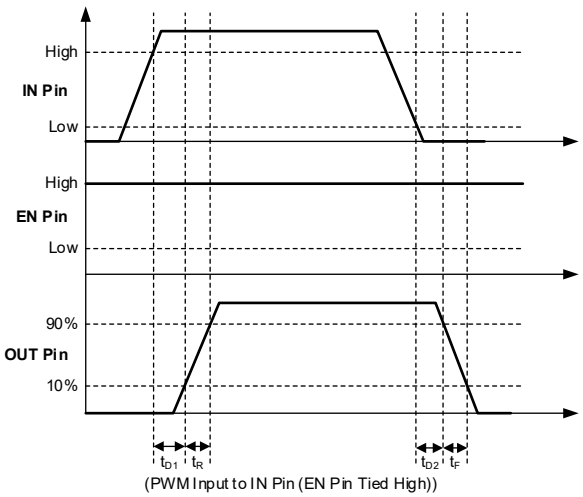


Figure 2. Non-Inverting Configuration

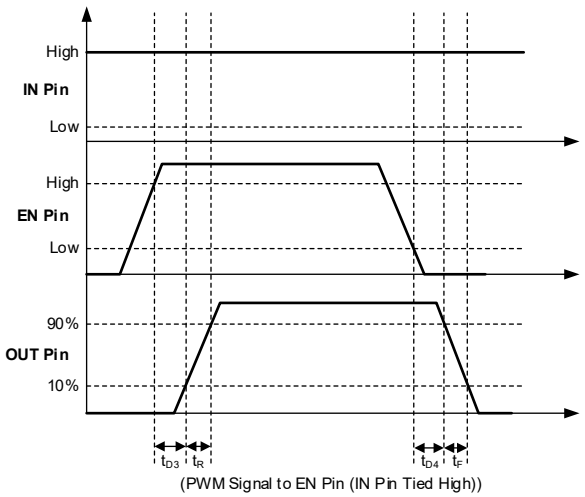
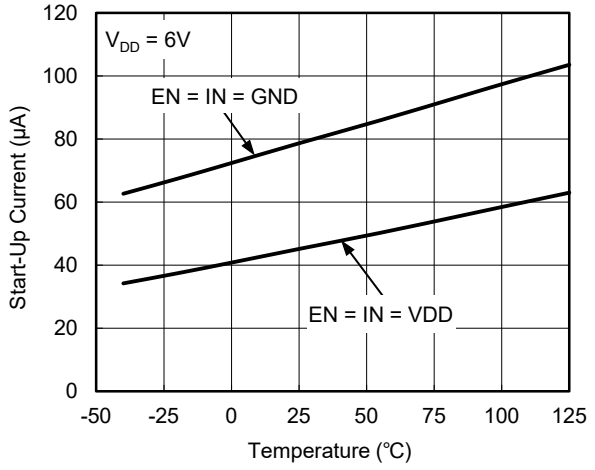


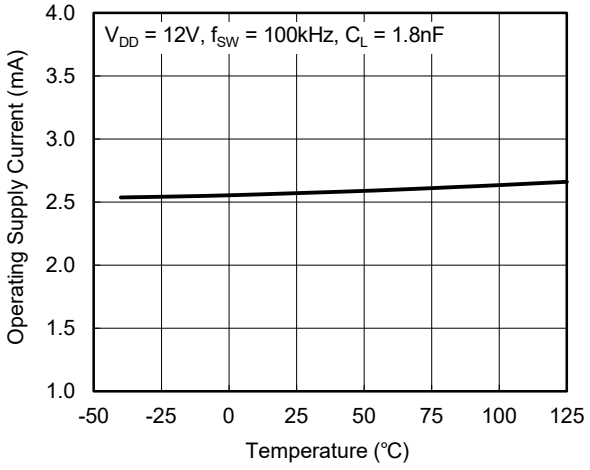
Figure 3. Enable Function

TYPICAL PERFORMANCE CHARACTERISTICS

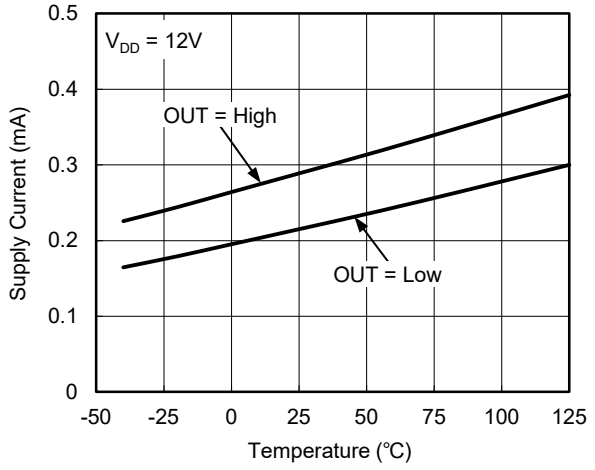
Start-Up Current vs. Temperature



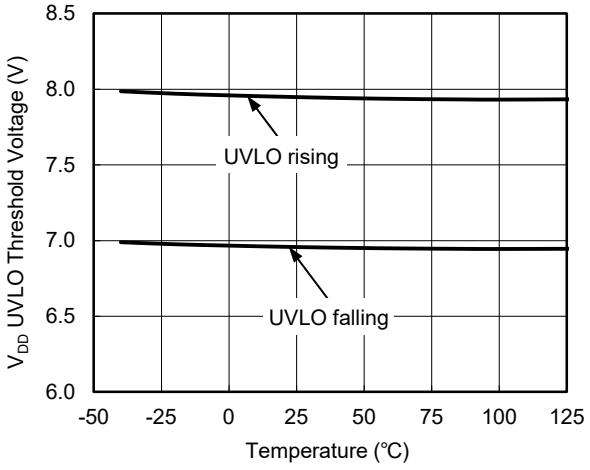
Operating Supply Current vs. Temperature (Output Switching)



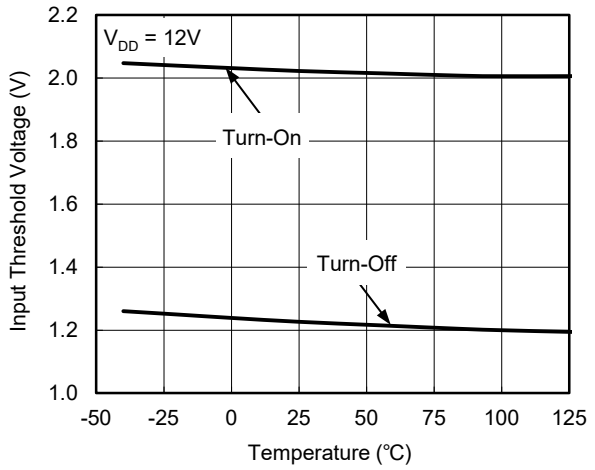
Supply Current vs. Temperature (Output in DC High/Low)



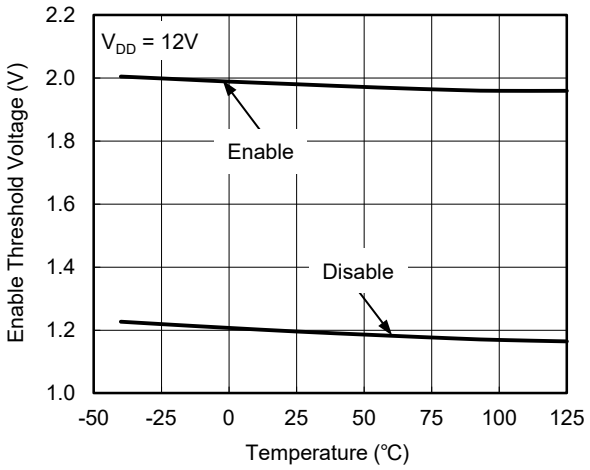
UVLO Threshold Voltage vs. Temperature



Input Threshold Voltage vs. Temperature

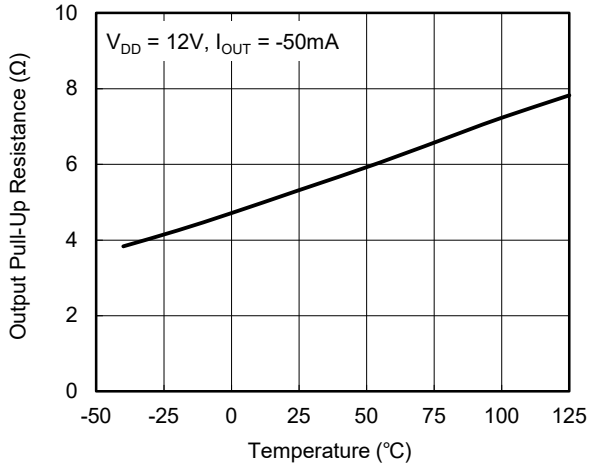


Enable Threshold Voltage vs. Temperature

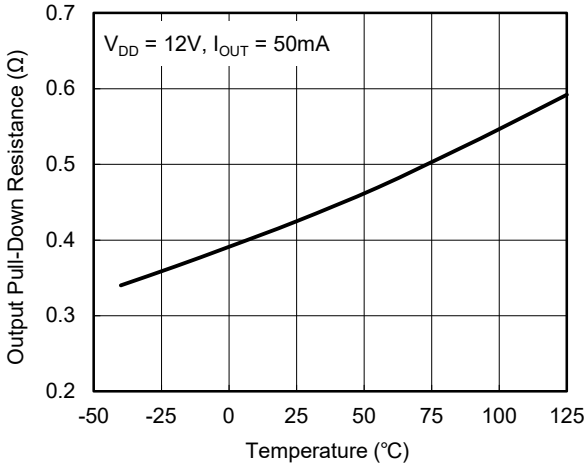


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

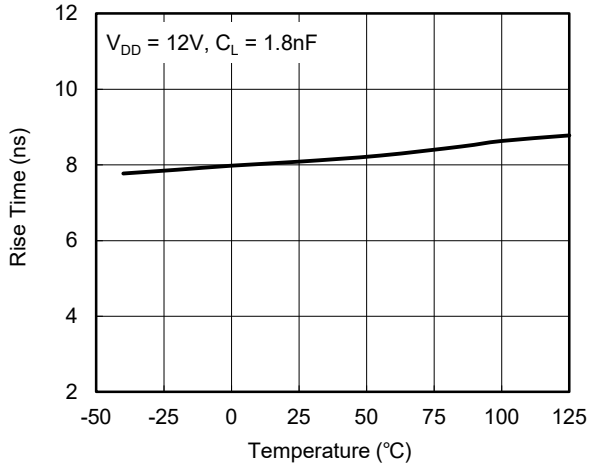
Output Pull-Up Resistance vs. Temperature



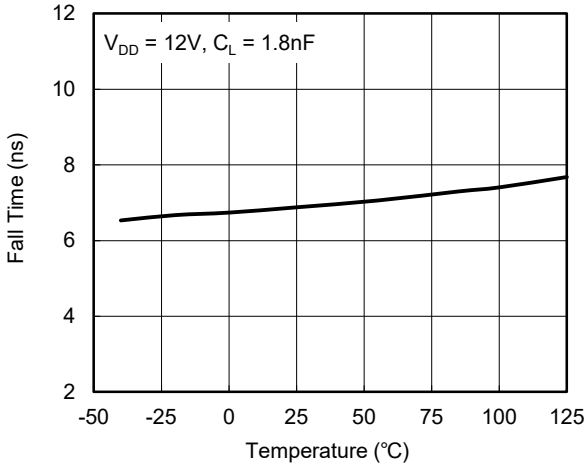
Output Pull-Down Resistance vs. Temperature



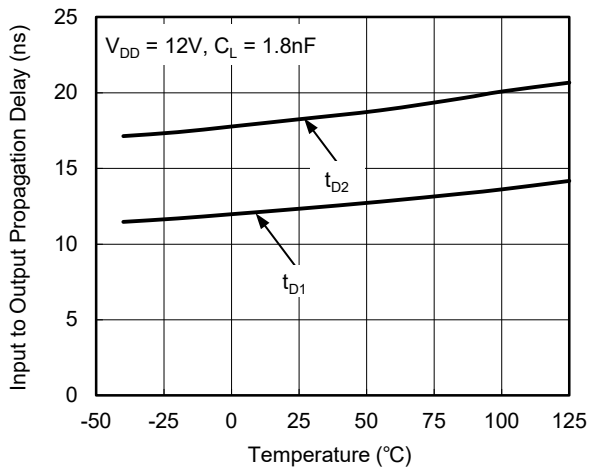
Rise Time vs. Temperature



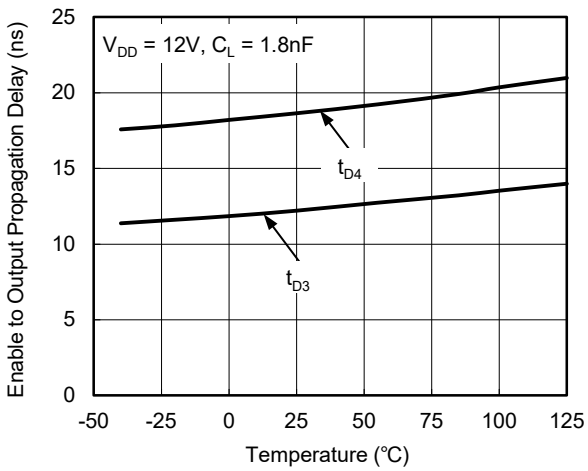
Fall Time vs. Temperature



Input to Output Propagation Delay vs. Temperature

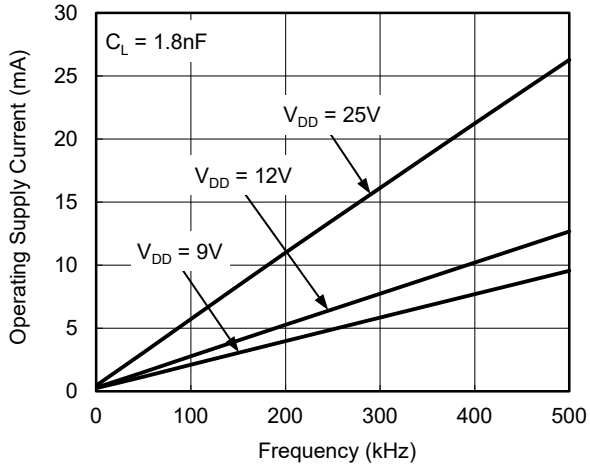


Enable to Output Propagation Delay vs. Temperature

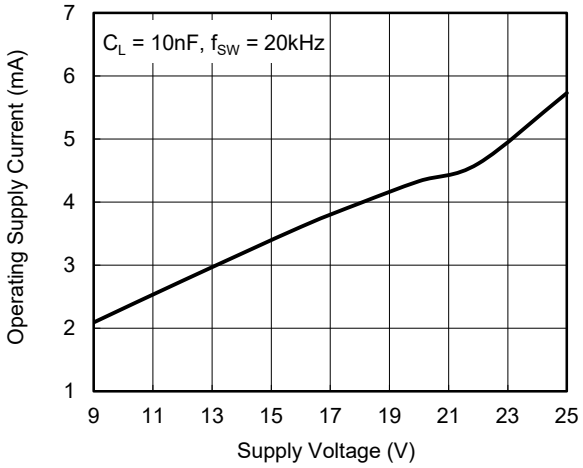


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

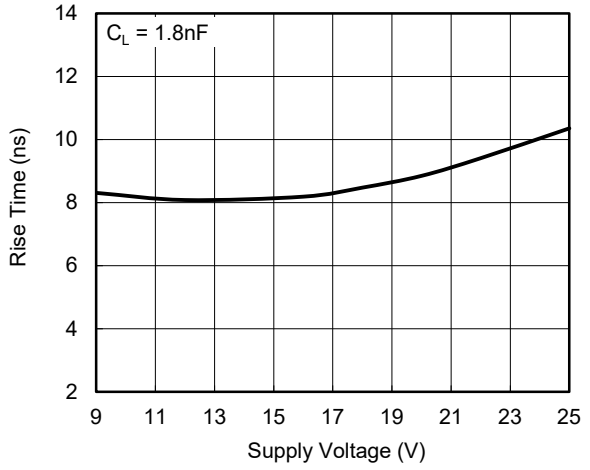
Operating Supply Current vs. Frequency



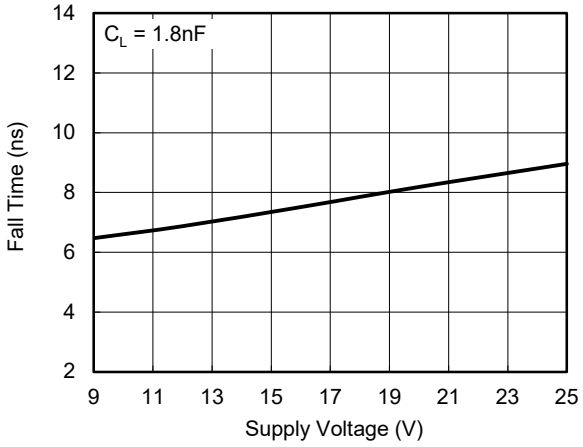
Operating Supply Current vs. Supply Voltage (Output Switching)



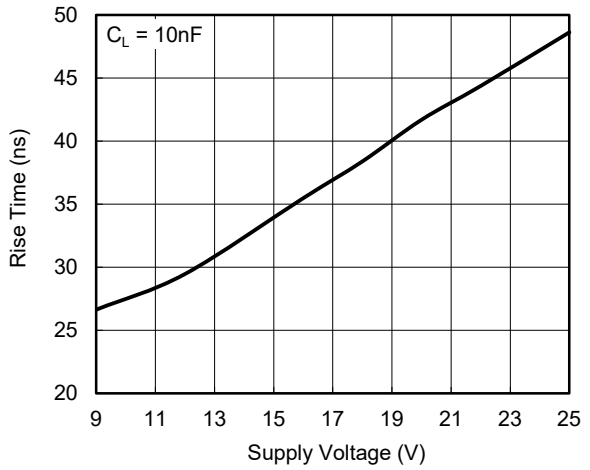
Rise Time vs. Supply Voltage



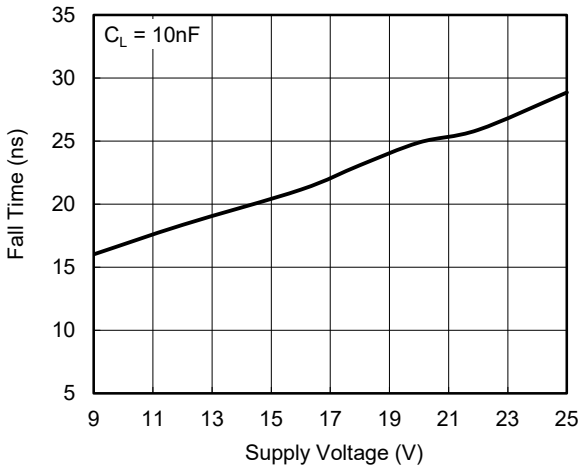
Fall Time vs. Supply Voltage



Rise Time vs. Supply Voltage

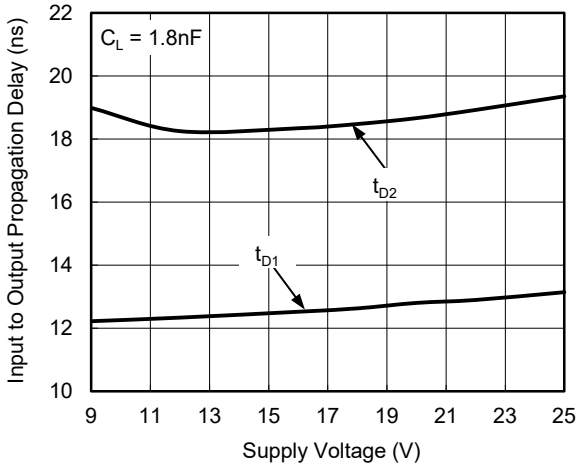


Fall Time vs. Supply Voltage

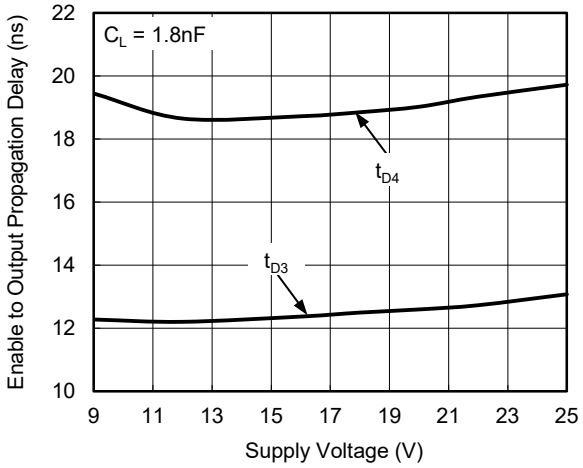


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Input to Output Propagation Delay vs. Supply Voltage



Enable to Output Propagation Delay vs. Supply Voltage



FUNCTIONAL BLOCK DIAGRAM

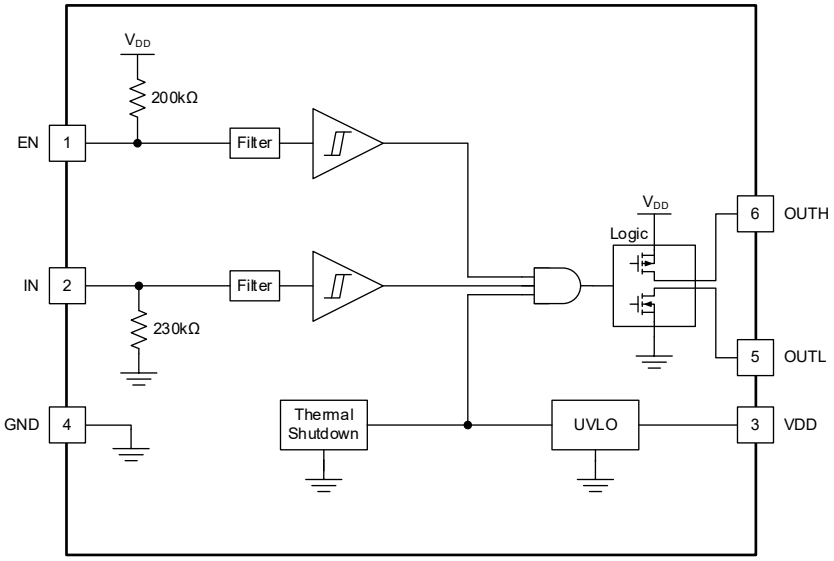


Figure 4. SGM48536BQ Block Diagram

DETAILED DESCRIPTION

The SGM48536BQ is a single high-speed low-side gate driver for MOSFET and IGBT power switches. The device can provide rail-to-rail drive capability, very small propagation delays, and 4A peak source and 8A peak sink currents (asymmetrical drive) when V_{DD} = 12V. The input can withstand a maximum negative voltage of -10V. Several other prominent features are listed in Table 1.

Table 1. Prominent Features and Benefits

Feature	Benefit
High source/sink current capability (4A/8A asymmetrical, TYP).	High current capability offers flexibility to drive various power switches at varying speeds.
Best-in-class propagation delays (18.5ns, TYP).	Very low delay and distortion in pulse transmission.
Wide supply voltage range (V_{DD} from 9V to 25V).	Design Flexibility.
Wide operating ambient temperature range (-40℃ to +125℃).	Wider system operating temperature range and smaller cooling system.
UVLO Protection on VDD.	Outputs are logic low in UVLO condition to ensure controlled and glitch-free driving during power-up and power-down.
Outputs are logic low when the input (IN) is floating.	This safety feature prevents unexpected gate pulses during abnormal situations such as the conditions tested in the safety certification.
Separate output structure option (OUTH, OUTL).	Turn-on and turn-off speeds can be independently set through series gate resistors.
CMOS/TTL compatible input with wide hysteresis	Improved noise immunity while compatible with digital logic (3.3V, 5V).
Input/enable pin voltage levels are not restricted by V_{DD}.	Simplified system especially in the auxiliary bias supply architecture.
Ability to handle -10V V_{DC} at input pins	Increased robustness in noisy environments.

DETAILED DESCRIPTION (continued)

VDD and Under-Voltage Lockout

The SGM48536BQ provides under-voltage lockout (UVLO) function to protect the driver in the event of a fault condition. The UVLO threshold is 8V (TYP), and the hysteresis voltage is 1V. Once the driver is in the UVLO state, regardless of the input state, the output will keep low.

For example, at power-up, when V_{DD} is lower than the UVLO threshold, the output of the driver remains low. After reaching the UVLO threshold, the driver outputs high, and the amplitude of the high level is consistent with V_{DD} until V_{DD} reaches a stable state. As shown in Figure 5, the PWM signal is connected to the IN pin. The output is held low until V_{DD} reaches the UVLO threshold, and then follows the input.

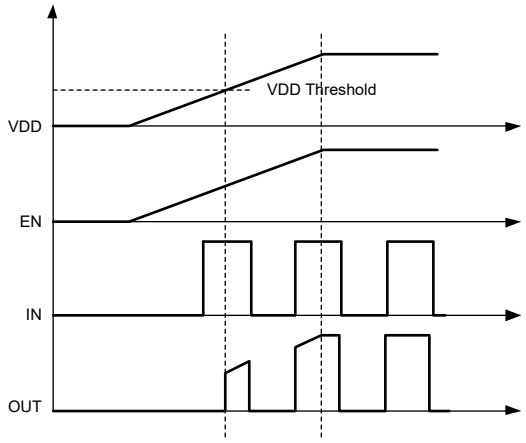


Figure 5. Power-Up in a Non-Inverting Driver Channel

To achieve better noise immunity and meet the peak drive current capability of the drive output, and to prevent noise problems, as well as to obtain the best performance of high-speed circuit, it is recommended to place two bypass capacitors as close to the VDD pin as possible. Low ESL/ESR surface mount capacitors are recommended. Place a 0.1μF ceramic capacitor as close to the VDD and GND pins as possible. Moreover, place a 1μF ceramic capacitor close to and in parallel with the 0.1μF capacitor. The 1μF capacitor is mainly used to provide the high peak current required by the load.

Operating Supply Current

The SGM48536BQ offers a very low quiescent current. The lowest quiescent I_{DD} current is generated when the gate driver is normally powered and the output is static (high level or low level). At this time, the internal logic circuit of the driver is fully operational. The total supply current is the sum of three components: the quiescent current, the average I_{OUT} current dissipated by the driving stage, and the pull-up current on the unused input pin. For example, when IN is pulled high, the internal pull-down resistor will consume a small amount of current from the VDD power supply (refer to the functional block diagram). Given the known switching frequency (f_{SW}) and MOSFET gate (Q_G) charge, the average output current is $I_{OUT} = Q_G \times f_{SW}$.

Input Stage

The input adopts a TTL and CMOS compatible structure, which will not be affected by V_{DD} and facilitate the direct drive of the PWM control signals of the 3.3V and 5V digital power controllers. It is designed with around 2V logic high and 1.2V logic low thresholds. Therefore the hysteresis voltage is 0.8V. The traditional TTL logic structure has a hysteresis usually less than 0.5V. Compared with the traditional TTL logic structure, a wider hysteresis voltage enhances the noise immunity. The device strictly controls the threshold voltage level of the input pins, simplify the system design, and ensure stable operation of the driver over the entire temperature range. The drive can operate normally at high switching frequency due to the very small input capacitance.

The device has strong noise immunity. A pull-down resistor is integrated separately inside the non-inverting input pin. Therefore, the output will remain in a stable low level state even if the input pin is floating.

The SGM48536BQ is configured with a single non-inverting input and an enable input. When the EN pin is set high, the output function of the device is normal, and the output logic is consistent with the non-inverting input logic. The device uses separate outputs (OUTH and OUTL), which can flexibly control the turn-on and turn-off strength of the drive and help reduce ground bounce.

DETAILED DESCRIPTION (continued)

The input PWM signal should have short rise or fall time. Care must be taken when the input of the driver is a slow-changing signal and the PCB layout is not optimal:

• The high di/dt output of the driver and the influence of the parasitic inductance of the PCB layout can cause ground bounce. The ground bounce will result in the differential voltage between the input pin and GND to change, and lead to the output to turn on and off by mistake, which will cause the output to oscillate at high frequency, increase power consumption, and possibly damage the device.

• Compared with standard low-side gate drivers in other industries, wider 0.8V input threshold hysteresis enhances noise immunity.

• In the worst case, that is to say, when the input signal is slow and the PCB layout is poor, place a 1nF capacitor as close as possible between the input pin of the driver and the ground to help improve the noise resistance and keep the output state stable.

In order to control the turn-on or turn-off speed of the power device, it is recommended to add an external drive resistance between the driver output and the gate of power device. Another advantage of using an external drive resistor is that it can transfer part of the power consumption of the drive and reduce the thermal stress of the drive.

Enable

The SGM48536BQ has an independent active-high enable pin. Similar to the input pin, the enable pin is independent of the supply voltage with tightly controlled thresholds and is compatible with TTL or CMOS logic. The EN pin is internally pulled up to VDD by a 200kΩ resistor in case of floating.

Low Propagation Delays

The SGM48536BQ can provide 18.5ns (TYP) propagation delay when V_{DD} = 12V, which is the best among similar products. This ensures that the signal distortion from input to output in high-frequency applications is also at the best level in the industry.

APPLICATION INFORMATION

In switching power supply applications, it is usually to use a powerful gate driver between the PWM output of the controller and the power semiconductor devices to achieve fast switching of power devices and reduce switching power loss. The PWM controller signal is usually a 3.3V logic signal that cannot directly drive the switching device. At this time, the gate driver needs to convert the 3.3V level logic command to the gate drive voltage (12V or above) to fully turn on the power devices and reduce switching power loss. Because the NPN/PNP bipolar transistor drive circuit based on the totem pole arrangement is emitter-followed output, it lacks level conversion capability and is not suitable for application in digital power supplies.

Design Requirements

The gate driver can provide level conversion and high-frequency high-current driving functions. In order to reduce the parasitic inductance in the gate drive loop and minimize the influence of noise, it is necessary to place the driver as close as possible to the power switch. Driving the gate drive can transfer the gate charge power loss to itself, thus it reduces the thermal stress of the controller. With the advent of wide band-gap power devices, such as GaN switches that support ultra-high switching frequencies, higher requirements are imposed on the drive capability of gate drivers. These requirements include low propagation delay, short rise/fall time, high peak drive current capability, and low parasitic inductance packaging. In short, the gate driver is a very important part of the switching power supply. It simplifies the system design, reduces the PCB space and the number of circuit components, and achieves a combination of low cost and high performance.

When choosing a suitable gate driver for the final design, some key parameters need to be considered comprehensively, such as operating voltage range, input logic level threshold, peak source and sink current capability, enable function, propagation delay, and package type.

Table 2. Design Parameters

Design Parameter	Example Value
Input-to-Output Logic	Non-Inverting
Input Threshold Type	TTL/CMOS Logic Level
VDD Bias Supply Voltage	12V (MIN), 15V (TYP), 16V (MAX)
Peak and Sink Currents	Minimum 4A Source and 5A Sink
Enable and Disable Function	Needed
Propagation Delay	42ns (MAX) or less

Input-to-Output Logic

When designing, at first it is necessary to determine the logical relationship between the driver input control signal and the driver output. If the driver is configured as non-inverting input, the output is high once the input signal is high when the driver is enabled, and the MOSFET or IGBT is turned on.

For applications where there is a ground bounce problem, the SGM48536BQ is recommended due to separate output structure. When the SGM48536BQ outputs high, the drive current is supplied to the MOSFET or IGBT gate through OUTH for charging. When it outputs low, the discharge current of the MOSFET or IGBT gate is absorbed through OUTL.

Input Threshold Type

The input adopts TTL and CMOS compatible structure with a wide range of hysteresis. The input level is independent of V_{DD}. It can be compatible with the logic level input signal from the digital controller, and higher voltage input signal of analog controller. Refer to the electrical characteristics for related parameters.

Supply Voltage V_{DD}

The bias supply voltage of the VDD pin cannot exceed the recommended maximum operating voltage (25V). In order to achieve the most effective turn-on and turn-off of different power devices, different voltage levels need to be applied to the gates of different power devices, such as Si MOSFET (V_{GS} = 10V, 12V) and IGBT (V_{GE} = 15V, 18V). The SGM48536BQ device has a wide operating voltage range and can drive different types of power devices.

APPLICATION INFORMATION (continued)

Peak Driving Currents

Generally, the power devices should be driven with sufficient peak current to achieve the target switching speed and the minimum the switching loss of as much as possible.

Usually the switching speed will be described by the slew rate of the drain-source voltage (dV_{DS}/dt) of the power MOSFET. For example, in a continuous conduction mode (CCM) Boost PFC-converter, the MOSFET operates in a hard-switching state. Reducing the switching power loss is critical to the system. Therefore, the system requires that the power MOSFET IPD20N60 must be turned on at a slew rate of not less than 20V/ns under a 400V DC bus voltage. This means that the MOSFET must be fully turned on in 20ns or less.

When the power MOSFET reaches the Miller plateau during the turn-on process, a drain-source voltage swing occurs. The gate driver provides a peak current for the Miller charge of the power MOSFET. Under this circumstance, the voltage between gate and source of the power MOSFET is the Miller plateau voltage. In order to achieve the target switching speed, the gate driver needs to provide Q_{GD} charge in 20ns or less (Q_{GD} = 33nC for IPD20N60, TYP). The calculation shows that the gate driver must provide a peak current of not less than 1.65A (= 33nC/20ns). The device can provide 4A peak source current, which fully meets the design requirements.

The 4A peak current drive capability of the device is 2.4 times the design requirement, which provides sufficient margin and flexibility for the design. The switching speed can be fine-tuned by adjusting the external gate resistor to achieve efficiency and EMI optimization. However, special attention should be paid to the routing and layout of the PCB gate drive loop. The parasitic inductance in the drive loop will have a serious impact on the switching speed of the power MOSFET. The parasitic inductance of the PCB driving loops will limit the di/dt of output current pulse of the gate driver, resulting in reduced switching speed.

The total gate charge of the MOSFET (Q_G of IPD20N60 = 87nC, TYP) is equal to the total area of the gate drive pulse current waveform. This pulse waveform is approximately triangular, and the area calculation equation is (½ × I_{PEAK} × time).

The parasitic inductance of the PCB traces will limit the di/dt of the drive current. If the required Q_G for power MOSFET switching is obtained, the calculated I_{PEAK} value of the current pulse will be less than actual peak current capability of the gate driver. The time in the formula will increase, which means that the switching speed becomes slower. Therefore, it may not meet the target switching speed even if the theoretical calculation shows that the driving capability of the gate driver is sufficient. In order to fully realize the peak current drive capability of the gate driver, it is necessary to place the gate driver as close to the power MOSFET as possible and design the gate drive loop with the smallest PCB trace parasitic inductance.

Enable and Disable Functions

Some applications require a separate enable pin to independently control the driver output. The SGM48536BQ can meet this requirement.

Power Dissipation

The power consumption of the gate driver is composed of static power consumption and switching loss, as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

Static power consumption $P_{DC} = I_Q \times V_{DD}$, where I_Q is the quiescent current of the whole driver, and V_{DD} is the power supply voltage of the driver. The quiescent current is the current consumed by all internal bias circuits of the driver (such as input stage, logic circuit, and protection) and the internal components of the switch when the driver output state changes. Each static current of the SGM48536BQ is very small (less than 1mA). Therefore it is considered that the static power consumption P_{DC} has a negligible effect on the total power consumption of the gate driver.

The amount of power dissipation in the device depends on the following:

- Switching frequency.
- Gate charge required to turn the MOSFET on or off.
- Size of the external gate resistors used (if any).

APPLICATION INFORMATION (continued)

Gate charge is usually a function of the drive voltage. The drive voltage is $V_{GS} \approx V_{DD}$ (the dropout of the driver, V_{OH}, is normally very low). Note that due to the low quiescent current and the internal bias power, the loss in the driver is effectively equal to the output driving losses caused by drive currents.

Using a discrete capacitor (C_g) as a similar switch gate load for testing, the loss in the driver can be easily estimated. The energy needed to charge the capacitor to the supply voltage V_{DD} is given by Equation 2:

$$E_G = \frac{1}{2} C_g V_{DD}^2 \quad (2)$$

It can be proved that the same amount of energy is dissipated in the driver output stage resistances and when the capacitor is discharged by the driver. Therefore, with a switching frequency of f_{SW}, the total power loss (in one channel) is:

$$P_G = C_g V_{DD}^2 f_{SW} \quad (3)$$

The equivalent gate capacitance could be found by test implemented on MOSFETs to determine the gate charge required for switching the device. The gate charge includes the impact of the input gate-source and drain-gate capacitances. The drain-gate capacitance also needs current for charge and discharge due to the voltage swing of the drain voltage when the power device is turning on and off. Usually the typical and maximum gate charges (Q_g) can be acquired from the specification of the power devices. Because $Q_g = C_g V_{DD}$, the power loss in the driver can be calculated from Equation 4 too:

$$P_G = C_g V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (4)$$

When an external series gate resistor, R_g, is used for MOSFET or IGBT, a portion the P_G loss will dissipate on R_g and not inside the driver. With a simplified analysis, the gate driving loss inside each channel can be calculated by Equation 5:

$$P_G = 0.5 \times Q_g \times V_{DD} \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_g} + \frac{R_{ON}}{R_{ON} + R_g} \right) \quad (5)$$

where $R_{OFF} = R_{OL}$ is the effective pull-down resistance from the channel output to the ground and $R_{ON} \approx 1.4 \times R_{OL}$ is the effective resistance of the internal pull-up stage.

Power Supply Recommendations

The SGM48536BQ driver has a rated operating power supply voltage range of 9V to 25V, and provides under-voltage protection (UVLO). When V_{DD} is lower than the UVLO threshold, the driver enters UVLO state. At this time, the output of the driver remains low and is not affected by the input signal state. The VDD pin has a 25V maximum rated operating voltage and a 28V absolute maximum voltage, with a 3V margin to prevent device damage caused by transient voltage spikes.

The UVLO hysteresis voltage is 1V, which improves the noise immunity of the power port. When V_{DD} is approximately to the UVLO threshold voltage, the ripple of the power supply needs to be controlled within the hysteresis voltage range to avoid triggering the UVLO state and causing abnormal driver output.

A low ESR/ESL ceramic capacitor needs to be placed between the VDD and GND pins and close to the IC to provide the high peak current when the FET is turned on.

In order to obtain the best transient performance, SGMICRO recommends a 0.1μF ceramic capacitor and a 1μF capacitor in parallel. Place the 0.1μF capacitor as close as possible to the IC, and place the 1μF capacitor close to the 0.1μF capacitor in parallel. The capacitance of 1μF provides enough peak drive current.

APPLICATION INFORMATION (continued)

Layout Guidelines

The SGM48536BQ integrates a fast response input circuit, short propagation delay and a powerful output stage which is capable of providing 4A peak source current and 8A peak sink current to improve the switching speed of power devices.

It is strongly recommended to use the following layout and connection guidelines:

• Keep high current output and power ground paths separate from logic input signals and signal ground paths to improve input noise immunity.

• Keep the driver as close to the load as possible to minimize the length of high-current traces. This reduces the series inductance to improve high-speed switching, while reducing the loop area that can radiate EMI to the driver input and other surrounding circuits.

• Many high-speed power supply circuits are susceptible to noise injected from their own outputs or other external sources, which may cause the output to re-trigger. These effects are especially noticeable if the circuit is tested on breadboards or non-optimal circuit layouts with long input, enable, or output leads. For best results, connect all pins as short and directly as possible.

• The turn-on and turn-off current paths should be minimized. In order to achieve the high peak current possible, the resistance and inductance in the path should be minimized.

• The decoupling capacitor between VDD and GND should be placed on the same side of the PCB. Vias are not used because the inductance of the vias may cause ringing on the IC pins.

REVISION HISTORY

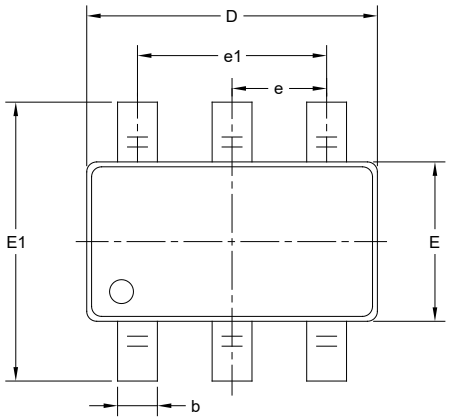
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

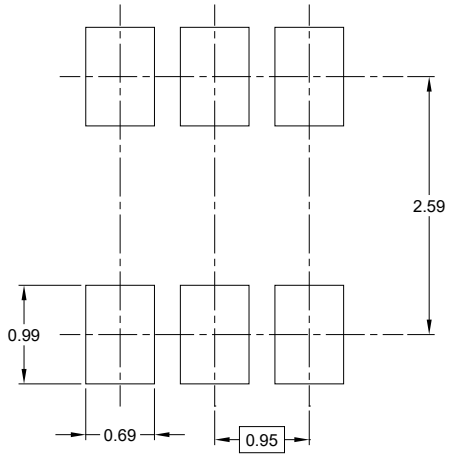
OCTOBER 2025 – REV.A to REV.A.1	Page
Added package thermal resistance	2
Changed HBM	2

Changes from Original to REV.A (MARCH 2024)	Page
Changed from product preview to production data	All

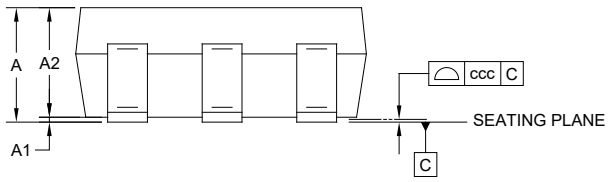
PACKAGE OUTLINE DIMENSIONS

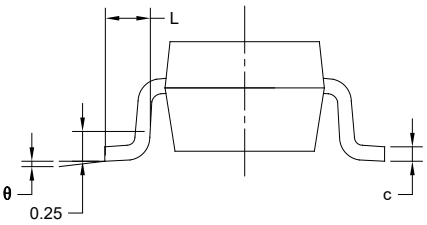
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



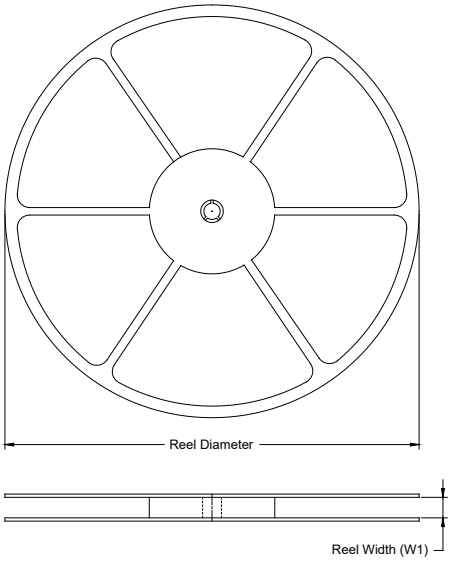


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

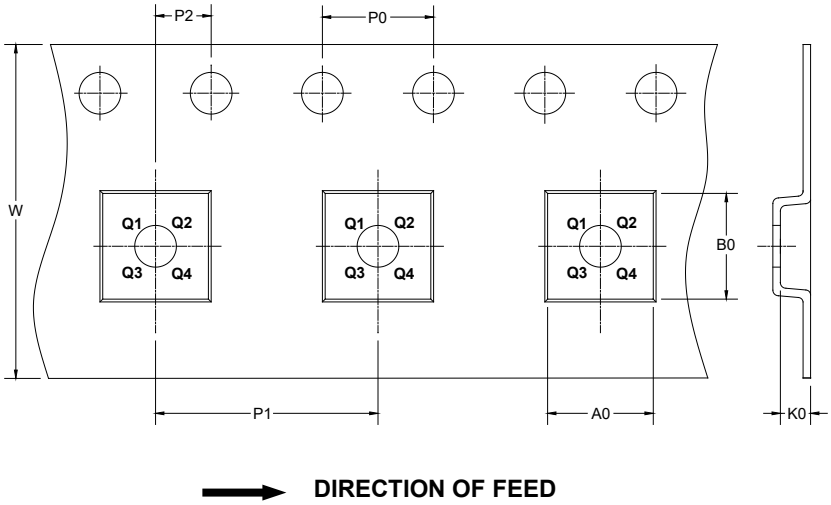
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



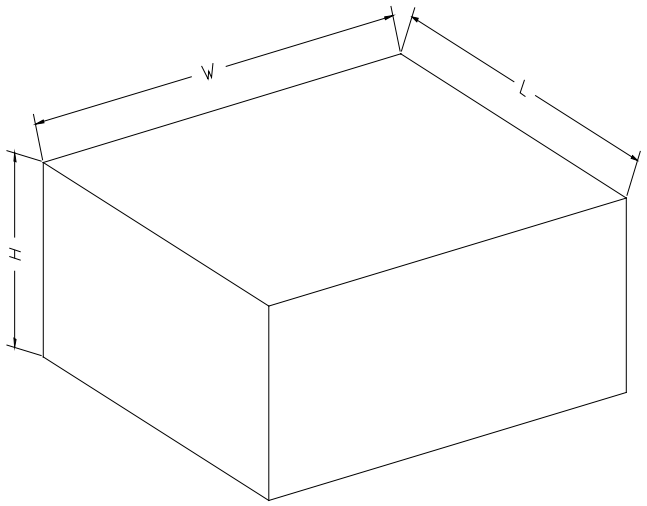
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002